Part No. 070-4421-00
Product Group 53

336
DIGITAL STORAGE OSCILLOSCOPE
SERVICE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

Please Check for CHANGE INFORMATION at the Rear of This Manual

First Printing SEP 1983
Revised MAY 1984

Tektronix®
COMMITTED TO EXCELLENCE

INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

TABLE OF CONTENTS

TABLE OF CONTENTS (cont)

LIST OF ILLUSTRATIONS

LIST OF TABLES

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply and do not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damages to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms as Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard not immediately accessible as one reads the marking.

Symbols in This Manual

This symbol indicates where applicable cautionary or other information is to be found. For maximum input voltages see Table 1-1 Electrical Characteristics.

Symbols as Marked on Equipment

DANGER—High Voltage.

Protective ground (earth) terminal.

ATTENTION—Refer to manual.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the ground conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) may be capable of rendering an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

For detailed information on power cords and types of connectors, see Table 2-1.

Use the Proper Fuse

To avoid fire hazard, use only a fuse of the correct type, voltage rating, and current rating as specified in the parts list for your product.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections or components while power is on. Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

4421-01

The 336 Digital Storage Oscilloscope.

SPECIFICATION

INTRODUCTION

The SONY®/TEKTRONIX® 336 is a combination nonstorage and digital storage, portable oscilloscope. It is capable of displaying analog and digitized waveforms simultaneously, and it can store the digitized waveforms for recall and display. The 336 is a microprocessor controlled instrument that incorporates alphanumeric crt readouts of the vertical and horizontal scale factors, the delay time position, and voltage and time readouts of the cursor positions. Many of the oscilloscope features and modes are chosen from a menu displayed on the crt rather than from hard-wired front-panel switches. Menu-selectable operating modes are described in Section 2, "Operating Information."

The 336 has a dual-channel, dc-to-50 MHz vertical deflection system for both nonstorage and equivalent-time digitizing. Storage bandwidth for single-sweep events (waveforms acquired as the result of a single triggering event) is dc-to-140 kHz. The vertical channels have calibrated deflection factors from 5 mV to 10 V per division with a choice of either AC or DC input coupling. In the NON STORE Mode, the 336 operates similarily to a conventional oscilloscope,

The horizontal deflection system's calibrated, nonstorage sweep rates are from 0.2 s to 0.1 μs per division for the A Sweep and from 50 ms to 0.1 μs per division for the B Sweep. The sweep speed of all sweeps (both nonstore and digitized) is increased by ten times with the use of the X10 MAG feature. Either variable sweep speed between the calibrated settings of the SEC/DIV switch or variable holdoff is available by selecting the function of the front-panel VAR SWP/HOLDOFF control from the SCOPE Menu choices. Variable sweep speed extends the slowest A Sweep rate to at least 0.5 s per division. STORE Mode sweep speed is not variable for acquisitions made during a single sweep (0.2 s to 0.1 ms per division), but the control does vary the STORE mode sweep for equivalent-time sampling (50 μs to 0.1 μs per division). Variable holdoff increases the NON STORE holdoff time by up to ten times normal. STORE display holdoff times are a function of the microprocessor operation and are not directly controllable from the front-panel.

Horizontal Display Modes for NON STORE sweeps are selected from a choice of A Sweep, B Delayed Sweep, or A Intensified alternated with B Delayed (ALT) for the time X-axis displays. X-axis drive for the X-Y displays is obtained from the CH 1 OR X input signal, while vertical deflection for the X-Y display is provided by the CH 2 OR Y input signal. The NON STORE X-Y display cannot be digitized, but the STORE and VIEW digitized waveforms do have a menu-selectable X-Y Display Mode.

When the ALT Horizontal Display Mode is selected, trace separation between the A Intensified Sweep and the B Sweep is menu selectable from zero to two divisions in 0.5 division steps.

In the STORE Mode, the 336 has a useful storage bandwidth of dc-to-50 MHz for equivalent-time sampling of repetitive signals and a dc-to-140 kHz useful storage bandwidth for signals acquired during a single sweep. Acquired signals will be displayed with a bright, flicker-free trace. Digital storage horizontal acquisition range is 50 μs to 0.1 μs per division for equivalent-time sampling (multiple sweeps required to obtain the waveform) and 0.2 s to 0.1 ms per division for real-time acquisitions (waveforms are acquired during a single sweep). The Horizontal Display Mode must be set to either A only or B delayed only to enable the STORE Mode. (It is not enabled during ALT Horizontal Display Mode.)

A ROLL Mode storage feature, with a range of 20 s to 0.5 s per division, is very useful for viewing low-frequency and low-repetition rate signals. The ROLL Mode is automatically entered when the SEC/DIV switch is set to 0.5 s per division or slower. Waveform data is acquired and displayed in a scrolling manner as the display moves from right to left on the crt.

The digital storage acquisition modes are NORMAL, ENVELOPE, and AVERAGE. NORMAL and AVERAGE Storage are useful over the entire STORE Display Mode SEC/DIV range (0.2 s to 0.1 μs per division); ENVELOPE Storage Mode functions from 2 ms to 0.2 s per division and is not enabled outside of that range of sweep speeds. Waveforms acquired during a single sweep (real-time sampling) have a trigger-point selection feature available. The menu-selected feature allows the user to choose PRE TRIG, MID TRIG, or POST TRIG data acquisition for viewing data prior to, on either side of, and after the single-sweep triggering event. Equivalent-time sampling (50 μs to 0.1 μs per division) is done with a Full Post Trig acquisition window (all the waveform data acquired occurs after the trigger event).

Digitized STORE waveforms are entered into the VIEW memory by pressing the ENTER push button. The stored waveform is recalled for display or processing by pressing

the VIEW push button. For making waveform comparisons, a single channel VIEW and STORE display of the CH 1 waveform may be displayed simultaneously (CH 1 VERT MODE). However, when any VERT MODE other than CH 1 is selected, VIEW and STORE waveforms can not be displayed together. Either VIEW or STORE waveforms may be displayed with the NON STORE waveforms.

In either STORE or VIEW Display Mode, cursors may be used to make simultaneous voltage and time measurements on the digitized waveform displays. The measurement results are displayed as a crt readout having three-digit resolution.

Two types of waveform processing are also available on the digitized displays. A menu-selected feature enables either addition, subtraction, and multiplication of the CH 1 and CH 2 waveforms or the calculation of the rms, peak-to-peak, and mean values of the waveforms with direct crt readout of the calculation results.

The 336 trigger circuitry has A Trigger Modes of p-p AUTO, NORMAL, and SINGLE Sweep. The B Trigger Modes are RUNS AFTER DELAY and Triggerable After Delay. Trigger SOURCE and COUPLING choices are the same for both A and B Trigger signals. Push-button controls are used to select CH 1 SOURCE and AC COUPLING. The remaining Trigger SOURCES (CH 2, EXT, EXT/10, and LINE) are selected under MENU control as are the remaining Trigger COUPLING Modes (DC, HF REJ, LF REJ, and TV SYNC). An LED is lighted behind the clear plastic push buttons to indicate when a particular mode or menu is selected.

An analog X-Y output feature permits the use of an external X-Y Plotter for making hard copies of the VIEW waveforms. This feature is menu controllable and has a choice two plotting speeds: FAST and SLOW. Calibration signals provided by the 336 enable the user to calibrate the X-Y Plotter deflection to the instrument's graticule.

The Option 01 for the 336 combines the General Purpose Interface Bus (GPIB) and an extended memory in one option package. The GPIB is a menu-selectable feature that enables a GPIB controller to obtain the stored waveform data over an eight-bit, parallel IEEE-488 data bus. The waveform data can then be either stored for future reference or analyzed to determine the waveform parameters. The 336 GPIB feature can be set up either to be addressed to talk or as a talker only. Setting of the instrument's my talk address (mta) or the TALK-ONLY Mode (TON) is done under menu control. The 336 GPIB interface is a talker only and, as such, has no remote control capability of the front panel settings.

Optional extended memory adds storage for up to eight stored frames (16 stored waveforms) to the standard instrument's one-frame (two-waveform) storage capability to provide a VIEW memory stack capable of storing 18 waveforms. The option includes a battery backup that maintains the stored data, the front-panel switch settings, and menu selections that were in effect at power off. With Option 01 installed, the instrument powers on with the same operating conditions present at power off (diagnostic mode excluded).

Additional options not affecting the instrument's operation are the selection of the proper power cord for international use. Options A1 through A5 provide a selection of the most used power cord plugs, and the instrument comes equipped with the option requested at the time of ordering.

The 336 is shipped with the following standard accessories:

2 Probe packages
1 Instrument accessories pouch
1 Zip-lock accessories pouch
1 Operators manual
1 Service manual
1 Power cord (as per power cord option ordered)
1 1.5 A, 250 V fuse
1 Front-panel cover
1 Menu diagram label (installed in the front-panel cover)
1 Clear plastic crt filter

For part numbers and further information about both standard and optional accessories, refer to either "Options and Accessories" (Section 7) in the Operators manual or the Accessories information at the rear of this manual. Your Tektronix representative or local Tektronix Field Office can also provide accessories information and ordering assistance.

PERFORMANCE CONDITIONS

The following electrical characteristics (Table 1-1) are valid for the 336 when it has been adjusted at an ambient temperature between +20°C and +30°C, has had a warm-up period of at least 20 minutes, and is operating at an ambient temperature between 0°C and +55°C for the standard instrument or between 0°C and +45°C for the Option 01 instrument (unless otherwise noted).

Items listed in the "Performance Requirements" column are verifiable qualitative or quantitative limits that define the measurement capabilities of the instrument.

Environmental characteristics are given in Table 1-2. The environmental tests performed meet MIL-T-28800B, Type III, Class 3, Style D, for Altitude, Vibration, and Shock.

Mechanical characteristics of the 336 are listed in Table 1-3, and Option 01 characteristics are given in Table 1-4.

Table 1-1
Electrical Characteristics

Characteristics	Performance Requirement
VERTICAL DEFLECTION SYSTEM	
Deflection Factor	
Range	5 mV per division to 10 V per division in a 1-2-5 sequence of 11 steps.
Accuracy (NON STORE Mode)	Graticule indication is within ±3%.
Uncalibrated (VAR) Range (NON STORE Mode)	Continuously variable between settings of the VOLTS/DIV switch. Extends deflection factor of 10 V per division setting to at least 25 V per division.
Frequency Response (NON STORE Mode)	Five-division reference signal from a terminated 50 Ω system, with VAR VOLTS/DIV in the calibrated detent (CAL).
Bandwidth (Channel 1 and Channel 2)	
0°C to +40°C	DC to at least 50 MHz.
+40°C to +55°C	DC to at least 40 MHz.[a]
ADD Mode	
0°C to +55°C	DC to at least 30 MHz.
AC Coupled Lower −3 dB Point	
1X Probe	10 Hz or less.[a]
10X Probe	1 Hz or less.
Step Response (NON STORE Mode)	Four-division reference signal, dc coupled at all deflection factors, from a 50 Ω terminated system; vertically centered with the VAR VOLTS/DIV in the calibrated detent (CAL).
Rise Time	
0°C to +40°C	7 ns or less (calculated).[a] Rise Time $= \frac{0.35}{\text{BW (in MHz)}}$
Input R and C	
Resistance	1 MΩ, within 2%.[a]
Capacitance	Approximately 33 pf.[a]
Maximum Input Voltage ⚠	
AC and DC Coupled	200 V (dc + peak ac); 200 V p-p ac at 1 kHz or less.
DIGITAL STORAGE VERTICAL ACQUISITION	
Accuracy	Scaled binary value of the stored digital word is within 3% of true input voltage.

Table 1-1 (cont)

Characteristics	Performance Requirement
DIGITAL STORAGE VERTICAL ACQUISITION (cont)	
Useful Storage Bandwidth	
Real Time Sampling	With SEC/DIV switch set to 0.1 ms per division. DC to 140 kHz (7 samples per cycle at 140 kHz).[a]
Equivalent Time Sampling	Five-division reference signal, vertically centered.
0°C to +40°C	DC to at least 50 MHz.
+40°C to +55°C	DC to at least 40 MHz.[a]
Signal Averaging	
Range	8, 16, 32, 64, 128, or 256 waveforms.
Envelope Mode (2 ms to 0.2 s per division)	
Range	1, 8, 16, 32, 64, 128, or 256 waveforms and continuous.
Frequency Response	Five-division reference signal, vertically centered. DC to 10 MHz at −3 dB.
Minimum Pulse Width	At least 10 μs (−10% amplitude).[a]
TRIGGERING	
Sensitivity (NORM Trigger Mode)	When using EXT/10 SOURCE, multiply external requirements by 10.
AC Coupled	0.3 division internal or 70 mV external from 30 Hz to 10 MHz; increasing to 1.5 divisions internal or 350 mV external up to 50 MHz.
LF REJ Coupled	0.5 division internal or 140 mV external from 50 kHz to 10 MHz; increasing to 1.5 divisions internal or 700 mV external up to 50 MHz. (Attenuates signals below approximately 50 kHz.)
HF REJ Coupled	0.5 division internal or 140 mV external from 30 Hz to 50 kHz. (Attenuates signals above approximately 50 kHz.)
DC Coupled	0.3 division internal or 70 mV external from dc to 10 MHz; increasing to 1.5 divisions internal or 350 mV external up to 50 MHz.
Trigger Jitter	
NON STORE Mode	1 ns or less at 50 MHz with SEC/DIV set for 10 ns per division and X10 MAG on.
STORE Mode (real-time sampling only)	±1 sample period.
External Trigger Inputs	
Maximum Input Voltage ⚠	200 V (dc + peak ac); 200 V p-p ac at 1 kHz or less.[a]
Input Resistance	
External SOURCE Selected	1 MΩ, within 10%.[a]
External SOURCE not Selected	1.13 MΩ, within 10%.[a]
Input Capacitance	Approximately 33 pf.[a]

Table 1-1 (cont)

Characteristics	Performance Requirement	
	TRIGGERING (cont)	
LEVEL Control Range		
EXT	At least ±1 V.	
EXT/10	At least ±10 V.	
A External Trigger View (NON STORE Mode and DC Trigger COUPLING)		
Deflection Factor		
EXT	100 mV per division, ±5%.	
EXT/10	1 V per division, ±5%.	
Rise Time	10 ns or less.[a]	
Bandwidth		
0°C to +44°C	DC to at least 35 MHz.	
+40°C to +55°C	DC to at least 25 MHz.	
Acquisition Window Trigger Point		
Real Time Sampling (single-sweep storage)		
PRE TRIG	7/8 of the waveform acquisition window occurs prior to the triggering event.	
MID TRIG	4/8 of the waveform acquisition window occurs prior to the triggering event.	
POST TRIG	1/8 of the waveform acquisition window occurs prior to the triggering event.	
Equivalent Time Sampling (multiple-sweep storage)	Full post trigger. Trigger point is approximately 1 division + 300 ns prior to the start of the acquisition window.	
	TV SYNC SEPARATOR	
Triggering	With CH 1 and CH 2 Input Coupling switches set to DC.	
Sync Separation	Stable video rejection and sync separation from sync-negative NTSC or PAL composite video.	
Trigger Amplitude	**Min**	**Max**
Internal		
Composite Video (Nominal)[b]	1.5 div	15 div
Composite Sync	0.5 div	20 div
External		
Composite Video (Nominal)	300 mV	1.5 V
Composite Sync	50 mV	2.0 V
EXT/10		
Composite Video (Nominal)	3 V	15 V
Composite Sync	500 mV	20 V

Table 1-1 (cont)

Characteristics	Performance Requirement	
HORIZONTAL DEFLECTION SYSTEM		
Sweep Rate (NON STORE Mode)		
Calibrated Range		
A Sweep	0.2 s per division to 0.1 μs per division in a 1-2-5 sequence of 20 steps. X10 MAG extends the maximum sweep rate to 10 ns per division.	
B Sweep	50 ms per division to 0.1 μs per division in a 1-2-5 sequence of 18 steps. X10 MAG extends the maximum sweep rate to 10 ns per division.	
Accuracy	Within the given percentages of the indicated value. Accuracy specification applies over the center eight divisions. Exclude the first and last 50 ns of the 10 ns and 20 ns per division sweep rates when in X10 MAG.	
	Unmagnified	**Magnified**
+20°C to +30°C	Within 2%	Within 3%
0°C to +55°C	Within 3%[a]	Within 4%[a]
Two-division Linearity Check	Over any two-division portion of center eight divisions. Exclude the first and last 50 ns of the 10 ns and 20 ns sweep rates when in X10 MAG.	
	Unmagnified	**Magnified**
+20°C to +30°C	Within 4%	Within 5%
0°C to +55°C	Within 5%[a]	Within 6%[a]
Differential Time Measurement Accuracy (NON STORE Mode)		
+15°C to +35°C	Within ± (1.5% of the indicated value +1% of the A SEC/DIV switch setting).	
0°C to +15°C and +35°C to +55°C	Within ± (2.5% of the indicated value +1% of the A SEC/DIV switch setting).	
Delay Time Jitter (NON STORE Mode)	1 part or less in 10,000 (0.01% of 10 times the A SEC/DIV switch setting).	
Calibrated Delay Time (VAR SEC/DIV control in the calibrated detent)	Continuous from 1 μs to at least 1.9 s after the delaying (A) sweep.	
Delay Time Resolution	14 bit.[a]	
Alternate Sweep (ALT) (NON STORE Mode)		
Trace Separation (TRACE SEP) (Menu Selectable)	Approximately 0, 0.5, 1.0, 1.5, or 2.0 divisions.	
Variable Range (VAR SEC/DIV) (A Sweep and NON STORE Mode)	Continuously variable between calibrated settings of the A SEC/DIV switch. Extends the slowest A Sweep rate to at least 0.5 s per division.	

Table 1-1 (cont)

Characteristics	Performance Requirement
HORIZONTAL DEFLECTION SYSTEM (cont)	
X-Y Operation (NON STORE Mode)	
X-Axis Deflection Factor	Same as vertical system.
Variable Range	Same as vertical system.
X-Axis Bandwidth	With an eight-division reference signal. DC to at least 1 MHz.
Input Resistance	Same as vertical system.[a]
Input Capacitance	Same as vertical system.[a]
Maximum Useable Input Voltage ⚠	Same as vertical system.[a]
Deflection Accuracy	Graticule indication is within 4% of true input voltage.
DIGITAL STORAGE HORIZONTAL ACQUISITION	
Range	
Equivalent Time Sampling	50 μs per division to 0.1 μs per division.
Real Time Sampling	0.2 s per division to 0.1 ms per division.
Roll Mode	20 s per division to 0.5 s per division.
Envelope Mode	0.2 s per division to 2 ms per division.
Accuracy (Sample Period)	
Real Time Sampling	Sample clock is within 0.1% of the selected sample period.[a]
Equivalent Time Sampling	Exclude the first and last 0.5 division of the X1 Horizontal Acquisition Window.
+20°C to +30°C	Within 3%.
0°C to +20°C and +30°C to +55°C	Within 4%.[a]
Dynamic Range	10.24 divisions.[a]
STORAGE DISPLAY	
Vertical	
Resolution	8 bit.[a]
Differential Accuracy	Graticule indication of voltage cursor difference is within 2% of readout value, measured over the center six divisions.
Horizontal	
Resolution	10 bit.[a]
Differential Accuracy	Graticule indication of time cursor difference is within 2% of the readout value, measured over the center eight divisions.

Table 1-1 (cont)

Characteristics	Performance Requirement
READOUT	
CURSOR Accuracy	
ΔV	Within ±(3% of reading + 4% of VOLTS/DIV switch setting).
Δt	
Real Time Sampling Acquisitions	Within ±0.1% of full scale. Full-scale both vertically and horizontally is 10.24 divisions.
Equivalent Time Sampling Acquisitions	
+20°C to +30°C	Within 3%.
0°C to +55°C	Within 4%.[a]
PROCESS	
Process Accuracy	
WFM	
CH 1 + CH 2	Within 6%.
CH 1 − CH 2	Within 6%.
CH 1 X CH 2	Within 7%.
PARAMETERS	Without window effect.
RMS	Within ±(3% + 6% of VOLTS/DIV setting).
P-P	Within ±(3% + 4% of VOLTS/DIV setting).
MEAN	Within ±(3% + 4% of VOLTS/DIV setting).
CHART OUTPUT	
Clock Rate	FAST or SLOW (menu selectable).
Amplitude	500 mV per division, ±10%.
Output Impedance	220 Ω, ±10%.[a]
CALIBRATOR	
Output Voltage	
0°C to +40°C	0.3 V, within 1%.
Repetition Rate	Approximately 1 kHz.
Output Resistance	Approximately 5 kΩ.[a]
Z-AXIS INPUT	
Sensitivity	3 V p-p signal causes noticeable modulation at normal display intensity. (Positive signal decreases intensity.)
Useable Frequency Range	DC to 1 MHz.[a]
Input Resistance	At least 10 kΩ.[a]
Maximum Input Voltage ⚠	25 V peak, maximum.[a]

Table 1-1 (cont)

Characteristics	Performance Requirement
POWER SOURCE	
Line Voltage Ranges	
115 V (Nominal)	90 V to 132 V ac.
230 V (Nominal)	180 V to 250 V ac.
Line Frequency	48 Hz to 440 Hz.[a]
Power Consumption	
Maximum	50 watts (75 VA).[a]
Typical	35 watts (55 VA).[a]

[a]Performance requirement not checked in manual.
[b]Peak video is approximately 7/3 sync amplitude for nominal video signal.

Table 1-2
Environmental Characteristics

Characteristics	Performance Requirements
	Environmental tests performed meet MIL-T-28800B, Type III, Class 3, Style D, for Altitude, Vibration, and Shock.
Temperature	
Nonoperating (Storage)	
Standard Instrument	−25°C to +75°C.
Option 01 Instrument	−20°C to +65°C.
Operating	
Standard Instrument	0°C to +55°C.
Option 01 Instrument	0°C to +45°C.
Altitude	
Nonoperating (Storage)	To 50,000 feet.
Operating	To 15,000 feet. Maximum operating temperature decreases 1°C for each 1,000 feet above 5,000 feet.
Humidity	
Nonoperating	Five cycles (120 hours) of MIL-STD-202D. Omit freezing and vibration. Performance test passed after drying period at +25°C ±5°C at 20% to 80% relative humidity.
Vibration	
Operating	A 15-minute sweep along each of three major axes at a total displacement of 0.025 inch p-p (four g at 55 Hz), with frequency varied from 10 Hz to 55 Hz to 10 Hz. Hold 10 minutes at each major resonance, or if no major resonance present, hold 10 minutes at 55 Hz.
Shock (Operating and Nonoperating)	30 g, half-sine, 11-ms duration, three shocks per axis in each direction for a total of 18 shocks.
EMI (electromagnetic interference)	Meets MIL-STD-461B when tested in accordance with the following test methods of MIL-STD-462: CE01, CE03, CS02, RE02 (limited to 1 GHz), RE04, RS01, and RS03 (limited to 1 GHz).
Packaged Transportation Drop	Meets the limits of the National Safe Transit Association test procedure 1A-B-2; 10 drops of 36 inches (Tektronix Standard 062-2858-00).
Packaged Transportation Vibration	Meets the limits of the National Safe Transit Association test procedure 1A-B-1; excursion of 1 inch p-p at 4.68 Hz (1.1 g) for 30 minutes (Tektronix Standard 062-2858-00).
Bench Handling (with and without cabinet installed)	Meets MIL-STD-810C, Method 516.2, Procedure V (MIL-T-28800B, Section 4.5.5.4.4).

Table 1-3
Mechanical Characteristics

Characteristics	Description
Weight	
Without Panel Cover, Accessories, and Accessory Pouch	
Standard Instrument	5.0 kg (11.1 lb).
Option 01 Instrument	5.1 kg (11.3 lb).
Height	
With Feet	112 mm (4.41 in).
Width	
With Handle	237 mm (9.33 in).
Without Handle	194 mm (7.64 in).
Depth	
Handle Extended	482 mm (18.98 in).
Without Handle	370 mm (14.57 in).
With Front Panel	375 mm (14.75 in).

Table 1-4
Option Characteristics

Characteristics	Performance Requirements
OPTION 01—GENERAL PURPOSE INTERFACE BUS (GPIB) AND EXTENDED MEMORY	
Interface Function	SH1 Source Handshake. AH1 Acceptor Handshake. T1 Basic talker, Talk Only mode, serial poll. L0 No Listener. SR1 Service Request. RL0 No Remote/Local. PP0 No Parallel Poll. DC2[a] Device Clear. DT0 No Device Trigger. C0 No Controller.
Waveform Data	Will conform to Tektronix Interface Standard (GPIB Codes, Formats, Conventions, and Features Standard, 062-1780-02). With no waveform data acquired, only the ID part of the waveform message will be transmitted.
Battery (NiCd)	
Nominal Capacity	3.6 V, 50 mAH.
Data Retention[b]	At least three days (after eight hours of operation).
Extended Memory	16 kbyte (up to eight frames of two waveform storage capacity). (Added to the standard instrument's 2 kbyte VIEW memory.)

[a]If device clear (DCL) is received during transmission of data, the 336 goes to a state of having to restart the transmission, and the buffer containing the ID and waveform message is cleared. The 336 remains addressed to talk, and does not have to receive a new My Talk Address (MTA) to become a talker again. When DCL is removed, the 336 restarts the ID and waveform from the beginning. To cease the transmission, the controller must sent DCL and UNTALK. After stopping the transmission in this manner, a new MTA must be received to start transmitting again. The DCL will clear any service request and all pending events except power on. DCL will not clear an SRQ issued as part of the power-on routine. To remove the power-on SRQ, the instrument must be made a talker, and the status byte sent. This action ensures that the controller knows the 336 is powered up on the bus.

[b]All the front panel settings except RESET and all the menu-selectable functions except PROCESS and DATA OUT are retained in memory. The stored ground references and GPIB address are also retained as is the waveform data stored in the VIEW memory stack.

OPERATING INFORMATION

This section of the manual provides information on instrument installation and power requirements, and the functions of controls, connectors, and indicators are described. Operating considerations, intended to familiarize the operator with basic measurement techniques, and operator's checks and adjustments for the 336 are included. For additional operating information, refer to the 336 Operators Manual.

PREPARATION FOR USE

SAFETY CONSIDERATIONS

Refer to the Safety Summary at the front of this manual for power source, grounding, and other safety considerations pertaining to the use of the instrument. Before connecting the oscilloscope to a power source, read entirely both this section and the Safety Summaries.

CAUTION

This instrument may be damaged if operated with the Line Voltage Selector set for the wrong applied ac source voltage or if the wrong fuse is installed.

LINE VOLTAGE SELECTION

The 336 operates from either a 115-V or 230-V nominal ac power source having a line frequency ranging from 48 to 440 Hz. Before connecting the power cord to a power-input source, verify that the Line Voltage Selector is set to the proper nominal voltage. To determine the Line Voltage Selector setting, locate the setting indicator on the rear panel of the instrument (refer to Figure 2-1). The nominal voltage and the range over which the instrument will operate are indicated by the installation of a black, Phillips-head screw. If the internal voltage selection is not correct for your location, use the following procedure to change the setting.

1. Remove the instrument cabinet. (See Cabinet removal instructions in the "Maintenance" section of this manual.

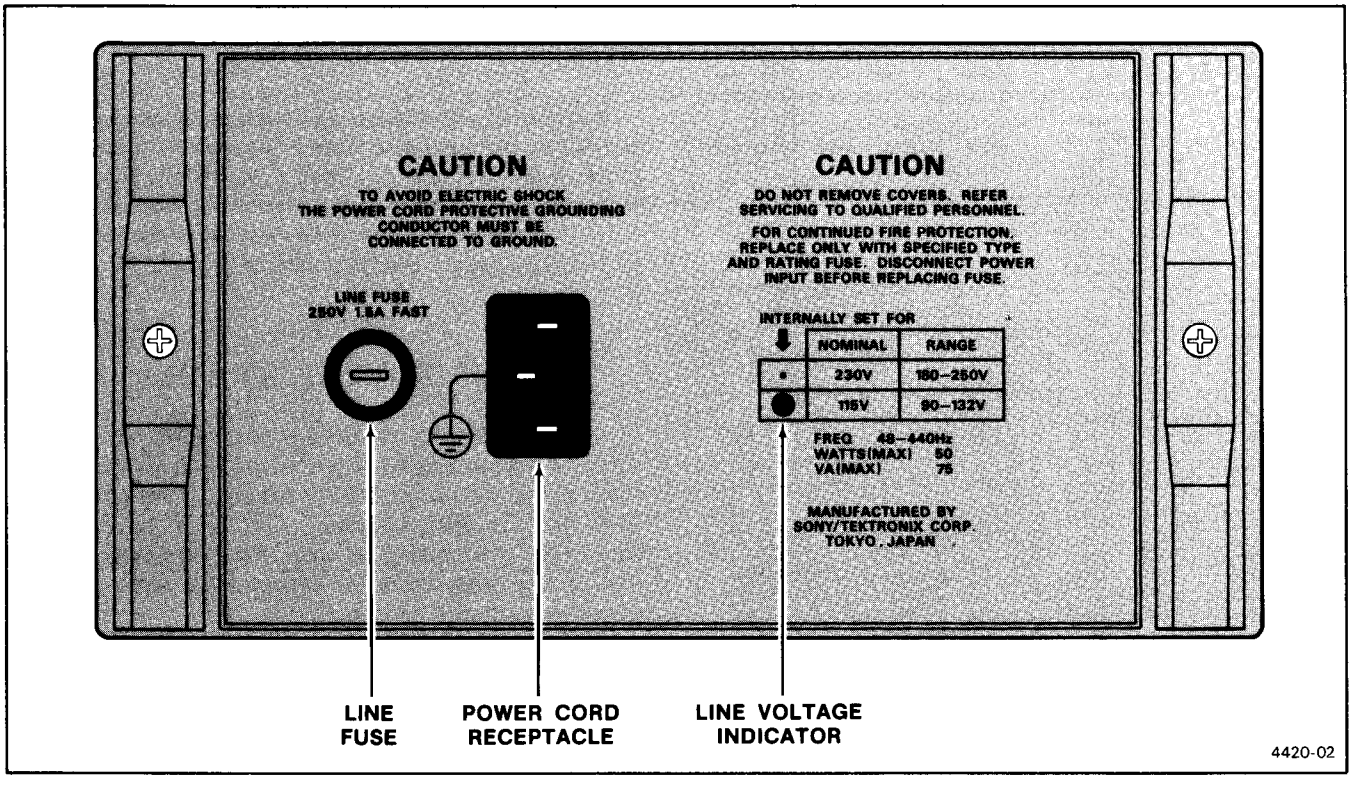


Figure 2-1. Line voltage indicator, line fuse, and power cord receptacle.

2. Remove the top cover of the power supply module.

NOTE

The last screw at the rear on the left side of the instrument holds the heat sink for the power supply switching transistor. Do not remove it.

3. The line voltage selector plug is located under a plastic shield at the top rear of the power supply module. Line voltage selection positions are printed on the shield.

WARNING

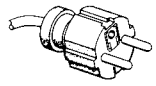
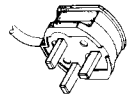
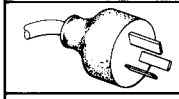
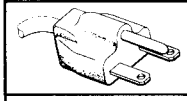
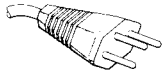
The power supply filter capacitors retain a charge for a short period of time after the power is turned off. Use care not to come in contact with exposed connections when moving the line voltage selector.

4. Pull the line voltage selector off the square-pins and move it to the correct line voltage range.

5. Replace the top cover of the power supply.

6. Reinstall the instrument cabinet.

Table 2-1
International power cord data

Plug Configuration	Usage	Line Voltage	Reference Standards	Option Number
	North American 120V/ 15A	120V	ANSI C73.11 NEMA 5-15-P IEC 83	Standard
	Universal Euro 240V/ 10-16A	240V	CEE (7),II,IV,VII IEC 83	A1
	UK 240V/ 13A	240V	BS 1363 IEC 83	A2
	Australian 240V/ 10A	240V	AS C112	A3
	North American 240V/ 15A	240V	ANSI C73.20 NEMA 6-15-P IEC 83	A4
	Switzerland 220V/ 6A	220V	SEV	A5

Abbreviations:
ANSI — American National Standards Institute
AS — Standards Association of Australia
BS — British Standards Institution
CEE — International Commission on Rules for the Approval of Electrical Equipment
IEC — International Electrotechnical Commission
NEMA — National Electrical Manufacturer's Association
SEV — Schweizevischer Elektrotechischer Verein

2931-21

7. Move the line voltage indicator, on the rear panel, to the correct position.

LINE FUSE

To verify that the instrument line fuse is of the proper value, perform the following procedure:

1. Press in the fuse-holder cap and release it with a slight counterclockwise rotation.

2. Pull the cap (with the attached fuse inside) out of the fuse holder.

3. Verify proper fuse value (1.5 A, fast-blow, 3AG).

4. Install the proper fuse and reinstall the fuse and cap in the fuse holder.

POWER CORD

This instrument has a detachable, three-wire power cord with a three-contact plug for connection to both the power source and protective ground. The protective-ground contact on the plug connects (through the power cord protective-grounding conductor) to the accessible metal parts of the instrument. For electrical-shock protection, insert this plug into a power-source outlet that is properly grounded.

Instruments are shipped with the required power cord as ordered by the customer. Available power-cord information is presented in Table 2-1. Part numbers are listed in the Accessories information at the rear of this manual. Contact your Tektronix representative or local Tektronix Field Office for additional power-cord information.

INSTRUMENT COOLING

To prevent instrument damage from overheated components, adequate internal airflow must be maintained at all times during operation. Before turning on the power, first verify that the air-intake holes in the top of the instrument cabinet and the fan-exhaust holes in the right side panel are free of any obstructions to airflow. After turning on the power, verify that the fan is on.

START-UP

The 336 automatically performs power-up tests each time the instrument is turned on. The purpose of these tests

is to provide the user with the highest possible confidence level that the instrument if fully functional. If no faults are encountered, the power-up test normally will be completed in under five seconds, after which the instrument will enter the normal operating mode. A failure of any of the power-up test will be indicated by error message display on the crt. If an error message should appear, turn off the power and then turn it back on again to ascertain if the error occurs a second time. The instrument's ability to function for any type of measurement depends on the nature of the failure and the circuitry involved. If the failure persists, refer the instrument to a qualified service technician for repairs.

Additional information on the power-up test and operator-initiated diagnostics may be found in "Maintenance" (Section 6) in this manual. Consult your service department, your local Tektronix Service Center, or nearest Tektronix representative if additional assistance is needed.

REPACKAGING FOR SHIPMENT

If this instrument is to be shipped by commercial transportation, it is recommended that it be packaged in the original manner. The carton and packaging material in which your instrument was shipped to you should be saved and used for this purpose.

If the original packaging is unfit for use or is not available, repackage the instrument as follows:

1. Obtain a corrugated cardboard shipping carton having inside dimensions at least six inches greater than the instrument dimensions and having a carton test strength of at least 350 pounds per square inch (24.5 kg per square centimeter).

2. If the instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag to the instrument showing the following: the name of a person at your firm who can be contacted, complete instrument type and serial number, and a description of the service required.

3. Wrap the instrument with polyethylene sheeting or equivalent to protect the outside finish and prevent entry of packing materials into the instrument.

4. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing three inches on each side.

5. Seal the carton with shipping tape or with an industrial stapler.

6. Mark the address of the Tektronix Service Center and your return address on the carton in one or more prominent locations.

CONTROLS, CONNECTORS, AND INDICATORS

INTRODUCTION

The following descriptions are intended to familiarize the operator with the location and functions of the instrument's controls, connectors, and indicators. Detailed descriptions provide the user with the limitations of certain of the features with regard to sweep speeds, display modes, and other conditions that affect the control's operation.

POWER, CRT, AND DELAY TIME/CURSOR POSITION CONTROLS

Refer to Figure 2-2 for the location of items 1 through 5.

(1) **POWER Switch**—Turns the instrument power on and off. Push in once to apply power to the instrument; push in again to release the switch and remove power from the instrument. When power is applied a power-up routine automatically runs for approximately five seconds or less. At the end of that time, if no faults are located, the instrument enters the normal operating mode. Instruments with the battery backup that is included with Option 01, will power-up in the same operating mode present at power-down (excluding diagnostics). The standard instrument, will power-up with the following default settings:

DISPLAY MODE	NONSTORE
VERT MODE	CH 1
CH 1 VOLTS/DIV	50 mV
CH 2 VOLTS/DIV	50 mV
CH 2 INVERT	Off
A SEC/DIV	2 ms
TRIGGER MODE	AUTO
TRIGGER SOURCE	CH 1
TRIGGER COUPLING	AC

(2) **INTENSITY Control**—Determines the brightness of the crt NON STORE waveform displays only. Screwdriver controls accessed through the bottom of the cabinet are provided for the readout and stored waveform displays (both STORE and VIEW). See Figure 2-11 for the location of the bottom panel controls.

(3) **FOCUS Control**—Used to adjust for optimum display definition.

(4) **DLY TIME/CURSOR Position Controls**—Set the delay time for the B DLY'D Sweeps or position the cursors (one at a time) for making time and voltage measurements on the display STORE and VIEW waveforms. When setting time delay, the left push button decreases delay time, and the right push button increases it. The amount of delay is displayed in the crt readout. Pressing both the DLY TIME/CURSOR buttons at the same time zeros the delay time readout at the current delay setting.

Cursor measurements can only be made on the STORE or the VIEW wave-form displays. Menu selection is required to obtain the CURSORS Mode and also to select which of the cursor dots will be positioned by the DLY TIME/CURSOR position controls. The left push button positions the active cursor to the left, and the right push button positions it to the right. Activating the second cursor for positioning is done by pressing MENU button "1". Each press of the "1" MENU button alternately activates the cursors.

The active cursor will move incrementally with each push of one of the DLY TIME/CURSOR buttons. Continuing to hold the button down will cause the cursor to start fast positioning movement in the selected direction. When X10 MAG is on, the intensified cursor dots move approximately one-tenth slower so the apparent positioning rate of the dot remains the same between X10 MAG on and X10 MAG off. The rate at which a cursor is positioned is also a function of the microprocessor operations in progress. Complex operations such as AVERAGE and PROCESS may slow down cursor positioning. Pressing both the DLY TIME/CURSOR buttons at the same time, positions the two cursor dots to the center of the digitized waveform and zeros the ΔV and Δt readouts.

The cursor measurement results are displayed at the bottom of the crt with the CH 1 ΔV measurement first, followed by CH 2 ΔV (if CH 2 is displayed), then the Δt measurement. If ADD VERT MODE is selected, the ΔV readout for VIEW waveforms is in divisions rather than in volts. The CURSORS Mode menu remains displayed even if all the traces are removed from the crt, to remind the user that the CURSORS Mode is on.

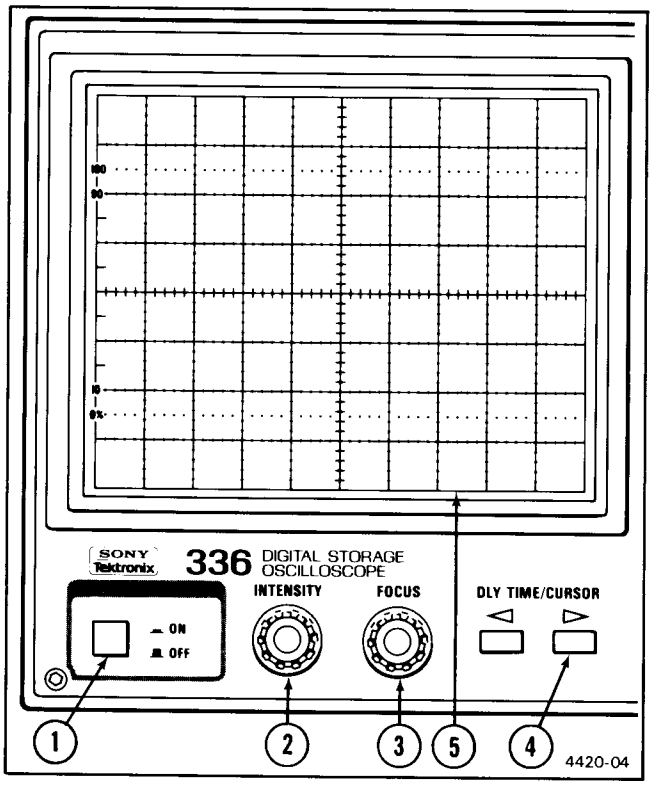


Figure 2-2. Power, CRT, and DLY TIME/CURSOR controls.

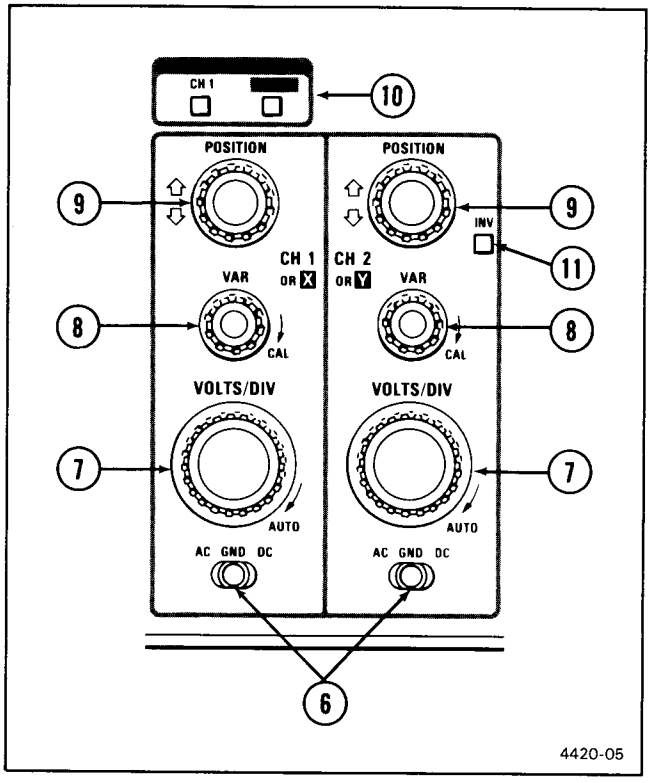


Figure 2-3. Vertical controls.

Exiting the CURSORS Mode is done by pressing the MENU "2" button. At that point the CURSORS Mode is off, but it will be reentered again if the MENU LAST push button is pressed to recall the CURSORS Menu. If another Main MENU selection is made after turning the cursors off, pressing the LAST button returns it rather than the CURSORS Menu.

(5) **Internal Graticule**—Eliminates parallax viewing errors. Rise time and amplitude measurement points are indicated at the left edge of the graticule.

VERTICAL CONTROLS

Refer to Figure 2-3 for the location of items 6 through 11.

(6) **AC-GND-DC Input Coupling Switches**—Select the method of coupling the input signal to the vertical deflection system. Switch positioning is read by the microprocessor, and the processor then controls magnetic reed switches to obtain the selected input coupling.

AC Position. Signals are capacitively coupled to the vertical input amplifier. The dc component of the input signal is blocked.

DC Position. All frequency components of the input signal are passed to the vertical input amplifier.

GND Position. The input to the vertical amplifier is grounded to provide a ground reference. In the GND position, the ac input coupling capacitor is allowed to precharge to the input signal dc level to prevent a sudden trace shift when switching from GND to AC input coupling. The GND position is used in the STORE Mode to acquire a ground reference level for use with the Storage PROCESS Menu selection. The ground reference is required for making the waveform calculations on the STORE or VIEW waveform displays. When STORE waveforms are entered into the 336 memory, the ground position is also stored and used for processing the VIEW waveforms.

(7) **VOLTS/DIV Switches**—Select the vertical deflection factor for Channel 1 and Channel 2 from 5 mV per division to 10 V per division in a 1-2-5 sequence of 11 steps. The VAR control must be in the calibrated detent position to obtain a calibrated deflection factor. The deflection factor selected is displayed in the crt readout. Probe coding is automatically adjusted for in the readout scale factor. The VOLTS/DIV switch position is read by the microprocessor, and the processor selects the proper attenuation by the use of magnetic reed switches.

In the STORE Mode, AUTO position (one step clockwise from the 5 mV per division setting) of the VOLTS/DIV position enables autoranging on the applied input signal. A colon (:) in front of the VOLTS/DIV readout indicates that autoranging is in effect. At the completion of autoranging, the signal will be displayed with between three to seven divisions of amplitude (the approximate switching points). Autoranging remains in effect until the VOLTS/DIV switch position is changed, and any signal amplitude change that crosses the autoranging switching points will switch the VOLTS/DIV readout to a new setting. The VOLTS/DIV readout at the end of autoranging is the new switch setting. Physically positioning the VOLTS/DIV switch exits the autoranging function.

NOTE

If either external or LINE Trigger SOURCE is selected, horizontal autoranging does not function. The SEC/DIV switch must, therefore, be manually set to the correct sweep speed. If the SEC/DIV switch is not set to the correct sweep speed, vertical autoranging may not be able to stabilize on one VOLTS/DIV setting.

(8) **VAR Controls**—Provide variable uncalibrated deflection factors between the calibrated settings of the VOLTS/DIV switches. Full clockwise rotation of the VAR knob places the control in the calibrated detent; full counterclockwise rotation of the VAR knob increases the vertical deflection factor to at least 2.5 times the indicated VOLTS/DIV setting. With the VAR control out of the calibrated detent, an uncal symbol (>) is displayed in front of the VOLTS/DIV readout for that channel; and cursor voltage measurements will produce a crt readout given in divisions rather than voltage units.

(9) **POSITION Controls**—Control the vertical position of the STORE and NON STORE displays on the crt. In the X-Y Mode, the Channel 2 POSITION control adjusts the vertical position of the display, and the Channel 1 POSITION control adjusts the horizontal position of the display. VIEW waveforms are not vertically positionable after storing, but the STORE waveforms respond to change in the vertical POSITION controls with each update of the display data. The vertical position of the STORE waveform is stored when ENTER is pressed, and that is the vertical position of the corresponding VIEW waveform when it is displayed.

(10) **VERT MODE Switches (CH 1 and MENU)**—Select the vertical mode used to display the input signals. The oscilloscope selects Channel 1 for display or storage when the CH 1 push button is pressed. Choosing other vertical modes is done by using the VERT MODE MENU. Using the menu, the user has a choice of CH 2, ADD, and TRIG VIEW (for external trigger only) VERT MODE or either CHOP or DUAL TRACE VERT MODE for two-channel displays (see Figure 2-4). When TRIG VIEW VERT MODE is selected, the CH 1 and CH 2 traces are displayed with the TRIG VIEW trace. Both ADD and TRIG VIEW VERT MODE disable the STORE Display Mode.

CH 1—Selects the Channel 1 input signal for display or storage when pressed. Menu selection is not required to obtain the Channel 1 VERT MODE. When selected, an LED is turned on to light the clear plastic CH 1 push button. Channel 1 only is deselected and the menu choices are displayed when the VERT MODE MENU push button is pressed.

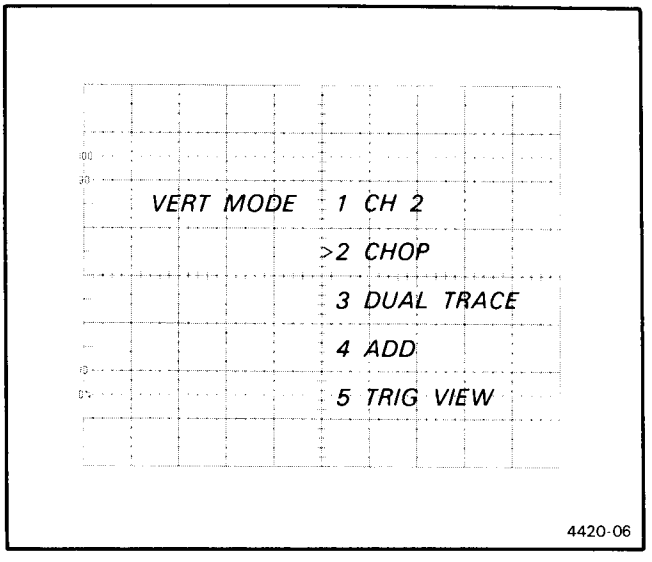


Figure 2-4. VERT MODE Menu with CHOP Mode selected.

MENU—Selects the VERT MODE MENU for display on the crt and turns off the CH 1 LED. VERT MODE selection is then made by pressing the numbered keys indicated by the menu display before the menu times out. When a VERT MODE MENU selection is the current operating mode, the MENU push button is lighted.

1 CH 2. Selects the Channel 2 input signal for display for NON STORE, STORE, and VIEW displays modes.

2 CHOP. Displays Channel 1 and Channel 2 input signals and selects the CHOP Mode for switching between the displayed traces. The chopping frequency is approximately 150 kHz at all SEC/DIV settings.

3 DUAL TRACE. Displays Channel 1 and Channel 2 input signals and switches between the vertical channel displays either in the CHOP Mode or Alternate Mode, depending on the SEC/DIV setting. Alternate switching between the traces occurs during holdoff time at the end of each sweep for sweep speed settings faster than 1 ms per division. With sweep speeds settings of 1 ms per division and slower, the NON STORE displays are switched between channels at the CHOP rate.

In NORM and AVERAGE STORE MODE, the digital storage memory acquires the Channel 1 and Channel 2 input signals interleaved, each with 1024-sample (10-bit) resolution. In ENVELOPE MODE, Channel 1 and Channel 2 input signals are acquired alternately with 512-sample (8-bit) resolution for the MIN and MAX envelopes of each waveform. STORE and VIEW waveform traces are alternately displayed at all sweep speeds.

4 ADD. Selects the algebraic sum of the Channel 1 and Channel 2 input signals to be displayed in NON STORE. The NON STORE ADD display cannot be stored. A digital add mode for STORE and VIEW displays is available by using the CH 1 + CH 2 and CH 1 − CH 2 waveform PROCESS Menu selections. VIEW waveforms may be displayed with the NON STORE ADD trace. STORE Mode is not enabled when ADD VERT MODE is being displayed, and if it is on when ADD VERT MODE is selected, the STORE Mode will be turned off.

5 TRIG VIEW. Selects the signal applied to the EXT TRIG IN connector for display if either EXT or EXT/10 TRIG SOURCE is also selected. The Channel 1 and Channel 2 traces are displayed with the external trigger signal. STORE Mode is not enabled when the trigger view signal is being displayed, but the VIEW waveforms may be displayed along with the NON STORE traces when TRIG VIEW VERT MODE is selected.

(11) **CH 2 INV Switch**—Inverts the Channel 2 display when pressed. Each press of the INV button toggles the polarity of the displayed Channel 2 waveform. When inverted, a down-arrow symbol appears in front of the Channel 2 VOLTS/DIV readout.

The invert feature may be used to convert sync-positive video signals to the correct polarity for application to the TV Sync Separator circuitry.

HORIZONTAL CONTROLS

Refer to Figure 2-5 for the location of items 12 through 15.

(12) **VAR SWP/HOLDOFF Control**—Either sets variable A Sweep speed or variable holdoff time for the A Sweep. The function is determined by the operator using the SCOPE Menu choices. Full clockwise rotation of the knob is the CAL position for variable sweep and the NORM position for variable holdoff. In its VAR SWP mode, the control affects the time base of the NON STORE A Sweep and the STORE

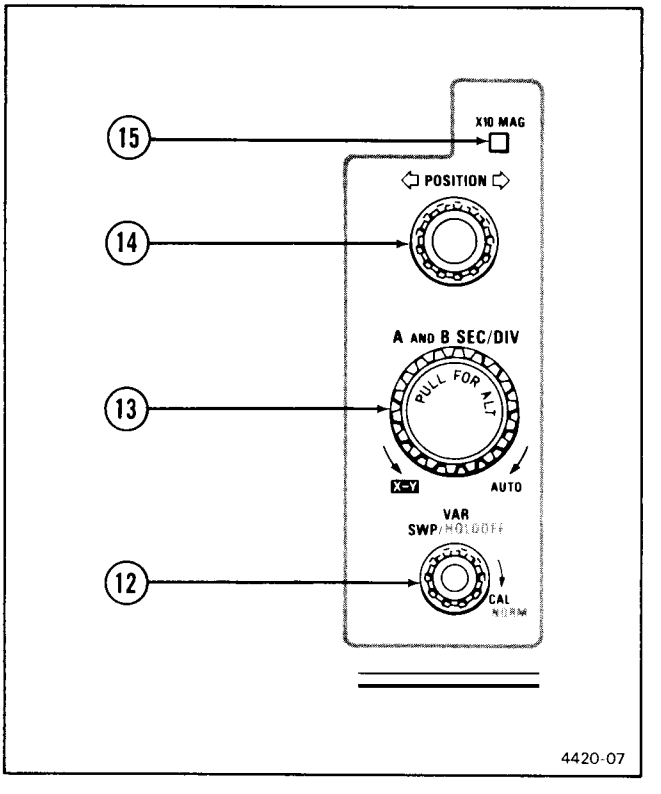


Figure 2-5. SEC/DIV and Horizontal controls.

Mode equivalent-time sampling A Sweep speeds. However, for real-time storage sweep speeds and ROLL Mode acquisitions, the VAR SWP control does not change the time base from that set by the SEC/DIV switch. When the VAR SWP control is out of the CAL detent, and varying the A Sweep speed, the crt delay-time and cursor delta-time measurement readouts will be in divisions rather than in time units. An uncalibrated A Sweep is also indicated by a greater-than symbol (>) displayed in front of the A SEC/DIV readout.

When the control is used in its VAR HOLDOFF mode, it can be used to increase the A Sweep holdoff (NON STORE sweeps only) by at least 10 times the NORM holdoff time. Storage holdoff times are a function of the microprocessor operation.

(13) **A and B SEC/DIV Switch**—Selects the calibrated sweep rates for both the A and the B Sweeps and controls the Horizontal Display Mode.

A Sweep. With the A SEC/DIV and B SEC/DIV set to the same sweep speed, and the knob pushed in, the switch selects A Sweep rates from 0.2 s per division to 0.1 μs per division in a 1-2-5 sequence of 20 steps. Full counterclockwise rotation to the end of the sweep speed settings selects the NON STORE X-Y Display Mode. Sweep speed settings of 0.5 s per division to 20 s per division, automatically place the instrument in the ROLL Storage Mode for data acquisition and display.

In the NORMAL STORE Mode, the AUTO position of the SEC/DIV switch (clockwise rotation of the switch until a colon symbol appears in front of the SEC/DIV readout) enables horizontal autoranging on the applied input signal (if the signal amplitude is greater than 0.5 vertical division and the oscilloscope is properly triggered). At the completion of autoranging, 1.5 to 4 cycles of the signal will be displayed across the full ten graticule divisions. The SEC/DIV readout at the end of autoranging is the new SEC/DIV switch setting. Autoranging remains in effect until the SEC/DIV switch is physically positioned. SEC/DIV autoranging does not take place if an external or LINE Trigger SOURCE is selected.

Aliasing can produce an incorrect autoranging result. A check of the NON STORE display will quickly confirm whether the horizontal autoranging resulted in the correct SEC/DIV setting. In any storage mode, except ROLL, changing the SEC/DIV switch setting causes the SEC/DIV readout to blink until the STORE display is updated to reflect the new switch setting.

ALTERNATE Sweep. Pulling the A and B SEC/DIV knob to the out position displays the NON STORE A Intensified Sweep alternated with the B Delayed Sweep and enables the switch to set the B Sweep rates. Calibrated B Sweep rates are from 50 ms per division to 0.1 μs per division in a 1-2-5 sequence of 18 steps. In ALT Horizontal Display Mode, the menu-selectable TRACE SEP feature can be used to separate the NON STORE A Intensified Sweep from the B Delayed Sweep vertically by up to two divisions in half-division steps. In ALT, the STORE Mode display is not enabled, and if on prior to entering ALT, it will be turned off.

Delay time for the B Delayed Sweep is set using the DLY TIME/CURSOR position push buttons. If the B Trigger is set for RUNS AFTER DELAY, the delay time position is continuously variable, and the waveform displayed on the B Delayed trace will move smoothly across the graticule area as the delay time is varied. When the B Trigger MODE is set to Triggerable After Delay (out of the RUNS AFTER DELAY detent position), the display will jump from trigger point to trigger point, and the waveform on the B Delayed trace will appear to remain stationary if it is repetitive.

B DELAYED SWEEP. Pushing the A and B SEC/DIV knob in, with the B Sweep speed set to a faster rate than the A Sweep speed, changes the Horizontal Display Mode to the B DLY'D trace only. The B Sweep speed cannot be set slower than the A Sweep speed. Rotating the switch back to the A SEC/DIV setting established prior to entering the B DLY'D Sweep display returns the horizontal display back to the A Sweep Display Mode.

NOTE

When the SEC/DIV knob is pulled to the out position to enter ALT Horizontal Display Mode, the B SEC/DIV readout is the same as the A SEC/DIV readout unless the A SEC/DIV switch setting is at either 0.2 s or 0.1 s per division. At either 0.2 s or 0.1 s per division A Sweep speed, pulling the SEC/DIV knob to the out position displays the B Sweep speed at the slowest B Sweep speed available (50 ms per division). Firmware version 4.4 does not recognize that the A and B Sweep speeds are automatically set to different SEC/DIV settings, and the microprocessor continues to respond to SEC/DIV switch changes just as at the faster sweep speeds. The effects of this for the operator are the following:

1. Even though the B Sweep speed is set faster than the 0.2 s or 0.1 s per division A Sweep speed, pushing in the SEC/DIV knob will not switch the Horizontal Display Mode to B Delayed until the SEC/DIV knob is rotated at least one position clockwise after entering the ALT Horizontal Display Mode.

2. When the X10 MAG feature is used, the B SEC/DIV readout is switched incorrectly until the SEC/DIV knob is rotated at least two positions clockwise from the 0.2 s A SEC/DIV switch setting or at least one position clockwise from 0.1 s A SEC/DIV switch setting. The slowest magnified B Sweep speed is 5 ms per division even though the B SEC/DIV readout may be indicating either 20 ms or 10 ms per division.

(14) **Horizontal POSITION Control**—Positions the waveform displays (STORE, VIEW, and NON STORE) horizontally, except the NON STORE X-Y display. The menu displays and crt readouts are not positionable with any front-panel control.

(15) **X10 MAG Switch**—Increases the display sweep speeds by a factor of 10 when pressed in. Extends the fastest sweep speed to 10 ns per division. The push button must be pressed in a second time to regain the X1 sweep speeds. The clear plastic X10 MAG button is lighted by a red LED when magnification is in effect, and the crt SEC/DIV readout switches to indicate the correct display sweep speed. X10 MAG is not enabled for NON STORE X-Y Display Mode, but it will horizontally magnify the STORE and VIEW X-Y displays.

TRIGGER CONTROLS

Refer to Figure 2-6 for location of items 16 through 20.

(16) **B TRIG LEVEL and SLOPE Control**—Sets the level at which the B Sweep can be triggered and determines on which slope of the trigger signal that triggering occurs. Counterclockwise rotation of the knob past the midpoint places the B TRIG LEVEL control in the positive slope region; clockwise rotation past the midpoint places it in the negative slope region. In addition, the B TRIG LEVEL control switches the B Trigger MODE between Triggerable After Delay and RUNS AFTER DELAY. Full ccw rotation of the knob into the detent selects the RUNS AFTER DELAY B Trigger Mode. In this mode the B Sweep is initiated immediately after the delay time set by the DLY TIME/CURSOR position push buttons. At any other position of the B TRIG LEVEL control, the B Sweep is in the Triggerable After Delay Mode, and the B Sweep is not initiated until a trigger signal is received following the delay time.

NOTE

The A Sweep must be running (either free running or triggered) to obtain a B Sweep display.

(17) **A TRIG LEVEL and SLOPE Control**—Sets the level at which the A Sweep can be triggered and determines on which slope of the trigger signal that triggering occurs. Counterclockwise rotation of the knob past the midpoint places the A TRIG LEVEL control in the positive slope region; clockwise rotation past the midpoint places it in the negative slope region. The LEVEL control range is limited to the trigger signal peak-to-peak amplitude when AUTO Trigger Mode is selected.

(18) **Trigger COUPLING Switches (AC and MENU)**—Select the method of coupling the trigger signal to the input of the trigger circuitry. AC COUPLING is obtained using the AC push button. Use of the AC COUPLING in conjunction with the CH 1 VERT MODE and CH 1 SOURCE switches allows the oscilloscope operator to obtain a quick, single-channel display without making menu selections. The remaining COUPLING choices are selected under MENU control. The selected push button is lighted by an LED to indicate the activated mode.

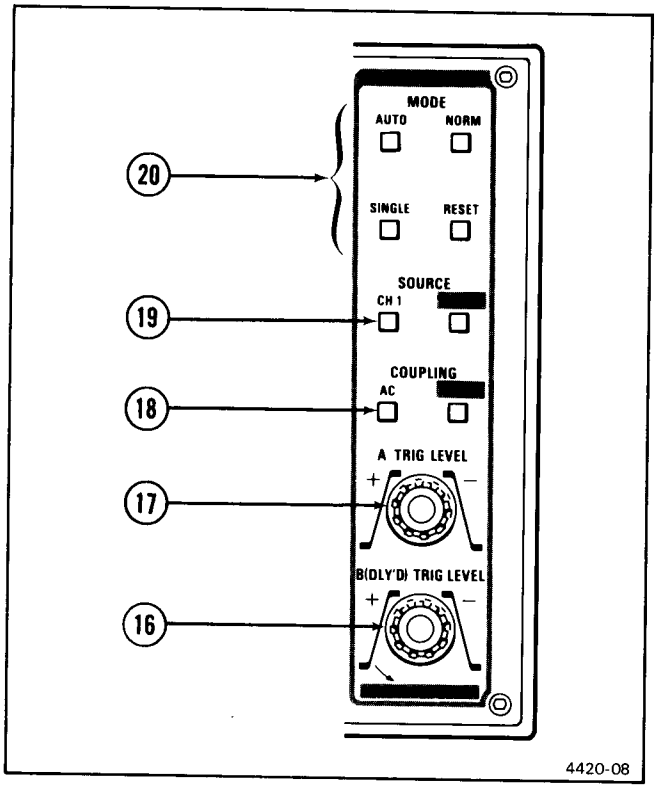


Figure 2-6. Trigger controls.

AC COUPLING. Signals are capacitively coupled to the input of the trigger circuit. The dc component is rejected, and signal components below about 30 Hz are attenuated. Triggering is allowed only on the ac portion of the applied trigger signal.

MENU. Selects the COUPLING Menu for display on the crt (see Figure 2-7). Trigger COUPLING selections are then made using the numbered keys associated with the choices displayed before the menu times out.

1 DC. All frequency components of a trigger signal are passed to the input of the trigger circuit. This coupling method is useful for providing a stable display of low-frequency or low-repetitive rate signals.

2 HF REJ. Signals are capacitively coupled to the input of the trigger circuit. The dc component is rejected, and signal components below about 30 Hz and above 50 kHz are attenuated. HF REJ COUPLING is useful for providing a stable display of the low-frequency components of a complex waveform and rejecting high-frequency interference from the trigger signal.

3 LF REJ. Signals are capacitively coupled to the input of the trigger circuit. The dc component is rejected, and signal components below about 50 kHz are attenuated. LF REJ COUPLING is useful for providing a stable display of the high-frequency components of a complex waveform and rejecting low-frequency interference or power-supply hum from the trigger signal.

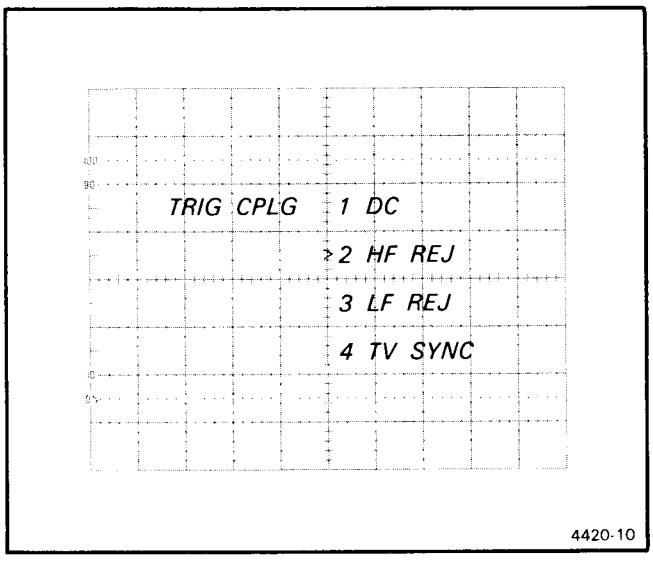


Figure 2-7. Trigger COUPLING Menu with HF REJ selected.

4 TV SYNC. Television signals applied to the TV Sync Separator circuit are processed to produce stable triggering on composite-video or composite-sync television signals. Video components of the trigger signal are rejected. The Sync Separator provides either vertical-sync or composite-sync pulses to trigger the A Sweep circuit; the B Sweep circuit is provided with composite-sync pulses only for triggering the B Sweeps.

Selection of the trigger signal to the A Sweep circuit is automatically determined by the A Sweep speed setting: vertical sync is used for A Sweep speeds slower than 0.1 ms per division; composite sync is used for A Sweep speeds of 0.1 ms per division and faster.

Sync-negative signals are required by the TV Sync Separator circuit for proper operation; however, sync-positive composite video or composite sync can be separated by applying the trigger signal to the CH 2 input connector and using the CH 2 INV feature to obtain the correct signal polarity. CH 2 SOURCE must also be selected, using the Trigger SOURCE Menu, for the TV Sync Separator to be operated in the manner just described.

(19) **Trigger SOURCE Switches (AC and MENU)**—Select the source of the trigger signal applied to both the A Trigger and the B Trigger circuitry. Channel 1 SOURCE is obtained by using the CH 1 push button. The remaining Trigger SOURCE choices are made under MENU control. The selected push button is lighted by an LED to indicate the activated button.

CH 1 SOURCE. Selects the Channel 1 input signal as the source of the triggering signal. When used in conjunction with the CH 1 VERT MODE and AC Trigger COUPLING switches, a quick, single-channel display may be quickly obtained without making any menu selections.

MENU. Selects the Trigger SOURCE Menu for display on the crt (see Figure 2-8). SOURCE selections are then made using the numbered keys associated with the choices displayed before the menu times out.

1 CH 2. Selects the Channel 2 input signal as the source of the triggering signal for both the A Sweep the B Sweep.

2 EXT. Selects the signal applied to the EXT TRIG IN connector (located on the instrument right side panel) as the source of the triggering signal. A display of the external trigger signal can be obtained by selecting TRIG VIEW from

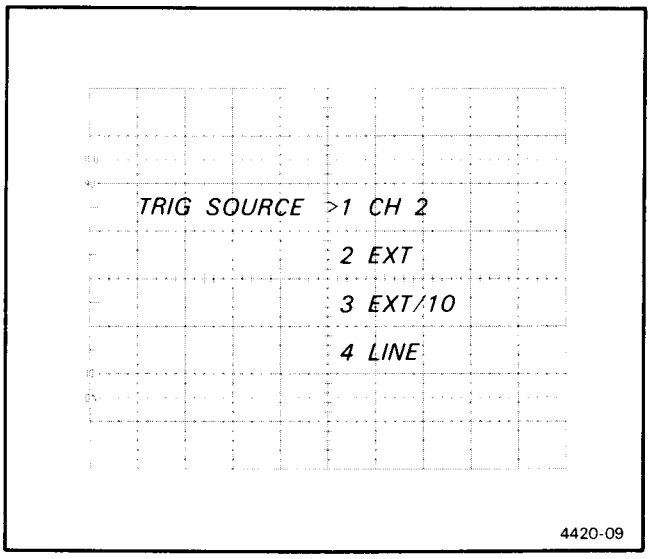


Figure 2-8. Trigger SOURCE Menu with CH 2 selected.

the VERT MODE Menu when either EXT or EXT/10 is selected as the Trigger SOURCE. The external trigger display is obtained in the NON STORE Mode only and is displayed along with the Channel 1 and Channel 2 traces.

3 EXT/10. Selects the signal applied to the EXT TRIG IN connector as the external trigger signal and attenuates it by a factor of 10 times. This allows the use of higher amplitude signals as the triggering source while maintaining an acceptable signal amplitude to the trigger circuitry.

4 LINE. Selects the ac power-source waveform as the source of the triggering signal. LINE SOURCE is useful when the displayed waveform frequency is a multiple or a submultiple of the ac power-source frequency. LINE is also useful for obtaining a stable display of a power-source frequency component in a complex waveform.

(20) **Trigger MODE Switches**—Select the mode of triggering of the A Sweep. When either AUTO or NORM Trigger MODE is selected, the associated push button is lighted. If SINGLE is the selected Trigger MODE, the associated button is lighted, and the RESET button is also lighted if the single sweep is armed (waiting for a trigger signal). As soon as the single sweep is triggered, the RESET button LED is turned off, and it remains off until the single sweep is rearmed by pressing the RESET button.

AUTO Mode. Automatically sets the A Trigger LEVEL control range to within the peak-to-peak amplitude of the applied trigger signal. In the absence of an adequate trigger signal (too small an amplitude, too slow a repetition rate, or an incorrect SOURCE chosen), the A Sweep freeruns to provide the operator with a trace for positioning the display and determining if any vertical input signal is present. AUTO is the MODE most frequently selected, as it provides stable triggering on the majority of signals to be displayed with the least amount of operator adjustment.

NORM Mode. Produces a NON STORE sweep or acquires data for storage when properly triggered. An adequate trigger signal must be present, and the Trigger LEVEL control must be set to within the correct range for the trigger signal applied. In the absence of an adequate trigger signal, a sweep is not initiated. The NORM Mode is useful for obtaining a stable display of low-frequency or low-repetition rate signals.

SINGLE Mode. Sweep is initiated one time (or one time window of waveform data is stored) when an adequate trigger signal is applied and the Trigger LEVEL control is properly set. The sweep cannot be triggered again until the sweep logic circuitry is rearmed by pressing the RESET push button. A STORE waveform obtained in the SINGLE acquisition mode can be continually displayed on the crt for analyzing the pulse or making time and voltage measurements. For STORE Mode acquisitions, SINGLE Trigger MODE is not enabled for the equivalent-time sampling sweep speeds (50 μs per divisions and faster). When ENVELOPE Storage Mode is in use, two sweeps are required to obtain a display update.

NOTE

If STORE Mode is turned on in the equivalent-time sampling region while attempting to obtain single-sweep NON STORE displays, Channel 1 and Channel 2 are displayed on alternate single sweeps. To return to normal SINGLE sweep operation of a single channel only, turn off the STORE Mode and press the AUTO Trigger MODE button, then press the SINGLE button to return to single-sweep triggering.

RESET Switch. Resets the sweep logic circuitry to be able to respond to the next adequate trigger signal received. The RESET button must be pressed once for each sweep displayed or acquired in the SINGLE Trigger MODE. While waiting for a trigger signal to occurs, the RESET button is lighted to indicate that the trigger circuitry is rearmed. When the single sweep is triggered, the RESET button LED is turned off.

NOTE

The armed condition of RESET is not retained by the Option 01 instrument when power is removed. However, when power is reapplied the RESET LED remains lighted at all times (SINGLE operation is not affected). To clear this condition, press the AUTO Trigger MODE button.

DISPLAY MODE, MEMORY, AND MAIN MENU CONTROLS

Refer to Figure 2-9 for location of items 21 through 23.

(21) **DISPLAY MODE Switches**—Select the NON STORE and STORE Modes of operation and determine the waveforms displayed. The following combinations of displays are available:

NON STORE waveforms only,

STORE waveforms only (not available with ADD and TRIG VIEW VERT MODE or ALT Horizontal Display Mode),

VIEW waveforms only (recalled from the VIEW memory stack),

NON STORE and STORE waveforms together (not available with ADD and TRIG VIEW VERT MODE or ALT Horizontal Display Mode),

NON STORE and VIEW waveforms (recalled from the stack memory).

STORE and VIEW waveforms together when the VERT MODE is CH 1 only (not available with ALT Horizontal Display Mode).

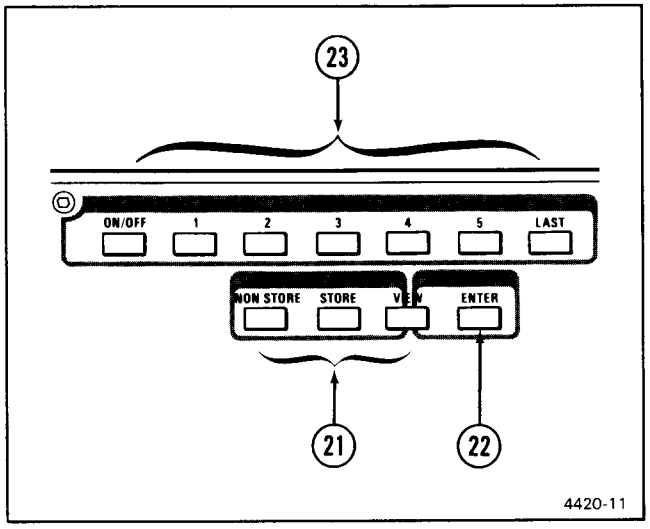


Figure 2-9. DISPLAY MODE and MENU controls.

NON STORE. NON STORE waveforms are displayed on the crt, and the instrument functions in a manner similar to a conventional oscilloscope.

NOTE

If FAST START, SLOW START, or CAL of the CHART Menu are selected while NON STORE and VIEW traces are on, the NON STORE displays will be turned off. NON STORE will be turned on again by any of the following actions:

1. *Pressing the STOP button (MENU 4).*
2. *Pressing either the MENU ON/OFF or MENU LAST button.*
3. *Pressing VIEW Display Mode button to turn off the VIEW display.*
4. *Entering ROLL Storage Mode to turn off the VIEW display.*

STORE. Channel 1 and Channel 2 input signals are digitized and stored. Stored waveforms are displayed on the crt as determined by the VERT MODE selected (CH 1 only, CH 2 only, or both). Updating of the displayed waveform(s) is continual when the instrument is properly triggered. When not triggered, the STORE waveform display remains as initially acquired. If ALT Horizontal Display Mode is selected when STORE Mode is in effect, the STORE Mode is turned off. STORE Mode will be turned on again when the display mode is switched to either A only or B only. If the VERT MODE is either ADD or TRIG VIEW, the STORE Mode is not selectable, but VIEW waveforms may be displayed together with the NON STORE ADD or TRIG VIEW displays.

(22) **MEMORY Controls**—Control the storing of waveforms in the VIEW memory stack and recalling of the waveforms for display.

VIEW Switch. Controls the display of waveforms stored in the VIEW memory stack. The first push of the VIEW button lights the VIEW button LED and brings up a VIEW waveform for display (providing a waveform is stored in the VIEW memory). If the extended memory of Option 01 is installed, a waveform must be stored in the currently selected VIEW waveform stack number for a waveform to be displayed when VIEW is pressed. If the STORE Mode is in effect, turning on VIEW Mode also turns off the STORE Mode, unless the VERT MODE is CH 1 only. In that case STORE and VIEW may be displayed together. A second push of the VIEW button turns off the VIEW Mode.

With the displayed VIEW waveform, the VIEW waveform readout information describing the VOLTS/DIV and SEC/DIV settings at which the waveform was acquired is also displayed. When the Option 01 extended memory is installed, the VIEW INCR-DECR Menu and waveform stack number are also displayed.

The INCR-DECR Menu is used to rotate through the VIEW memory stack (in either direction) to either bring up succeeding stored waveforms for display or position the stack to store a new waveform in the selected stack number (indicated by the stack number displayed on the crt). The INCR-DECR Menu times out similar to the VERT MODE, Trigger SOURCE, and Trigger COUPLING Menus, and is not recalled by the LAST MENU button. To return the menu to the display for stack positioning after it times out, press VIEW off then on again. While the INCR-DECR Menu is displayed, pressing the "1" MENU button increments the VIEW waveform stack number; pressing the "2" button decrements it. The Option 01 extended memory adds eight frames of storage space (up to 16 waveforms) to the standard instruments two-frame memory space for a total of nine frames of VIEW memory (18 waveforms total).

Pressing the VIEW button while ROLL Storage Mode is enabled, stops the ROLL acquisition and displays the VIEW waveform (if a VIEW waveform is present in either the currently selected stack number for Option 01 or in stack number W-1 for the standard instrument). If no waveform data is stored, only the stack number appears when the VIEW button is pressed. With Option 01 installed, the VIEW Display Mode INCR-DECR Menu also appears as well as the stack number. A second push of the VIEW button turns off the VIEW Display Mode and restarts the ROLL Mode acquisition.

Stored VIEW waveforms are not cleared from the VIEW waveform stack when called up for display. The extended memory of Option 01 is circular, and incrementing or decrementing through the stack returns it to the starting point.

NOTE

VIEW waveform stack number W-1 is used for storage during AVERAGE Storage Mode. Consequently, when averaging, data previously stored in that stack number is destroyed, leaving an empty memory at that location.

ENTER Switch. Enters digitized STORE Display Mode waveforms into the VIEW memory stack. Each push of the ENTER button stores the current contents of the display RAM into the VIEW memory (at the currently selected stack number of the Option 01 extended memory). The standard instrument memory stores one frame (two waveforms); the optional memory stack stores up to eight frames (16 waveforms), for a total of nine frames (18 waveforms). The Channel 1 and Channel 2 waveforms are both digitized and stored, even if only one is being displayed. The number of waveforms displayed (either one or two) upon recalling the stored waveforms for display, depends on the VERT MODE selection. Waveform data outside the dynamic digitizing range of the instrument when stored will not be visible when recalled.

When ENTER is pressed while ROLL Storage Mode is active, the digitized ROLL storage acquisitions are stored in the currently selected VIEW waveform stack (W-1 in the standard instrument), and the VIEW function is activated. Pressing the VIEW button to turn off the VIEW Display Mode reactivates the ROLL Storage Mode.

NOTE

When VIEW Mode is active, the ENTER pushbutton is disabled except in the case of using the PROCESS WFM Menu. Resulting waveforms from processing VIEW waveforms may be directly stored in the VIEW memory stack.

NOTE

A ground reference cannot be acquired in ROLL Mode. If PROCESS Menu calculations are to be performed on the ROLL Mode waveforms after it is stored in the VIEW memory, the previously acquired ground level references will be used; therefore, the correct ground reference must be acquired prior to entering the ROLL Mode.

(23) **MAIN MENU Switches**—Select the oscilloscope functions not selected by designated front-panel switches or menus. Entry into the Main MENU may be done using the MENU ON/OFF button or by using the MENU LAST button. Entering using the MENU ON/OFF button starts a menu display that is a list of additional menu choices requiring further selection to choose a desired function. Entering MENU operation using the LAST button, starts at the last Main MENU selection displayed, and further choices depend on point the Main MENU was exited (either by using the MENU ON/OFF button or by the menu timing out).

MENU ON/OFF. Starts the Main MENU display or stops any menu display, except CURSORS. When MENU ON/OFF is pressed to turn the menu display on, it starts with the initial choices available (see Table 2-2 for a list of the Main MENU selections).

Numbered MENU Buttons (1, 2, 3, 4, and 5). Select the desired MENU item from the choices displayed. The selection MENU button must be pressed while the menu is displayed for a choice to be effected. Only those numbered buttons that correspond to a choice in the menu are active. Pressing a numbered button not listed in the menu does nothing.

LAST. Used to reverse scroll through the Main MENU selections or to return to the last Main MENU being displayed either before a time out or before the MENU ON/OFF button was pressed to turn the menu display off. Pressing LAST does not return to any of the three front-panel control menus (VERT MODE, Trigger SOURCE, or Trigger COUPLING), or to the VIEW Mode INCR-DECR Menu, after those menu displays time out.

RIGHT SIDE PANEL CONNECTORS

Refer to Figure 2-10 for location of items 24 through 30.

(24) **CAL Output Connector**—Provides a 0.3 V peak-to-peak square-wave signal at a repetition rate of approximately 1 kHz. The Calibrator signal is useful for checking the vertical accuracy of the NON STORE and STORE waveforms, and for checking the approximate horizontal timing and probe condition.

(25) **CH 1 OR X and CH 2 OR Y Input Connectors**—Provide for application of external signals to the input of the vertical amplifiers. These connectors each include a coding-ring contact that activates the scale-factor-switching circuitry whenever a properly coded 10X probe is attached. The VOLTS/DIV crt readout therefore reflects the correct deflection factor for the signal displayed.

In the NON STORE X-Y Display Mode, the signal applied to the CH 1 OR X input connector provides the horizontal deflection, and the signal applied to the CH 2 OR Y input connector provides the vertical deflection.

(26) **EXT TRIG IN Connector**—Provides for external triggering of the oscilloscope. The external trigger signal is applied to the trigger generator circuitry whenever EXT or EXT/10 Trigger SOURCE is selected. When selected, the external trigger signal may be displayed on the crt by choosing the TRIG VIEW feature from the VERT MODE Menu. The external trigger signal is then displayed together with the Channel 1 and the Channel 2 input signals. The external trigger signal cannot be stored.

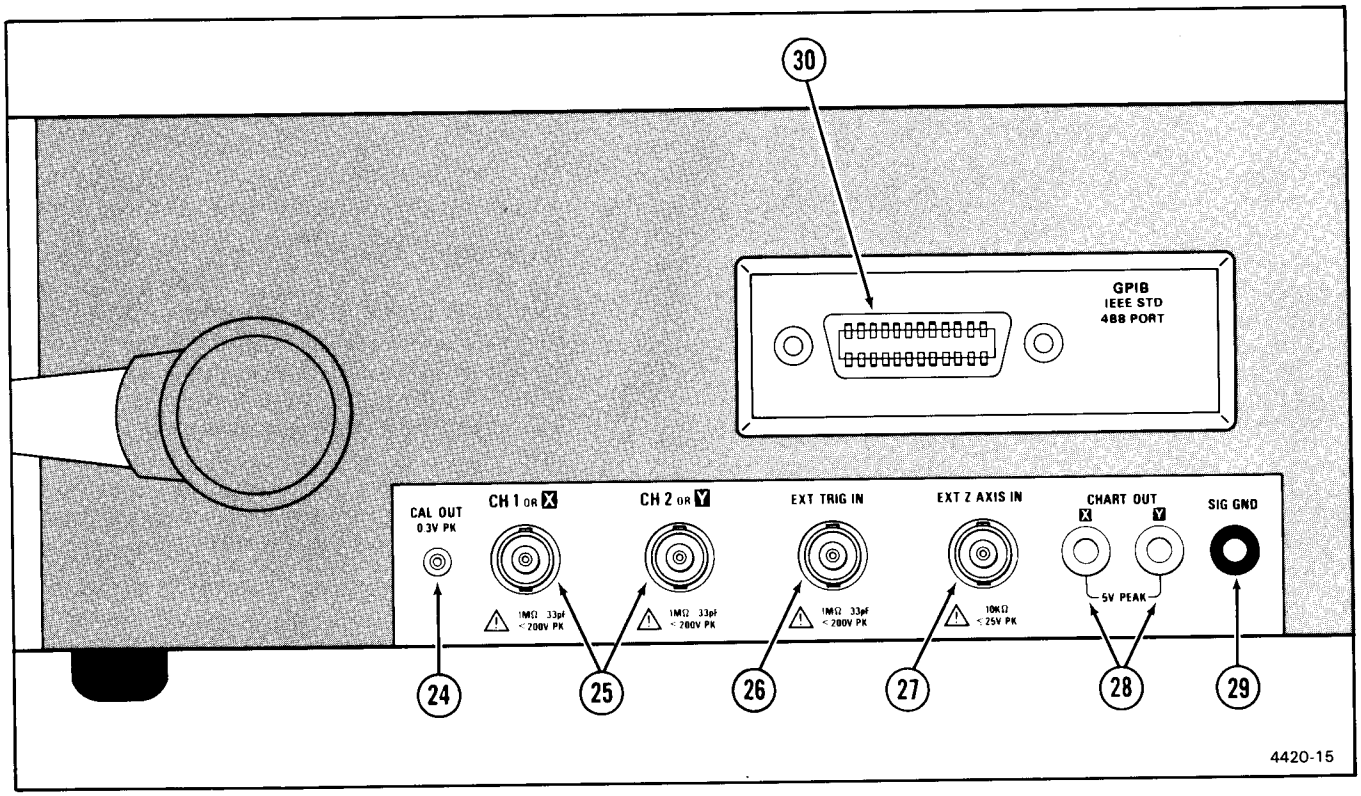


Figure 2-10. Right side panel connectors.

(27) **EXT Z-AXIS IN Connector**—Provides for external Z-Axis intensity modulation of the displayed waveforms. The useable frequency range of input signals is dc to 1 MHz. A 3 V peak-to-peak signal causes noticeable modulation at normal display intensity, and a positive signal decreases the intensity.

(28) **X and Y CHART OUT Connectors**—Provide analog X and Y output signals for use with an external X-Y Plotter. Output amplitude is about 500 mV per division with an output impedance of approximately 220 Ω. A choice of two clocking rates (FAST and SLOW) and the pen position calibration voltages are menu selectable. The CAL Menu selection provides two voltage levels (corresponding to the lower left and upper right corners of the graticule area) for calibrating the X-Y Plotter deflection to the 336 graticule before plotting a waveform. After calibrating the X-Y Plotter, pressing the FAST START MENU button starts the waveform plot at the faster clocking rate; pressing SLOW START MENU button starts the waveform plot at the slower clocking rate. The data output rate is controlled automatically by the difference in preceding data.

(29) **SIG GROUND Connector**—Provides an auxiliary signal ground when interconnecting the 336 to equipment under test or to an external X-Y Plotter.

(30) **GPIB Connector (Option 01)**—Provides a data output port to an IEEE-488 data bus. The connector is a standard 24-pin GPIB connector, and the electrical and physical arrangement of the pins conforms to the IEEE-488 Standard of 1978 for General Purpose Interface Bus equipment.

BOTTOM PANEL CONTROLS

Refer to Figure 2-11 for location of items 31 through 33.

(31) **TRACE ROTATION Control**—Permits trace rotation adjustment to align the baseline trace with the horizontal graticule lines. It is a screwdriver adjustable control that, once adjusted, should not require frequent alignment under normal operation.

(32) **READOUT INTENSITY Control**—Permits the user to adjust crt readout intensity for optimum viewing. This control is also screwdriver adjustable.

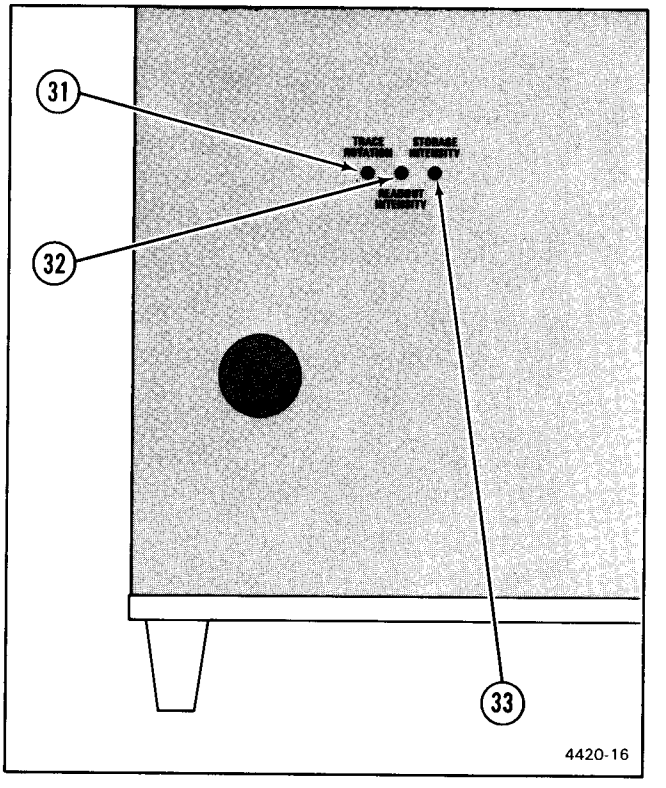


Figure 2-11. Bottom panel controls.

(33) **STORAGE INTENSITY Control**—Permits the user to adjust STORE and VIEW trace intensity for optimum viewing. It is also a screwdriver adjustable control.

REAR PANEL

Refer to Figure 2-12 for items 34 through 36.

(34) **Fuse Holder**—Contains the instrument's primary power fuse.

(35) **Power Cord Receptacle**—Provides the connection point for the ac power source to the instrument. The power cord safety-ground connection is connected to the exposed metal parts of the instrument. The power cord must be connected to a properly grounded power source for electrical-shock protection.

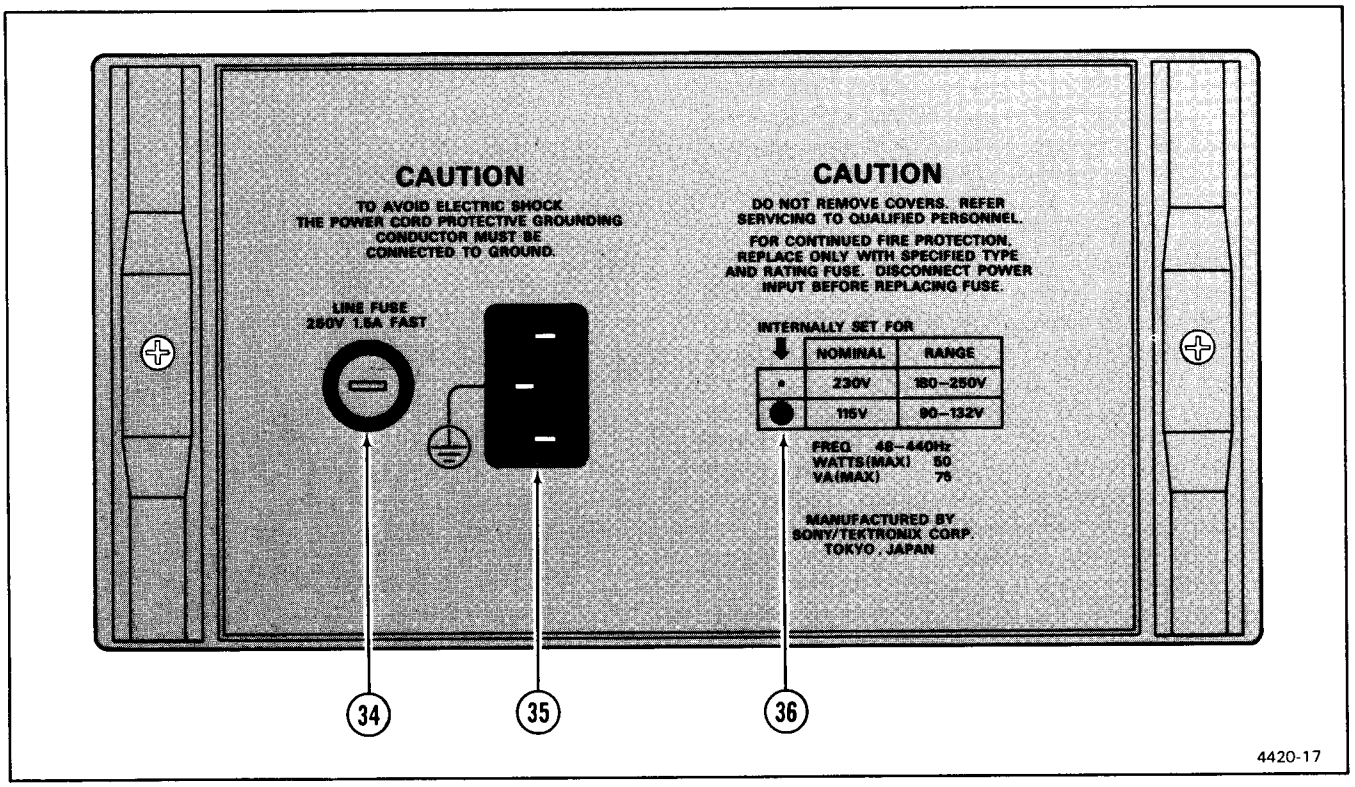


Figure 2-12. Rear panel.

(36) **Line Voltage Selected Indicator**—Indicates the nominal ac power source from which the instrument is internally set to operate. The nominal voltages and ranges are indicated in the rear panel nomenclature.

MAIN MENU OPERATION

The following information details the use of the Main MENU in selecting the various features under its control and describes those features. Table 2-2 gives a brief outline of the MENU operation in tabular form as a quick reference guide. The Menu Diagram located in the front-cover, illustrates the exact menus that are available and the selection route.

STORAGE MENU—Displays the storage feature menu items of:

1 STORE MODE

2 ACQ WINDOW

3 DISPLAY

4 CURSOR

5 PROCESS

Each of these functions and associated sub-menus are explained here.

STORE MODE. Displays the menu of STORE MODE choices for acquiring and digitizing waveform data.

NORMAL Acquisition Mode. At sweep speed settings of 0.1 ms per division to 0.2 s per division, waveform data is acquired in a single sweep (real-time sampling). The useful storage bandwidth for real-time sampling is dc to 140 kHz. For sweep speed settings of 50 μs per division to 0.1 μs per division, equivalent-time sampling is used to acquire waveform data over multiple sweeps of repetitive signals. The useful storage bandwidth for equivalent-time sampling is dc to 50 MHz with a sample rate of up to 1 megasample per second. Vertical gain and acquisition rate of the waveforms are determined by the VOLTS/DIV and SEC/DIV switches respectively. Waveform data will be repetitively acquired and the display updated if the TRIG MODE is set to AUTO or NORM (and the instrument is triggered).

If the TRIG MODE is set to SINGLE, and the SEC/DIV setting is within the real-time sampling range (0.1 ms to 0.2 s per division), waveform data will be acquired for one sweep only when triggered, and the acquired waveform will remain displayed for analysis and measurements.

Table 2-2
336 Main MENU Selections

1 STORAGE			
First Sub-Menu	**Second Sub-Menu**	**Third Sub-Menu**	**Comments**
STORE MODE	NORM		
	ENVELOPE	INCR DECR RESTART	1, 8, 16, 32, 64, 128, 256, or continuous at SEC/DIV setting of 2 ms per division and slower.
	AVERAGE	INCR DECR	8, 16, 32, 64, 128, or 256 averages.
ACQ WINDOW	PRE TRIG MID TRIG POST TRIG		Real-time Storage Mode only. SEC/DIV settings from 0.2 s to 0.1 ms per division.
DISPLAY	TIME X-Y		STORE and VIEW Horizontal time base selection.
CURSORS	CURSOR SEL OFF		CURSORS Menu display does not reduce the STORE or VIEW display intensity.
PROCESS	WFM	CH 1 + CH 2 CH 1 − CH 2 CH 1 X CH 2	STORE or VIEW waveforms. Must acquire a ground reference level to obtain the correct calculation results. PROCESS Menus do not reduce the STORE or VIEW display intensity.
	PARAMETERS	RMS P-P MEAN	

2 DATA OUT			
First Sub-Menu	**Second Sub-Menu**	**Third Sub-Menu**	**Comments**
CHART	FAST START SLOW START CAL STOP		CHART function is valid for VIEW Display Mode waveforms only.
GPIB (Option)	INCR DECR TRANSMIT STOP		Sets Talk Address or Talk Only Mode.

3 SCOPE			
First Sub-Menu	**Second Sub-Menu**	**Third Sub-Menu**	**Comments**
SCOPE	HORIZ VAR	HOLDOFF SEC/DIV	Selects function of VAR SWP/HOLDOFF control.
	TRACE SEP	INCR DECR	Sets trace separation between A Sweep trace and alternate B Sweep trace in 0.5 division steps from zero to about two divisions.

Table 2-2 (cont)

4 CHARACTER			
First Sub-Menu	**Second Sub-Menu**	**Third Sub-Menu**	**Comments**
READOUT	ON OFF		
TIME OUT	FAST NORMAL SLOW		In about 1 second. In about 3 seconds. In about 15 seconds. CPU operation affects these times.
5 SETTINGS			
First Sub-Menu	**Second Sub-Menu**	**Third Sub-Menu**	**Comments**
NONE			Displays current settings of: VERT MODE, TRIG SOURCE, TRIG CPLG, ACQ MODE, ACQ WINDOW, DISPLAY, and HORIZ VAR. Does not time out. Settings display is automatically erased by any changes to the front-panel settings.

NOTE

In the equivalent-time sampling region, STORE Display Mode waveforms will not be updated when SINGLE Trigger MODE is selected, and the last acquired waveform will remain displayed. It is recommended that STORE Mode not be selected when using the SINGLE Trigger MODE for NON STORE displays.

ENVELOPE Acquisition Mode. The ENVELOPE acquisition mode is limited to a sweep speed range of 2 ms per division to 0.2 s per division. At faster sweep speeds the NORMAL acquisition mode remains in effect. In ENVELOPE Mode, waveform data is repetitively acquired for a selected number of acquisitions (two sweeps are required for each acquisition), during which time the envelope of the accumulated waveform is displayed. Differences between successively acquired waveforms are displayed as they occur. As the waveform acquisitions are being made, a countdown number is displayed in the lower right hand corner of the crt. The countdown number indicates the number of waveforms remaining to be accumulated in the envelope display and the rate of acquisition.

At the end of the selected number of acquisitions, the countdown number is replaced by the letters "ENV", and the final envelope waveform is held momentarily. Then, the accumulated display is cleared, and the acquisitions are restarted. The number of waveforms to be accumulated is selectable using the INCR and DECR MENU buttons to change to number indicated in the readout. A choice of 1, 8, 16, 32, 64, 128, and 256 waveforms may be accumulated before resetting, or the ENVELOPE may be set for continuous accumulation (infinity symbol is displayed in place of the countdown number). Each change of the number selected restarts the acquisitions at the new number. The ENVELOPE acquisitions in progress may also be stopped and restarted by pressing MENU button 3 (RESTART).

AVERAGE Acquisition Mode. Waveforms are acquired for a choice of 8, 16, 32, 64, 128, or 256 sweeps, and the averaged waveform is displayed. The INCR and DECR MENU buttons are used to select the number of waveforms to be averaged before the display is updated. As the waveforms are being acquired, a countdown number is displayed in the lower right hand corner of the crt. The countdown number indicates the number of waveforms remaining to be acquired for averaging and the acquisition rate. When the selected number of waveforms have been acquired, the letters "AVG" replaces the countdown number, and the display is updated to reflect the result of the last averaging cycle. AVERAGE acquisitions commence immediately upon selecting the AVERAGE Mode. Each change of the selected number of waveforms to be averaged, restarts the waveform acquisitions at the new number.

NOTE

VIEW waveform stack location W-1 is used during the AVERAGE Storage Mode for calculating the averaging results. Consequently, the VIEW waveform data stored in location W-1 is lost when AVERAGE Storage acquisitions are made.

ACQ WINDOW. A choice of trigger point in the waveform data is available for the STORE real-time acquisitions. This feature is not enabled for equivalent-time sampling.

1 PRE TRIG. Selects a trigger point that allows a display of waveform data occurring prior to the triggering event. Seven-eighths of a waveform are stored before the trigger point, and one-eighth is stored after the trigger point.

2 MID TRIG. Selects the center of the acquired waveform data as the trigger point. Allows a display of waveform data occurring equally on either side of the triggering event.

3 POST TRIG. Selects a trigger point that allows a display of waveform data occurring after the triggering event. One-eighth of the waveform is stored prior to the trigger point, and seven-eighths are stored after the trigger point.

DISPLAY. Presents a choice of either TIME or X-Y display of the STORE and VIEW waveforms.

1 TIME. When TIME display is selected, the horizontal deflection of the displayed waveform is provided by the digitized waveform x-axis.

2 X-Y. When X-Y display is selected, the horizontal deflection of the displayed waveform is provided by the stored Channel 1 vertical amplitude; the stored Channel 2 signal provides the display vertical deflection. A VERT MODE that displays both Channel 1 and Channel 2 must be selected to enable the STORE or VIEW X-Y display.

CURSORS. Turns on the CURSORS Mode for use with the STORE and VIEW waveforms and displays the menu used to control the CURSORS Mode operation (see Figure 2-13). The CURSORS Menu does not time out. Switching to another menu display using the MENU LAST button or selecting one of the front-panel menus (VERT MODE, Trigger SOURCE, or Trigger COUPLING), removes the CURSORS Menu from the display, but it will return to the readout as soon as the recalled menu either times out or the MENU ON/OFF button is pressed to turn off the displayed menu.

1 CURSOR SEL. Selects the cursor dot that is positioned by the DLY TIME/CURSOR position push buttons. Each push of the "1" MENU button switches the cursor dot that is positionable with the DELAY TIME/CURSOR position buttons to the opposite cursor.

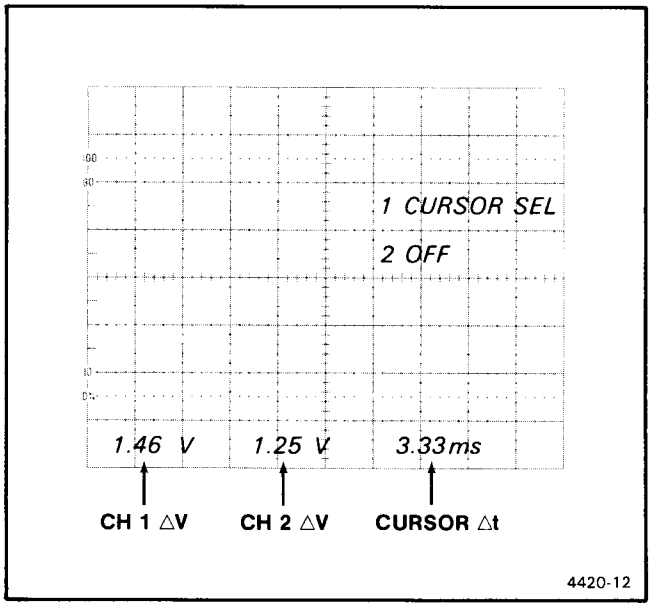


Figure 2-13. CURSORS Menu and cursor readout locations.

2 OFF. Turns off the CURSORS Mode and removes the CURSORS Menu display. Pressing the MENU LAST button before any other Main MENU has been selected, will return the CURSORS Menu to the display and reenters the CURSORS Mode.

NOTE

A firmware problem in Version 4.4 causes incorrect cursor readouts when attempting to measure time on 20 seconds and 10 seconds per division ROLL Mode acquisitions. It is recommended that cursors not be used to attempt to measure timing on waveforms acquired at these two ROLL Mode sweep speed settings.

PROCESS. Selects the stored signal processing function menu. The processing choices are selected from either the (WFM) waveform or the PARAMETER submenu. Before processing the waveforms, a ground reference must be acquired in the STORE Mode. This is done by switching the input coupling AC-GND-DC switches on the channel(s) to be processed to the GND position. Either the A Trigger MODE must be set to AUTO or an external trigger source must be used to obtain the ground baseline trace and trigger the sweep when the input signal is grounded. After switching back to either AC or DC input coupling, the Vertical POSITION controls must remain unchanged from the position at which the ground reference is obtained to keep a valid zero ground reference for the calculations.

WFM (Waveform). The WFM selections provide a choice of adding, subtracting, or multiplying the Channel 1 and Channel 2 STORE or VIEW waveform data together. The waveform calculations begin as soon as the numbered MENU button associated with the menu choice is pressed. The resulting waveform is displayed when the calculation is completed. The center horizontal graticule line is the zero reference of the calculated waveform display (providing that the Vertical POSITION controls are not moved after acquiring the ground reference). For example, if both the CH 1 and CH 2 input coupling switches are in the GND position, the trace resulting from a WFM calculation will appear on the center horizontal graticule line. To maintain the resulting waveform within the graticule viewing area, it is recommended that the input signals be displayed with plus or minus two divisions or less vertical amplitude from the ground reference. The WFM Menu choices and functions are as follows:

1 CH 1 + CH 2. Adds the waveform data of the Channel 1 and the Channel 2 input signals.

2 CH 1 − CH 2. Subtracts the waveform data of the Channel 2 input signal from the Channel 1 input signal.

3 CH 1 X CH 2. Multiplies the waveform data of the Channel 1 input signal by the Channel 2 input signal.

Waveform calculations are not performed until a VERT MODE is chosen that displays both Channels.

In STORE Mode, the waveform calculation is performed with each update of the display. Once a selected calculation is made, only the resulting waveform will be displayed. Changes in the input signals from either channel are automatically calculated in the displayed waveform. In VIEW Mode, each press of one of the WFM sub-menu item buttons first displays the original two VIEW waveforms, then the calculated waveform. When a selection is made, a greater-than symbol (>) is displayed in front of the chosen sub-menu item. When the calculation is completed, the > symbol is replace by an arrow-head symbol (▷), and the calculated waveform is displayed.

If the cursor measurement mode is used on the calculated waveform display, the vertical amplitude readouts will be in divisions rather than in voltage units. For ease of menu operation, it is recommended that the cursor measurements be made on VIEW calculated waveforms rather than on STORE calculated waveforms. The STORE waveform display updates if the CURSORS Menu is chosen in order to allow switching the active cursor.

NOTE

While the 336 is executing PROCESS Menu calculations, the microprocessor responds to front-panel changes at a slower rate. However, changes to the front-panel setting are read during the processing time and will be executed as soon as the calculation is completed.

PARAMETERS. This feature permits the user to obtain specific types of parametric information about the waveform data. The PARAMETERS Menu selections are enabled on both the STORE and the VIEW waveforms. The parametric calculations begin as soon as the numbered MENU button associated with the menu choice is pressed. The calculation results are displayed immediately below the menu as soon as the calculation is completed (see Figure 2-14).

The choices of parametric calculations available are as follows:

1 RMS. Determines the RMS value of the waveform data.

2 P-P. Determines the peak-to-peak amplitude of the waveform data.

3 MEAN. Determines the mean value of the waveform data.

As with the waveform calculations, the Vertical POSITION controls must not be moved once the ground reference has been obtained. (Ground reference level does not affect the peak-to-peak waveform calculations.)

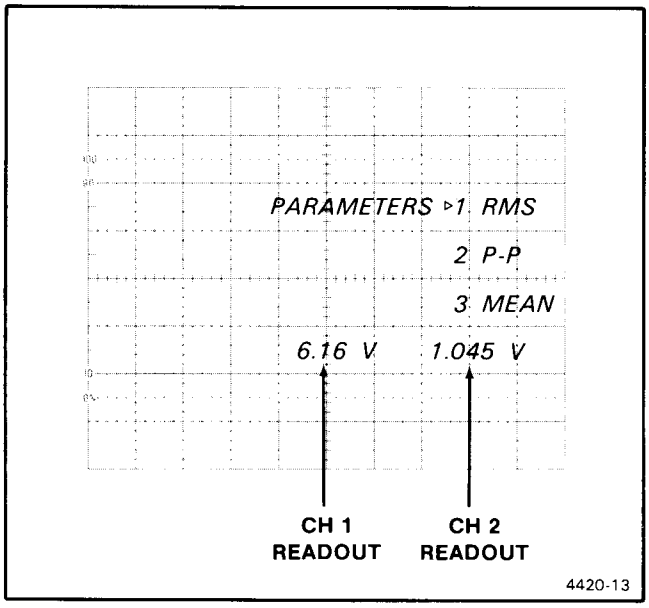


Figure 2-14. PARAMETERS Menu display with RMS indicated and Channel 1 and Channel 2 readouts indicated.

DATA OUT Menu—Controls outputting of waveform data. Waveforms may be plotted by an external analog X-Y Plotter using the drive signals provided from the X and Y CHART OUT connectors as a standard feature. Parallel, eight-bit data bytes defining the stored waveforms may be sent via the General Purpose Interface Bus (GPIB) IEEE-488 output port provided with the Option 01 instruments.

CHART. The sub-menu associated with the CHART feature is used to calibrate the maximum and minimum deflection positions of the external X-Y Plotter to the graticule of the 336 and control the data output rate. CHART is enabled for VIEW waveform displays only. STORE Mode must be turned off before the CHART Menu is active. If a NON STORE display is on with VIEW when one of the CHART selections (except STOP) is made, it will be turned off automatically.

1 FAST START. Starts the data output rate at the auto-fast speed.

2 SLOW START. Starts the data output rate at the auto-slow speed. (Switching between start speeds causes the waveform data to restart at the beginning.)

NOTE

In the case of both FAST START and SLOW START, the data output rate varies automatically as a factor of the data difference in the leading data.

NOTE

If any other menu selection is made (such as VERT MODE or TRIGGER SOURCE), the CHART Menu is removed from the display, and the data output stops just as when the STOP MENU button is pressed. Once the plot is started, do not make any other menu selections until the waveform is completely plotted and the plot pen lifted.

3 CAL. Sends two calibration signals to be used to set up the external X-Y Plotter in preparation for plotting the waveform. Each press of the CAL MENU button alternately switches the X and Y output voltages between the maximum and minimum graticule deflection points to calibrate the X-Y Plotter deflection to the graticule. The deflection voltages correspond to the lower left and upper right corners of the 336 graticule.

4 STOP. Ceases the output of analog data to the X and Y CHART OUT connectors immediately upon pressing the STOP MENU button. The voltages at the X and Y output connectors return to the values of the delay time control voltage and the trace separation control voltage held prior to activating the CHART feature when the STOP MENU button is pressed. If a NON STORE display was present before pressing the CAL or one of the START MENU buttons, it will be returned to the display upon pressing the STOP MENU button.

After calibrating the X-Y Plotter, pressing either of the plot START MENU buttons begins the waveform plot. The plot pen remains at the start of the CH 1 trace for about seven seconds before the data plot commences. At the completion of the CH 1 trace, the plot pen again remains stationary for about seven seconds. If a two-trace waveform is plotted, the pen moves to the beginning of the CH 2 trace at the end of the wait following the completion of the CH 1 trace. The pen again remains for about seven seconds, then begins the CH 2 waveform. The delays allow the user to avoid a retrace by manually lifting the plotting pen at the end of the Channel 1 plot, then again lowering it to plot Channel 2. The pen also remains at the end of the last waveform plotted for about seven seconds, then the voltages present at the X and Y CHART OUT connectors return to the previously set values for the TRACE SEP and DELAY TIME position control voltages.

NOTE

When the CHART Menu is not selected, the DELAY TIME control voltage appears at the X CHART OUT terminal, and the TRACE SEP control voltage appears at the Y CHART OUT terminal. Disconnecting the X-Y Plotter from the 336 is recommended when not is use for plotting waveforms.

GPIB. Enables the user to control the waveform data transmission capability provided by the GPIB portion of Option 01. See "Options" (Section 7 of this manual) for additional information on the GPIB capabilities of the 336.

1 INCR. Used to increment the bus address of the 366. A choice of addresses from 0 to 30 is available for MTA (My Talk Address). The address is incremented once for each press of the INCR MENU button. Incrementing past address 30 switches the GPIB to the TALK ONLY Mode.

2 DECR. Used to decrement the bus address of the 336. Decrementing below address 0 also switches the GPIB to the TALK ONLY Mode.

3 TRANSMIT. Used to initiate a waveform transmission via the data bus. An SRQ (service request) is issued prior to sending the waveform data to start the handshake with a controller or a listener on the bus. In TALK ONLY Mode,

pressing the TRANSMIT button is the only way to start the data transmission. When MTA is set to a number, a bus controller can initiate data transmission by addressing the 336 GPIB Option to talk. If no waveform data is available to be sent (such as when in NON STORE or in VIEW with no waveform data stored in the selected VIEW stack number) the 366 will send the ID (identification) portion of the transmission only. If waveform data is available, it is sent immediately following the ID message.

If both Channel 1 and Channel 2 data are available, a single request (press of the TRANSMIT button or request by a bus controller) sends Channel 1 data followed immediately by the Channel 2 data.

4 STOP. Ceases transmission of waveform data via the GPIB option. Two different situations exist: one is when the 336 is addressed to talk with a controller on the bus, and the other is when the 336 is in the TALK ONLY Mode. In the first situation, a press of the STOP button will cause a service request (SRQ) to be asserted along with the Stop Request Status Byte (decimal 197). After the controller receives the status byte, it would then have the capability to control the bus as the application requires. It can, for example, send Device Clear (DCL) followed by Untalk (UNT) to abort the transmission. In the TALK ONLY (TON) Mode, STOP completes the current handshake, then sends the message terminator (CR and LF with EOI).

SCOPE—Enables the user to select the function performed by the front-panel VAR SWP/HOLDOFF control and the amount of trace separation between the A Intensified and the B Delayed NON STORE traces when ALT Horizontal Display Mode is in use.

1 HORIZ VAR. The VAR SWP/HOLDOFF control is a single potentiometer that can be either the variable sweep speed control or the variable holdoff control. The user selects its function depending on the requirements of the measurements to be made. Description of the VAR control operation in either mode is included in the discussion of the VAR SWP/HOLDOFF control earlier in this section of the manual (see HORIZONTAL CONTROLS).

2 TRACE SEP. Permits menu control of the trace separation between the A Intensified and the B Delayed NON STORE traces of the ALT (Alternate) Horizontal Display Mode. The INCR and DECR MENU buttons are used to select from zero to about two divisions of separation in half-division steps.

CHARACTER—Permits user control of two display functions: READOUT and TIME OUT.

READOUT. Presents choices of READOUT ON or OFF. See Figure 2-15 for the READOUT Menu controlled displays. The READOUT Menu may be used to turn off those readouts normally displayed at all times (plus others).

1 ON. VOLTS/DIV and SEC/DIV settings with modifiers are displayed across the top of the crt as appropriate with the current front-panel settings. Delay time, CURSOR readouts, and VIEW waveform stack number are displayed at the bottom of the crt when appropriate. Modifying symbols displayed in front of the VOLTS/DIV and A SEC/DIV readouts are the colon (:)— indicating that autoranging is on, the greater-than symbol (>)—indicating that the readout is uncalibrated, and the down-arrow symbol (↓)—indicating the CH 2 vertical display is inverted.

2 OFF. VOLTS/DIV and SEC/DIV readouts, delay time readout, CURSOR readouts, and VIEW waveform stack number are turned off. Waveform parameter readouts (the calculated values resulting from the PARAMETERS sub-menu) are not affected by turning off the READOUT.

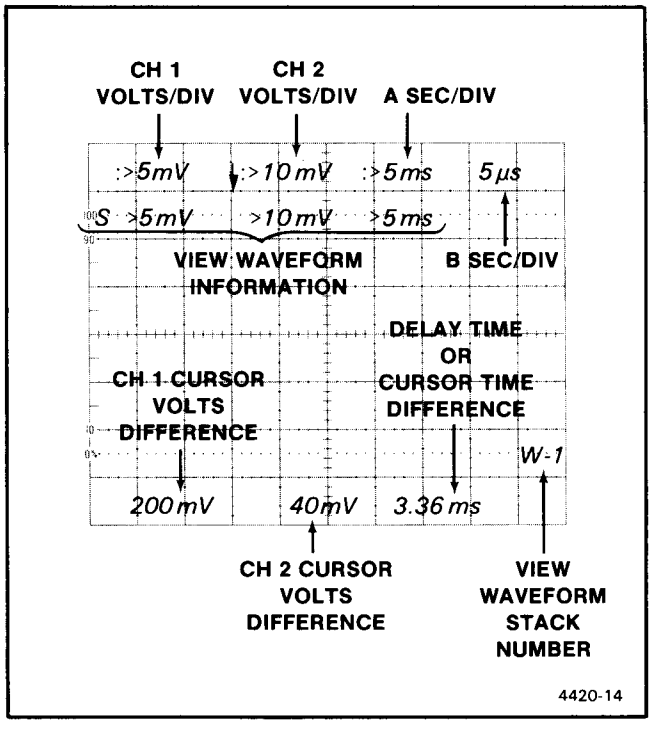


Figure 2-15. READOUT Menu controlled displays.

TIME OUT. Controls the amount of time that the timed menus are displayed.

1 FAST. Timed menus remain displayed for about one second. This selection is useful for a user that is familiar with oscilloscope's operation and does not require the menus to be displayed for a period of time to make a choice.

2 NORMAL. Timed menus remain displayed for about five seconds. As the name implies, this selection allows the menus to be displayed for enough time to permit most decisions to be made.

3 SLOW. Timed menus remain displayed for about 15 seconds. For a user becoming familiar with the instrument, this time-out selection allows the menus to be displayed long enough for the menu items to be studied.

SETTINGS—Permits the user to view the current settings for the following items:

VERT MODE

TRIG SOURCE

TRIG CPLG

STORE MODE

ACQ WINDOW

DISPLAY

HORIZ VAR

The SETTINGS Menu does not time out, but any change in the controls requiring an update by the microprocessor removes it from the display.

OPERATING CONSIDERATIONS

INTRODUCTION

This part contains basic operating information and techniques that should be considered before attempting to make any measurements with your instrument.

GRATICULE

The graticule is internally marked on the faceplate of the crt to eliminate parallax-viewing error and to enable measurements (see Figure 2-16). It is marked with eight vertical and ten horizontal major divisions. In addition, each major division is divided into five subdivisions. The vertical deflection factors and horizontal timing are calibrated to the graticule so that accurate measurements can be made directly from the crt. Also, percentage marks for the measurement of rise and fall times are located on the left side of the graticule.

GROUNDING

The most reliable signal measurements are made when the 336 and the unit under test are connected by a common reference (ground lead) in addition to the signal lead or probe. The probe's ground lead provides the best grounding method for signal interconnection and ensures the maximum amount of signal-lead shielding in the probe cable. A separate ground lead can also be connected from the unit under test to the SIG GND receptacle on the oscilloscope's right side panel.

SIGNAL CONNECTIONS

Probes

Generally, the accessory probes supplied with the instrument provide the most convenient means of connecting a signal to the vertical inputs of the instrument. The probe and probe lead are shielded to prevent pickup of electromagnetic interference, and the 10X attenuation factor of the probe offers a high input impedance that minimizes signal loading in the circuitry under test. The attenuation factor of the standard accessory probe is coded so that the VOLTS/DIV readout seen on the crt is automatically switched to the correct scale factor when the probe is attached.

Both the probe itself and the probe accessories should be handled carefully at all times to prevent damage to them. Avoid dropping the probe body. Striking a hard surface can cause damage to both the probe body and the probe tip. Exercise care to prevent the cable from being crushed or kinked. Do not place excessive strain on the cable by pulling.

The standard-accessory probe is a compensated 10X voltage divider. It is a resistive voltage divider for low frequencies and a capacitive voltage divider for high-frequency signal components. Inductance introduced by either a long signal or ground lead forms a series-resonant circuit. This circuit will affect system bandwidth and will ring if driven by a signal containing significant frequency components at or near the circuit's resonant frequency. Oscillations (ringing) can then appear on the oscilloscope waveform display and distort the true signal waveshape. Always keep both the ground lead and the probe signal-input connections as short as possible to maintain the best waveform fidelity.

Misadjustment of probe compensation is a common source of measurement error. Due to variations in oscilloscope input characteristics, probe compensation should be checked and adjusted, if necessary, whenever the probe is moved from one oscilloscope to another or between channels. See the probe compensation procedure in "Operator's Check and Adjustments," or consult the instructions supplied with the probe.

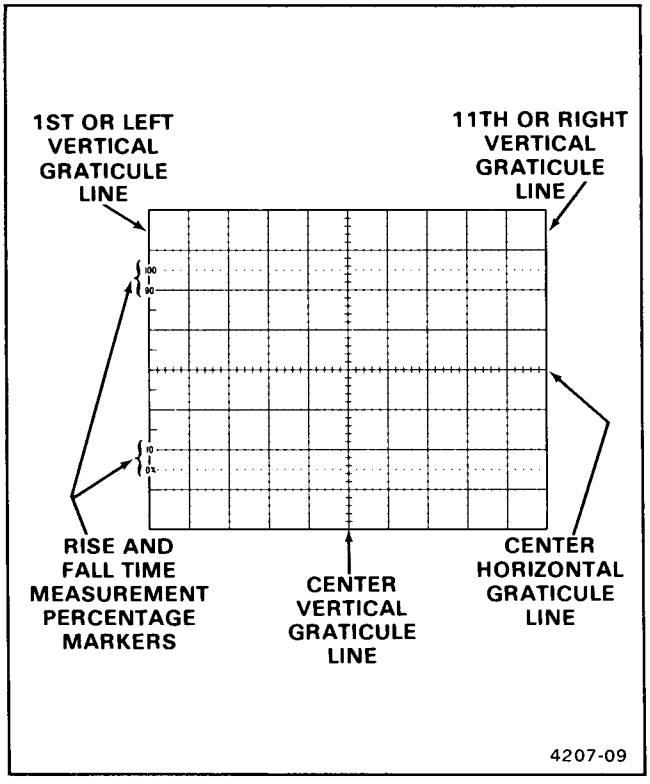


Figure 2-16. Graticule measurement markings.

Coaxial Cables

Cables may also be used to connect signals to the vertical input connectors, but they may have considerable effect on the accuracy of a displayed waveform. To maintain the original frequency characteristics of an applied signal, only high-quality, low-loss coaxial cables should be used. Coaxial cables should be terminated at both ends in their characteristic impedance. If this is not possible, use suitable impedance-matching devices.

INPUT-COUPLING CAPACITOR PRECHARGING

When the input coupling switch is set to the GND position, the input signal is connected to ground through the input coupling capacitor and a high resistance value. This series combination forms a precharging circuit that allows the input-coupling capacitor to charge to the average dc voltage level of the signal applied to the input connector. Thus, any large voltage transients that may accidentally be generated will not be applied to the vertical amplifier input when the input coupling is switched from GND to AC. The precharging network also provides a measure of protection to the external circuitry by reducing the current levels that can be drawn from the external circuitry while the input coupling capacitor is charging.

If AC input coupling is in use, the following procedure should be followed whenever the probe tip is connected to a signal source having a different dc level than that previously applied. This procedure becomes especially useful if the dc level difference is more than ten times the VOLTS/DIV switch setting.

1. Set the AC-GND-DC switch to GND before connecting the probe tip to a signal source.

2. Touch the probe tip to the oscilloscope chassis ground.

3. Wait several seconds for the input coupling capacitor to discharge.

4. Connect the probe tip to the signal source.

5. Wait several seconds for the input coupling capacitor to charge to the dc level of the signal source.

6. Set the AC-GND-DC switch to AC. A signal with a large dc component can be vertically positioned within the graticule area, and the ac component of the signal may be measured in the normal manner.

OPERATOR'S CHECKS AND ADJUSTMENTS

INTRODUCTION

To verify the operation and basic accuracy of your instrument before making measurements, perform the following checks and adjustment procedures. If adjustments are required beyond the scope of these operator's checks and adjustments, see the "Adjustment Procedures" in Section 5 of this manual.

For new equipment checks, before proceeding with these instructions, refer to "Preparation for Use" in this section to prepare the instrument for the initial start up before applying power.

INITIAL SETUP

1. Verify that the POWER switch is OFF (out position with the word OFF visible), then plug the power cord into the ac power outlet.

2. Press in the POWER switch button (ON) and set the instrument controls to obtain a baseline trace.

Display

INTENSITY	Midrange
FOCUS	Midrange

Vertical

VERT MODE	CH 1
CH 1 and CH 2 POSITION	Midrange
CH 1 VOLTS/DIV	5 mV
CH 1 AC-GND-DC	DC
CH 2 AC-GND-DC	DC
CH 1 and CH 2 VAR	CAL (in detent)

Horizontal

A SEC/DIV	0.5 ms
VAR SWP/HOLDOFF	CAL (in detent)
POSITION	Midrange
X10 MAG	Off (indicator unlighted)

Trigger

SOURCE	CH 1
COUPLING	AC
MODE	AUTO (P-P)
A LEVEL	For a stable display (with signal applied)
A SLOPE	+ (plus)
B LEVEL	Runs After Delay (fully ccw)

Display Mode

NON STORE	On (indicator lighted)
STORE	Off (indicator unlighted)
VIEW	Off (indicator unlighted)

3. Adjust the INTENSITY and FOCUS controls for the desired display brightness and best focused trace.

4. Adjust the Vertical and Horizontal POSITION controls to position the trace within the graticule area.

5. Allow the instrument to warm up before commencing the adjustment procedures (20 minutes is recommended for maximum accuracy).

TRACE ROTATION ADJUSTMENT

1. Preset the instrument controls and obtain a baseline trace as described in "Initial Setup."

2. Use the Channel 1 POSITION control to move the baseline trace to the center horizontal graticule line.

NOTE

Normally, the resulting trace will be parallel to the center horizontal graticule line, and the TRACE ROTATION adjustment should not be required.

3. If the baseline trace is not parallel to the center horizontal graticule line, use a small-bladed screwdriver or alignment tool to adjust the TRACE ROTATION control and align the trace with the graticule line (see Figure 2-11 for location of the control on the bottom of the instrument).

PROBE COMPENSATION

Misadjustment of probe compensation is one of the sources of measurement error. The attenuator probes are equipped with compensation adjustments. To ensure optimum measurement accuracy, always check probe compensation before making measurements. Probe compensation is accomplished as follows:

1. Preset the instrument controls and obtain a baseline trace as described in "Initial Setup."

2. Connect the two 10X probes (supplied with the instrument) to the CH 1 OR X and CH 2 OR Y input connectors. Observe that the CH 1 VOLTS/DIV readout display changes from 5 mV to 50 mV when the 10X probe is attached to the CH 1 OR X input.

3. Remove the hook tip from the end of both probes.

4. Insert the Channel 1 probe tip into the CAL OUT connector

NOTE

While the probe tip is in the CAL OUT connector, use care not to place excessive side force on the probe body. It is possible to break off the probe tip if care is not taken.

5. Use the CH 1 POSITION control to vertically center the display. Adjust the A Trigger LEVEL control to obtain a stable display on the + (plus) SLOPE, if necessary.

6. Check the waveform display for overshoot and rounding (see Figure 2-17). If necessary, use a small-bladed screwdriver to adjust the probe compensation for a square front corner on the waveform.

7. Remove the Channel 1 probe tip from the CAL OUT connector and insert the Channel 2 probe tip.

8. Use the VERT MODE Menu to select CH 2 for display.

9. Use the Trigger SOURCE Menu to select CH 2 as the trigger source.

10. Use the CH 2 POSITION control to vertically center the display, and check the waveform display for overshoot and rounding as for Channel 1. Adjust the probe compensation, if necessary, for a square front corner on the waveform.

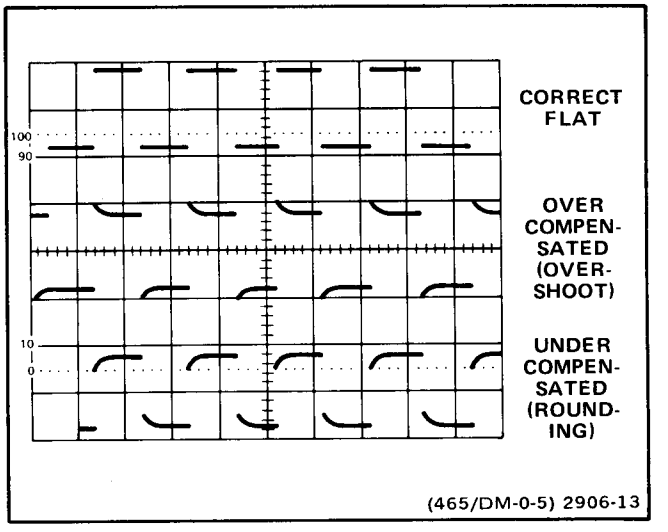


Figure 2-17. Probe compensation.

NOTE

Refer to the instruction manual supplied with the probe for more complete information on the probe and probe compensation.

VERTICAL ACCURACY CHECK

The basic vertical gain accuracy, within the accuracy of the CAL OUT signal, may be checked using the following procedure. Step 1 continues from Step 10 of the preceding probe compensation check.

1. Check the CAL OUT signal amplitude for six divisions within ±0.25 division.

2. Press the STORE Display Mode button on and press the NON STORE Display Mode button off.

3. Check the STORE waveform display of the CAL OUT signal for six divisions within ±0.25 division.

4. Press ENTER to store the waveform, then press VIEW to display the stored CAL OUT waveform.

5. Check the VIEW waveform display for six divisions of amplitude within ±0.25 division.

6. Select the CURSORS measurement mode. (See either the menu diagram in the front-panel cover or the STORAGE Menu description in "Controls and Connectors," in this section for the menu selections necessary.)

7. Position one cursor dot on the positive peak amplitude of the waveform display using the DLY TIME/CURSOR position push buttons on the front panel. Press the CURSOR SEL button (MENU 1) to activate the second cursor dot, and place it on the negative peak amplitude of the waveform.

8. Check the CURSOR volts readout for CH 2 is 300 mV ±18 mV.

9. Remove the Channel 2 probe tip from the CAL OUT connector and insert the Channel 1 probe tip.

10. Press the CH 1 VERT MODE button and the CH 1 Trigger SOURCE button to obtain a stable display of CH 1.

11. Press the MENU 2 button to turn the CURSOR measurement mode OFF. Turn NON STORE Mode on and VIEW Mode off.

12. Repeat Steps 1 through 8 to check the Channel 1 vertical accuracy.

HORIZONTAL ACCURACY CHECK

A check of the horizontal timing can be made using the accurate time measurement capability of the CURSOR measurement mode. Obtain a baseline trace, either from the initial setup or from the previous Vertical Accuracy Check, by switching the CH 1 AC-GND-DC switch to the GND position, and use the following procedure to check the horizontal accuracy.

1. Press STORE Display Mode on and turn the NON STORE Display Mode off.

2. Set the SEC/DIV switch setting to 1 ms.

3. Select POST TRIG acquisition window using the Main MENU selections, then select the CURSOR measurement mode.

4. Use the Horizontal POSITION control to position the start of the STORE Mode trace to the left graticule edge and use the Vertical POSITION control to align the baseline trace with the center horizontal graticule line.

5. Position one of the cursor dots to the second vertical graticule line (one division in from the left edge) using the DLY TIME/CURSOR position control buttons.

6. Press the MENU 1 button (CURSOR SEL) to activate the second cursor dot and use the DLY TIME/CURSOR position buttons to position the cursor dot to the tenth vertical graticule line (one division in from the right graticule edge) for an eight-division spacing between the cursor dots.

7. Check that the cursor time difference readout is 8 ms ±0.16 ms (7.84 ms to 8.16 ms).

8. Ensure that the CH 1 probe tip is in the CAL OUT connector and set the CH 1 AC-GND-DC switch to DC. Set the SEC/DIV switch setting to obtain a display of at least one full period of the calibrator signal (0.1 or 0.2 ms per division).

9. Use the Vertical and Horizontal POSITION controls to center the display as necessary.

10. Use the DLY TIME/CURSOR position control buttons and the CURSOR SEL button (MENU 1) to align the cursor dots with the rising edges of the CAL OUT signal (measurement is of the calibrator signal period). Note the cursor dot time difference readout and the graticule measurement (horizontal distance between rising edges as taken from the graticule markings) of the signal for later reference.

11. Check that the cursor readout of the calibrator period and the graticule measurement of the calibrator period agree within ±2%.

12. Turn the STORE Display Mode off and turn the NON STORE Display Mode on. Press Main MENU button 2 to turn the CURSOR Menu off.

13. Use the Horizontal POSITION control to align the first rising edge of the calibrator signal with the second vertical graticule line.

14. Determine the horizontal graticule measurement of the calibrator signal period. Note the reading for later reference.

15. Check that the NON STORE Mode calibrator signal period measurement obtained from the graticule markings is within ±3% of the STORE Mode calibrator signal period obtained in step 10.

16. Press the X10 MAG button on (indicator illuminated) and set the A SEC/DIV switch setting to obtain a display of at least one full period of the calibrator signal (0.1 or 0.2 ms per division).

17. Check that the magnified NON STORE Mode calibrator signal period measurement obtained from the graticule markings is within ±4% of the STORE Mode calibrator signal period obtained in Step 10.

18. Press the X10 MAG button to turn off the magnified display and set the A SEC/DIV switch setting to obtain a display of at least two full periods of the calibrator signal (0.2 ms or 0.5 ms per division).

19. Pull the SEC/DIV knob to the out position for ALT Horizontal Display Mode and set the B SEC/DIV to one sweep speed faster than the A SEC/DIV switch setting.

20. Press and hold the left DLY TIME/CURSOR position button until the intensified zone on the A Sweep trace is positioned to its maximum left position (delay time readout stops changing). (The INTENSITY control may require adjustment to view the intensified zone.)

21. Use the DLY TIME/CURSOR position control buttons to align the first rising edge of the B DLY'D trace calibrator signal with center vertical graticule line (commonly used as a measurement reference for making delayed time measurements).

22. Press both the DLY TIME/CURSOR buttons in together to zero the delay time readout. (Verify that the rising edge of the signal remains correctly aligned when the readout is zeroed. If it does not, perform the alignment and zeroing to perfect the initial positioning.)

23. Use the DLY TIME/CURSOR buttons to align the second rising edge of the calibrator signal with the center vertical graticule line. When the rising edge is nearly positioned, press in the SEC/DIV knob to obtain smoother positioning control, if needed.

24. Read the delay time readout (calibrator signal period) and note for further reference.

25. Check that the delay time readout is within ±2% of the cursor time difference readout obtained in Step 10.

THEORY OF OPERATION

SECTION ORGANIZATION

This section contains a functional description of the 336 Oscilloscope circuitry. The discussion begins with an overview of the instrument functions and continues with detailed explanations of each major circuit. Reference is made to supporting schematic and block diagrams which will facilitate understanding of the text. These diagrams show interconnections between parts of the circuitry, identify circuit components, list specific component values, and indicate interrelationships with front-panel controls and side-panel connectors.

The block diagram and the schematic diagrams are located in the tabbed "Diagrams" section at the rear of this manual, while smaller functional diagrams are contained within this section near the associated text. The particular schematic diagram associated with each circuit description is identified in the text, and the diagram number is shown (enclosed within a diamond symbol) on the tab of the appropriate foldout page. For optimum understanding of the circuit being described, refer to both the applicable schematic diagram and the functional block diagram.

HYBRID AND INTEGRATED CIRCUIT DESCRIPTIONS

Digital Logic Conventions

Digital logic circuits perform many functions within this instrument. The operation of these circuits is represented by specific logic symbology and terminology. Most logic-function descriptions contained in this manual use the positive-logic convention. Positive logic is a system of notation whereby the more positive of two levels is the TRUE (or 1) state; the more negative level is the FALSE (or 0) state. In the logic descriptions, the TRUE state is referred to as HI, and the FALSE state is referred to as LO. The specific voltages which constitute a HI or a LO vary between individual devices. For specific device characteristics, refer to the manufacturer's data book.

Hybrids

Some of the circuits in this instrument are implemented in hybrid devices. The hybrids are specialized electronic devices combining thick-film and semiconductor technologies. Passive, thick-film components and active, semiconductor components are interconnected to form the circuit on a ceramic carrier. The end result is a relatively small "building block" with enhanced performance characteristics, all in one package. Hybrid circuits are shown on schematics simply as blocks with inputs and outputs identified. Information about hybrid functioning is contained in the related portion of the Detailed Circuit Description.

Linear Devices

The operation of individual linear integrated circuit devices is described in this section using waveforms or other graphic techniques to illustrate their operation.

BLOCK DIAGRAM

The following discussion is provided as an aid in understanding overall operation of the 336 Oscilloscope circuitry before the individual circuits are discussed in detail. A simplified block diagram of the 336 Oscilloscope, showing basic interconnections, is shown in Figure 3-1. The diamond-enclosed numbers in each block refer to the schematic diagram(s) at the rear of this manual in which the related circuitry is located.

BLOCK DESCRIPTION

The Low-Voltage Power Supply is a high-efficiency, switching supply with active output regulation that transforms the ac source voltage to the various dc voltages required by the 336. The High-Voltage Power Supply and CRT circuit develops the high accelerating potentials required by the crt using voltage multiplication techniques, and a dc restorer provides interfacing for the low-potential intensity signals from the Unblanking Logic to the crt control grid.

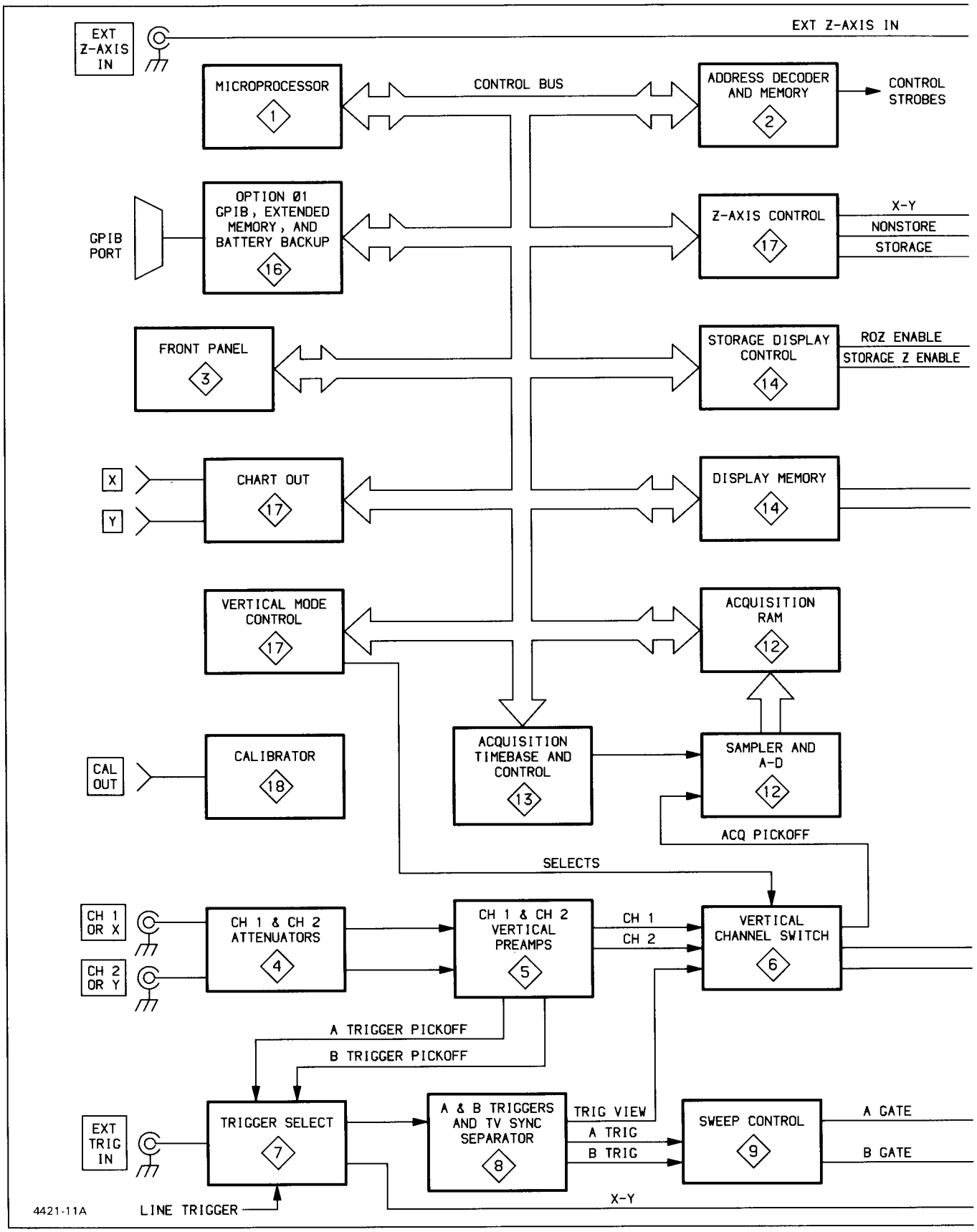


Figure 3-1. Simplified Block Diagram.

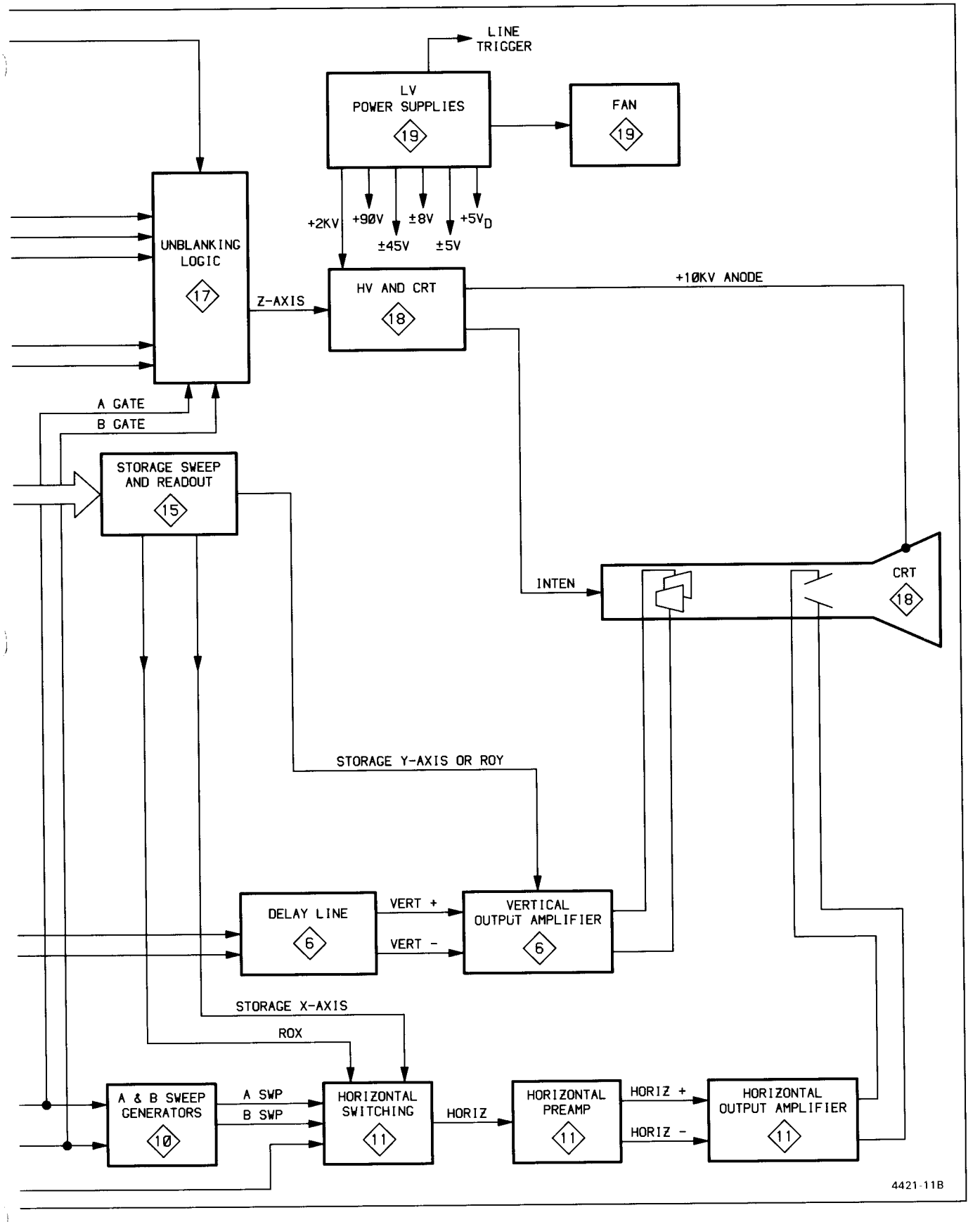


Figure 3-1. Simplified Block Dkiagram (cont).

Most of the activities of the 336 are directed by a Microprocessor. The Microprocessor, under firmware control (firmware is the programmed instructions contained in read-only memory that tells the processor how to operate), monitors instrument functions and sets up the operating modes according to the instructions received.

Various types of data to and from the Microprocessor (program instructions, constants, control data, etc.) are transferred over a group of eight bidirectional signal lines called the Data Bus. The Data Bus is dedicated solely to Microprocessor-related data transfer.

Another group of signal lines, called the Address Bus, are responsible for selecting or "addressing" the memory location or device that the Microprocessor wants to communicate with. Typically, depending on the instruction being executed, the processor places an address on the Address Bus that identifies the location the Microprocessor must communicate with. This address, along with some enabling logic, opens up an appropriate data path via the Data Bus; and data is then either read from or written to that location by the processor. These busses, grouped together for simplicity, are shown on the Block Diagram (Figure 3-1) as one large Control Bus.

When power is applied to the 336, a brief initialization sequence is performed, and then the processor begins scanning the Front-Panel controls. Depending on the operating mode called for, the processor will generate some mode-dependent data that must be placed in temporary storage (along with the Front-Panel settings) for later use. The RAM (random-access memory) in the Address Decoder and Memory stage provides this storage function.

The Front-Panel switch settings detected cause the processor to set various control registers and control voltages within the instrument that define the operating mode of the instrument. These register settings and voltage levels control the vertical channel section and deflection factors, the sweep rate, the triggering parameters, the readout activity, and sequencing of the display. Loading the control data into the various registers throughout the instrument is done via the data bus, while the individual control-clock signals that load the registers are generated by the Address Decoder.

Coordination of the vertical, horizontal, and Z-axis (intensity) components of the display must be done in real time. Due to the speed of these display changes and the precise timing relationships that must be maintained between display events, direct sequencing of the display is beyond the capabilities of the processor. Instead, control data from the processor is sent to several register-controlled stages that sequence the real-time display signals. The control stages are stepped through a predefined sequence that is determined by the control data. Typically, as the sequence is being executed, the oscilloscope may be changing vertical signal sources, Z-axis intensity levels, triggering sources, and horizontal sweep signal sources. The specific activities being carried out by any control stage depend on the display mode called for by the control data.

Vertical deflection for crt displays comes from either or both of the two side-panel vertical inputs, the trigger circuitry for trigger-view displays or, when displaying readout or stored waveform information, from the Storage Display circuitry. Signals applied to the side-panel Channel 1 and Channel 2 inputs are connected to their respective Preamplifiers via processor-switched Attenuator networks. Control data from the Microprocessor, defining the attenuation factor selected for each channel, is loaded into the Attenuator control register. The relay switches of each Attenuator network are then either opened or closed by the Attenuator Register output levels.

Attenuated Channel 1 and Channel 2 input signals are amplified by their respective Preamplifiers. The gain factor for the Preamplifiers is settable by control data from the processor. The preamplified signals are applied to the Vertical Channel Switch along with the trigger signal, where they are selected (by select signals from the Vertical Mode Control stage) for display when required.

The selected vertical (or trigger-view) signal is applied to the Delay Line (which delays the signal long enough to see the trigger point) and is then amplified by the Vertical Output Amplifier. This amplifier raises the real-time and storage (waveform or readout) signals to proper crt drive levels to vertically deflect the crt beam. Both the channel 1 and channel 2 vertical input signals are applied to the Trigger Select circuitry via TRIGGER PICKOFF outputs from the Preamplifier stage. Either signal may be selected as the trigger source for the A or the B trigger circuitry (separate trigger SOURCE selection for A and B is not provided). Selection is controlled by the Microprocessor setup data. Two other trigger sources available are LINE and external (EXT and EXT/10). The TV Sync Separate (one of the COUPLING selections) extracts the horizontal and vertical sync signals from an applied composite video signal for stable triggering on TV signals. When the selected trigger signal meets the preset trigger requirements, a sweep can be initiated.

The Sweep Control circuit initiates both the A Sweep and the B Sweep as required by the display mode selected. In the case of A Sweeps, the Sweep Control circuit will enable the A Sweep Generator whenever sweep holdoff requirements are met and an A Trigger signal occurs. For B Sweeps, and in the case of intensified sweeps, the A Sweep's delay gate signal enables the B Sweep Generator. Depending on the B Trigger mode selected, a B Sweep will be initiated either immediately after the A delay has elapsed

(RUN AFT DLY) or on the next B Trigger signal received after the A delay time has elapsed (TRIG AFT DLY). The slopes of the sweep ramps are dependent on control data from the Microprocessor. The data is loaded into internal control registers of the A and B Sweep Generators.

Sweep signals generated by the A and B Sweep Generators are applied to the Horizontal Switching stage, which selects the source of the signal applied to the Horizontal Preamp. The Horizontal Switching stage will select from A SWP, B SWP, X-Y (a buffered version of the CH 1 signal), the STORAGE X-AXIS or the RO X (readout X) signals, depending on display mode control data from the Microprocessor.

The selected signal is amplified to crt drive levels by the Horizontal Preamp and the Horizontal Output Amp and provides the horizontal deflection of the crt beam.

To control the display intensity, the Microprocessor will write mode information to the Z-Axis Control stage. This stage produces the mode-dependent, real-time control signals for switching Z-Axis display modes. The Unblanking Logic will change the Z-Axis drive level based on the type of display selected.

The varying Z-Axis drive signal is coupled to the high-voltage environment of the crt by a dc restorer circuit within the HV and CRT stage. The resulting INTEN output, along with the horizontal and vertical deflection signals, will produce a visible display of real-time waveform, stored waveform, and readout information on the crt.

As with the real-time displays, acquisition and display of stored waveforms is controlled by Microprocessor control data written into control registers within the stages being controlled.

To acquire a waveform from the CH 1 or CH 2 inputs, mode data written into the Vertical Mode Control stage will cause the Vertical Channel switch to route the desired vertical signal to the Sampler and A-D stage via the ACQ PICK-OFF lines. Sampling-rate and sampling-mode data written to the Acquisition Time Base and Control stage causes sampling clocks to be generated at the proper rate for the selected sampling mode. The Sampler and A-D converter samples the applied signal and stores a digital representation of each sampled point into the Acquisition RAM. When the entire waveform has been acquired, it is transferred to Display Memory for future recall.

Depending on display-mode information written into the Storage Display Control stage, it will continuously clock the selected waveform data from the Display Memory to the Storage Sweep and Readout circuit, producing the vertical deflection data for the selected waveform.

The Storage Sweep and Readout stage routes this vertical deflection information (for storage waveforms or readout displays) to the Vertical Output Amp. It also produces the sweep ramp to display this stored waveform deflection data against and routes it to the Horizontal Switching stage. For readout displays, the Storage Sweep and Readout stage will produce horizontal readout deflection signals instead of a waveform sweep ramp.

Unblanking of storage displays is controlled by signals from the Storage Display Control stage to the Unblanking Logic.

With these Z-Axis, horizontal deflection, and vertical deflection signals amplified to their proper levels, a storage waveform or readout display will result.

The optional GPIB, Extended Memory, and Battery Backup board provides additional memory locations for storing up to eight additional acquired waveforms. The Battery Backup portion of this circuit will maintain the stored waveform (and scale factor) data with instrument power off.

The GPIB interface circuit allows the 336 to transfer its acquired waveform data to another GPIB device under control of a GPIB controller.

The Chart Out circuit allows the Miroprocessor to output the stored waveform data in analog fashion to control an external X-Y plotter. This allows hard copies of the acquired waveform data to be made.

The Calibrator circuit produces an approximate 1 kHz square-wave output used for matching the frequency response of the oscilloscope probes to the vertical channels to which they are connected. The Fan provides instrument cooling.

MICROPROCESSOR ◇1

The Microprocessor (diagram 1) directs the operation of most oscilloscope functions by following firmware control instructions stored in memory. These instructions direct the Microprocessor to monitor the front-panel controls and to send control signals that set up the various signal processing circuits accordingly.

Microprocessor

The Microprocessor (U100) is the center of control activities. It has an eight-bit, bidirectional data bus for data transfer (D0-D7) and a sixteen-bit address bus (A0-A15) for selecting the source or destination of the data. Precise timing of instruction execution, addressing, and data transfer is provided by an external crystal-controlled clock signal.

The clock signal is developed by the Microprocessor Clock stage and applied to the Microprocessor at pin 6. Using the external clock as a reference, the Microprocessor generates synchronized control signals ($\overline{WR}$ (write), $\overline{RD}$ (read), $\overline{MREQ}$ (memory request) and $\overline{IORQ}$ (IO request)) that maintain proper timing relationships throughout the instrument.

Microprocessor Clock

The Microprocessor Clock stage generates a 2.4576 MHz square-wave signal to the Microprocessor and a 1.2288 MHz clock to other timing circuitry. The clock generator IC U110 oscillates at the frequency set by crystal Y110. Internal countdown dividers at the F/2 and F/4 outputs provide the clock frequencies used in the instrument. Schmitt inverter U180F inverts and buffers the F/2 signal to the Microprocessor. The inductor L110 prevents oscillation at a harmonic or subharmonic frequency
of the crystal.

Power-Up Reset

The Power-Up Reset stage consists of voltage sensor U182. This IC compares an internally-generated voltage reference to the level across a charging capacitor. When power is applied, the $\overline{RESET}$ level to the Microprocessor will be LO until external capacitor C180 charges to the internal reference level, at which time the reset is removed. This time delay ensures that all power supplies have had time to stabilize before processor operation begins.

LED Scan

The LED Scan circuit consists of 14-bit counter U115 that divides the 1.2288 MHz signal from the Microprocessor Clock stage down to the 150 Hz and 75 Hz signals used to sequence the LED Driver circuitry (diagram 3). In addition, the 150 Hz signal produces a microprocessor interrupt request used to update the various time-dependant functions at a known realtime rate.

Interrupt Logic

The Interrupt Logic provides the interface for handling interrupt requests to the microprocessor from various peripheral circuits. The processor, upon detecting the presence of an interrupt request, will branch from its normal program execution to an interrupt handling routine that determines which circuit requires servicing, and then performs the required servicing operations.

Microprocessor interrupt requests may be generated by (1)the real-time clock (U115 and U180A), (2)the Acquisition circuitry (diagram 12) when in ROLL mode, and (3) the optional GPIB circuitry (if present). GPIB interrupt requests are detected by U190A, and U190C applies a LO $\overline{INT}$ (interrupt) to pin 16 of the microprocessor. The processor generates a LO $\overline{IORQ}$ (I/O requested) signal to U170 and enables the Status Buffer's number "2" buffers. The LO $\overline{GPIBINT}$ (GPIB interrupt request) is buffered through U170 to data bus line D3, where the processor may read it. This LO bit defines the GPIB as the requestor and the processor branches to a GPIB interrupt handler routine. When the GPIB circuit recognizes that it is being serviced, it will remove its interrupt request. Normal processor operation will resume when servicing is complete.

The other two interrupts, realtime (150 Hz) and roll mode ($\overline{ROLLINT}$), are mutually exclusive and are selectable by the microprocessor. For normal (non-roll) operation, the processor will place a LO on data bus line D4 and generate an $\overline{OPTBNK}$ (option bank) pulse via the address decode circuitry, clocking a LO to the Q output of U130B. This LO is applied to U190B, disabling the roll interrupt path and forcing the reset of U130A HI (if not already HI). The rising edge of the free-running 150 Hz timing signal clocks the LO at the data input of 130A to its Q output, generating an interrupt to the processor (via U190A and U190C).

The processor checks the Status Buffer as described earlier and determines that this is a $\overline{TIMER}$ interrupt. The processor generates an $\overline{INTACK}$ (interrupt acknowledge) pulse, resetting U130A to remove the interrupt request and branches to the realtime service routine. When the realtime servicing is complete, the processor returns to normal program execution. Each sucessive 150 Hz clock generates another interrupt and the realtime service routine is executed again.

For roll displays, the processor will clock a HI into U130B instead of the LO used for generating timer interrupts. The resulting HI at the Q output of U130B pulls the clock input of U130A HI through CR132 and holds it HI, in spite of the 150 Hz timer clock signal. The HI is also applied to pin 5 of U190B and enables the roll interrupt ($\overline{ROLLINT}$) path.

When a $\overline{ROLLINT}$ pulse is generated by the Acquisition circuitry (diagram 12), a LO reset pulse will be applied to U130A, resetting it's Q output LO. This produces an interrupt to the processor (via U190A and U190C) and the processor will branch to its interrupt-handling routine. The processor reads the Status Buffer, determines that a roll

interrupt has occured, issues an interrupt acknowledge ($\overline{\text{INTACK}}$ from Address Decode, diagram 2), and branches to the roll-interrupt handler routine. In roll mode, this interrupt will be generated each time a data point is acquired.

ADDRESS DECODER AND MEMORY ◇2

The Address Decoder (diagram 2) generates enabling signals and strobes that allow the Microprocessor to control various devices and circuit functions. The Memory stage provides the permanent and temporary storage locations for data used by the Microprocessor in executing its control functions.

Address Decoder

The Address Decoder stage, comprised of U500, U510, U520, U530, U540D, and U550, generates strobes and enables for controlling devices and circuit functions by decoding the various bits of the Address bus. Table 3-1 illustrates address decoding by this stage.

Inverting AND gate U540D decodes address bit A15 for enabling U200 (ROM0). Whenever A15 is LO (lower 32 k of address space) and the $\overline{\text{RD}}$ line from the Microprocessor is LO, U200 is enabled and data may be read from the device.

The 2-line to 4-line decoders U500A, U500B, U510A, and U510B and the 3-line to 8-line decoders U520 and U530 decode the 10 MSBs of the address bus to generate the other enables and strobes illustrated in Table 3-1. The outputs from U530 will only be generated when a $\overline{\text{WR}}$ (write) enable from the Microprocessor is present.

The OR gates of U550 allow the 3 LSBs of the address bus to address one bit in the Attenuator Register (diagram 4) whenever address block CE00-CFFF is decoded (by pin 7 of U510A). The data bit DM0 from the processor data bus is applied to the register's input via U550C and will be written to the register when an address between CFC0 and CFFF is decoded by pin 7 of U530 ($\overline{\text{ATT}}$ is generated). See Attenuator Register description for further information.

Memory

The Memory stage consists of ROMs (read-only memory) U200 and U220 and RAM (random-access memory) U300.

The ROMs contain the firmware (operating instructions) used to control processor (and thus oscilloscope) operation. Addresses falling within the lower 48k-bytes of addressable space will enable data to be read from either U200 or U220 (see Table 3-1) when enabled by a LO $\overline{\text{RD}}$ (read) signal from the Microprocessor.

The RAM IC, U300, provides 8k-bytes of temporary storage of transient processor data and acquired waveform data points. Of these 8k-bytes, the lower 4k-bytes are used for the transient data storage area for processor functions. The upper 4k-bytes are used to store CH 1 and CH 2 data points for two acquired (and "STORED") waveforms. Reading and writing of addressed RAM locations is controlled by the $\overline{\text{RD}}$ (read) and $\overline{\text{WR}}$ (write) enables from the Microprocessor respectively.

The two remaining chip enables (CE1 and CE2) are routed to an edge card connector and are jumpered (or left unjumpered) depending on whether the instrument contains the RAM expansion option board. Without the option board, the address-decoded $\overline{\text{SYS}}$ (system RAM) enable is jumpered to the $\overline{\text{SYSB}}$ line and controls the CE1 enable while the CE2 enable is permantently enabled by jumpering the $+5\ V_{B0}$ line to the $+5\ V_D$ supply line. When instrument power is turned off, the contents of the RAM are lost.

With the "Extended Memory, Battery Backup and GPIB" option board (diagram 16) installed, the CE1 and CE2 enables are controlled by circuitry on the option board. The CE2 enable (and more importantly, U300's Vcc supply pin) is connected to a switched battery supply circuit on the option board that maintains power to the RAM chip with the power switch off. The CE1 enable operates in the normal fashion (controlled by $\overline{\text{SYS}}$) as long as normal instrument power is applied, but when the power switch is turned off (detected by circuitry on the option board), the $\overline{\text{SYSB}}$ enable is removed before the instrument power supplies decay below nornal operating levels. This early disabling prevents the contents of the RAM from being altered by unpredictable operation of the other oscilloscope circuitry (especially the processor) as their power supplies go out of limits. The Battery Backup and the early disabling allow the setup data (instrument configuration) and stored waveform data to be preserved with instrument power off.

KEYBOARD AND INTERFACE ◇3

The Keyboard and Interface (diagram 3) is the operator's means of controlling the user-selectable oscilloscope functions. Along with the crt, it provides visual feedback to the operator about the present operating state of the instrument.

Table 3-1
336 Address Decoding

Address Range	Control Signal	Decoding/Generating Device
0000-07FF	$\overline{\text{ROM0}}$	U540D
8000-BFFF	$\overline{\text{ROM2}}$	U500B
C000-CBFF	UNUSED	U510B and U510A
CC00-CC3F	$\overline{\text{RDACQ}}$	U520
CC40-CC7F	$\overline{\text{WFMCTRL}}$	U520
CC40-CC4F	$\overline{\text{DISMD}}$	U130A
CC50-CC5F	$\overline{\text{TBD}}$	U785A
CC60-CC6F	$\overline{\text{LO}}$	U785A
CC70-CC7F	$\overline{\text{ARM}}$	U785A
CC80-CCBF	$\overline{\text{OPTBNK}}$	U520
CCC0-CCFF	$\overline{\text{H-V MODE CONT}}$	U520
CD00-CD3F	$\overline{\text{TALK CONT}}$	U520
CD40-CD7F	$\overline{\text{INTACK}}$	U520
CD80-CDBF	$\overline{\text{RDDATA}}$	U520
CDC0-CDFF	$\overline{\text{KEYCONT}}$	U520
CDC0-CDC3	$\overline{\text{LC}}$	U100A
CDC4-CDC7	$\overline{\text{LED}}$	U100A
CDC8-CDCB	$\overline{\text{SW}}$	U100A
CDCC-CDFF	UNUSED	U100A
CE00-CE3F	$\overline{\text{TSOURCE}}$	U520
CE00	V/$\overline{\text{H}}$ SYNC	U620—This a data register. Data on DD0 is written to the addressed location. Seven overlays of this space exist up to address CE3F.
CE01	AUTO	
CE02	NC	
CE03	RUNS AFT DLY	
CE04	TV ENABLE	
CE05	$\overline{\text{HF REJ}}$	
CE06	$\overline{\text{LF REJ}}$	
CE07	$\overline{\text{DC}}$	

Table 3-1 (cont)

Address Range	Control Signal	Decoding/Generating Device
CE40-CE7F	$\overline{\text{TCOUPLE}}$	U520
CE40	INT	U600—This is a data register. Data on DD0 is written to the addressed location. Seven overlays of this space exist up to address CE3F.
CE41	EXT	
CE42	EXT(÷)10	
CE43	STORAGE INTENSITY	
CE44	$\overline{\text{LINE TRIG}}$	
CE45	$\overline{\text{CH2 TRIG}}$	
CE46	UNUSED	
CE47	$\overline{\text{CH1 TRIG}}$	
CE80-CEBF	$\overline{\text{SWP HO LATCH}}$	U520
CE80	$\overline{\text{RESET}}$	U140—This is a data register. Data on DD0 is written to the addressed location. Seven overlays of this space exist up to address CEBF.
CE81	HOLDOFF CHANGE	
CE82	VAR HOLDOFF SEL	
CE83	$\overline{\text{VAR SWP SELECT}}$	
CE84	LOCKOUT	
CE85	$\overline{\text{AUTO}}$	
CE86	HO TIMING 1	
CE87	HO TIMING 2	
CEC0-CEFF	UNUSED	U530
CF00-CF3F	$\overline{\text{PREAMP}}$	U520
CF00	CH1(divide)4	U430—This is a data register. Data on DD0 is written to the addressed location. Seven overlays of this space exist up to address CF3F
CF01	CH1(divide)1	
CF02	CH1(divide)2	
CF03	CH2(divide)1	
CF04	CH2(divide)2	
CF05	CH2(divide)4	
CF06	CH2 INVERT	
CF07	CH2 NORM	

Table 3-1 (cont)

Address Range	Control Signal	Decoding/Generating Device
CF40-CF7F	$\overline{\text{SWP CONTROL LATCH}}$	U520
CF40	B TIMING CAP 2	U120—This is a data register. Data on DD0 is written to the addressed location. Seven overlays of this space exist up to address CF7F.
CF41	B TIMING CAP 1	
CF42	A TIMING CAP 2	
CF43	A TIMING CAP 1	
CF44	$\overline{\text{RUNS AFTER DELAY}}$	
CF45	$\overline{\text{TRIG AFTER DELAY}}$	
CF46	SINGLE SWP	
CF47	UNUSED	
CF80-CFBF	$\overline{\text{TIMING CURRENT LATCH}}$	U520
CF80	B SEL 4	U100—This is a data register. Data on DD0 is written to the addressed location. Seven overlays of this space exist up to address CFBF.
CF81	B SEL 2	
CF82	B SEL 1	
CF83	UNUSED	
CF84	A SEL 1	
CF85	A SEL 2	
CF86	A SEL 4	
CF87	UNUSED	
CFC0-CFFF	$\overline{\text{ATT}}$	U520
CFC0	$\overline{\text{CH2 GND}}$	U50 *—This is a data register. Data on DD0 is written to the addressed location. Seven overlays of this space exist up to address CFFF.
CFC1	$\overline{\text{CH1 GND}}$	
CFC2	$\overline{\text{CH2 X10}}$	
CFC3	$\overline{\text{CH1 X100}}$	
CFC4	CH1 AC/$\overline{\text{DC}}$	
CFC5	CH2 AC/$\overline{\text{DC}}$	
CFC6	$\overline{\text{CH2}}$ X100	
CFC7	$\overline{\text{CH1}}$ X10	
D000-D7FF	$\overline{\text{WRDISP}}$	U510B
D800-DFFF	$\overline{\text{OPTRAM}}$	U510B
E000-FFFF	$\overline{\text{SYS}}$	U500A

***NOTE: These outputs are inverted from the levels loaded into the register.**

Switch Matrix

The operator selects oscilloscope operating mode by pressing or turning the various switches in the Switch Matrix. The switches are arranged in a seven-row by seven-column matrix and are read as explained in the Switch Scanning description (following). The diodes associated with each switch prevent ambiguous data and/or damage to components when multiple switch closures are present.

Switch Scanning

The Switch Scanning stage is made up of U100A, U120, U220, and the associated components and allows the Miroprocessor to detect and interpret closures of the front-panel switches. To read the switches, the Microprocessor sequentially sets each column of the matrix LO (by itself) and reads the resulting closure data from the data bus. The processor uses the combination of the column selected and the closure data read back for that column to determine which switch(es) is closed.

To set the individual columns of the Switch Matrix LO, the Microprocessor "writes" data to a location between CDC0 and CDC3. This address range causes the Address Decoder to generate a LO $\overline{\text{KEYCONT}}$ (keyboard control) enable to decoder U100A. Address bits A2 and A3 are decoded and produce a LO $\overline{\text{LC}}$ (load column) enable to the latched decoder U220. The lower 3 bits of the data byte (D0-D2) are used to select the desired output and cause it (and it alone) to go LO. The $\overline{\text{LC}}$ enable is removed when the address goes away but, because the select data is latched into U220, the LO column select remains on.

With the column selected as described, the processor then reads the data from a location between CDC8 and CDCB. This address causes the Address Decoder to enable U100A with $\overline{\text{KEYCONT}}$, and address bits A2 and A3 are decoded to produce the $\overline{\text{SW}}$ (switch) enable to tristate buffer U120. Any closed switch on the selected column line will pull its associated row line LO. The data byte read by the processor is then correlated with the column select data to identify each closed switch.

LED Matrix

The front-panel LEDs provide visual feedback to the operator about oscilloscope operating mode. The LEDs are arranged in a 4 x 4 matrix and are used to backlight selected switch functions.

LED Driver

The LED Driver stage provides the LED selection function and the current drive required to illuminate the LEDs (used to backlight selected switches as visual feedback to the operator).

To select which LEDs will be illuminated, the Microprocessor writes four bytes of data to U200. U200 is a 4-word by 4-bit RAM with independent read and write address lines. Writing data to address locations CDC4 through CDC7 will cause the Address Decoder to enable U100A with a LO $\overline{\text{KEYCONT}}$ signal and it will generate the LO $\overline{\text{LED}}$ signal that "write enables" U200. With U200 write enabled, the two LSBs of the address bus, A0 and A1, select one of the four locations in the RAM. The four LSBs of the data bus (D0-D3), defining which LEDs of the corresponding row should be illuminated, are written to the addressed location. This occurs four times to define the LED states in each of the four rows within the LED Matrix, a HI bit being written for each LED that should be illuminated.

The two free-running clocks (75 Hz and 150 Hz) applied to U200's read address pins (RA0 and RA1) cause the RAM to continuously cycle through its four locations, outputting the four data words defining which LEDs to illuminate. At the same time, the same two clocks cause U100B to continuously cycle a LO through each of its four outputs, enabling one row of the LED Matrix. In this way, the four data words each correspond to one of the four rows. A HI bit in the data word from U200 sources current through the LED associated with the selected row line. The complete process (scanning four rows) occurs at a fast enough rate (75 Hz) to prevent visible flicker of the LEDs.

Front-Panel Potentiometers

The Front-Panel Potentiometers provide operator control of some of the oscilloscope's analog-type functions. Those controls on the top-right corner of the diagram merely provide a variable dc voltage to the circuits they control.

The A TRIG LEVEL and B TRIG LEVEL potentiometers, shown at the top-left corner of the diagram, operate with constant voltages applied to their ends in normal trigger operation; however, when T (trigger) MODE AUTO is being used, the dc levels of the Trigger signal's positive and negative peaks are applied to the ends of the potentiometers. This spreads the active range of the trigger level controls over the range of the trigger signal amplitude.

CH 1 AND CH 2 ATTENUATORS ④

The CH 1 and CH 2 Attenuators (diagram 4) allow the operator to select various vertical deflection and coupling factors. The Microprocessor reads the settings of the front-panel VOLTS/DIV and input coupling switches and then digitally switches relays controlling the signal attenuation factors and coupling mode. The CH 1 and CH 2 Attenuators are identical; therefore, only the CH 1 Attenuator will be described.

CH 1 Attenuator

The CH 1 Attenuator routes the input signal through a series of reed relays and, depending on the path, determines input coupling mode and attenuation factor. The relays are driven by the inverters within U10 and U20 of the Attenuator Register and Buffer Stage and are closed when the corresponding buffer output is LO.

With relay contact S3 open, the input signal is ac coupled to the rest of the attenuator through capacitor C3. Closing relay S3 bypasses C3 and the signal coupling is dc.

Dual-contact relays K10 and K4 are controlled by complementary signals CH1 100X and $\overline{\text{CH1 100X}}$, and only one set of contacts may be closed at any time. If the Microprocessor determines that an 100X attenuation factor is required, the $\overline{\text{CH1 100X}}$ line will be set LO, closing contacts S10A and S10B. At the same time, U10 inverts the $\overline{\text{CH1 100X}}$ signal and applies a HI CH1 100X signal to relay K4, opening its contacts. Closing relay contacts S10A and S10B places a frequency-compensated ÷ 100 resistive divider in series with the input signal, reducing the amplitude of the output signal by a factor of 100.

If the 100X attenuation is not needed ($\overline{\text{CH1 100X}}$ HI), contacts S10A and S10B will remain open while those of K4 (A and B) will be closed. This passes the input signal on to a similar 10X attenuation network controlled by relays K22 and K20. For a 10X attenuation factor, contacts S22A and S22B are closed while S20A and S20B remain open. For a 1X (no attenuation) factor, contacts S4A, S4B, S20A, and S20B are all closed, to pass the unattenuated signal on to the output buffer comprised of Q40A, Q40B, and their associated components.

The attenuated (or unattenuated) signal is applied across R30 and develops a voltage that drives the FET-buffered output. Normal signal drive for the buffer is via R32, C32, and R34 and drives the gate of Q40A configured as a source follower. Closing relay contact S31 grounds the drive signal for the buffer and provides a zero-voltage reference trace on the crt display.

FETs Q40A and Q40B form a source-follower buffer, providing a high input impedance and a high current output. Transistor Q40B and R48 are configured as a constant current source for the rest of the buffer. Since the FETs are closely matched and since nearly identical currents are flowing in them, the voltage drop from the gate of Q40A to the output will match that from the gate of Q40B to the −5 V supply (0 volt drop). The signal output (at the drain of Q40B) follows the input signal at the gate of Q40A.

Attenuator Register and Buffer

The Attenuator Register and Buffer provides storage of the attenuator control data and buffers the data to the attenuator relays to hold the appropriate relays closed. The Microprocessor sets up each of the 8 bits in the Attenuator Register U50 by writing 1 bit of data (via data bus line DD0) to each of the eight locations between CFC0 and CFC7 (see address decoding, Table 3-1). Addresses falling within this range cause the Address Decoder to enable U50 with a LO $\overline{\text{ATT}}$ (attenuator) enable. The lower 3 bits of the address (DA0, DA1, and DA2) are decoded by U50 and select one of the 8-bit locations within the register for storage of the $\overline{\text{DD0}}$ data. After each location is set to its proper level, the $\overline{\text{ATT}}$ enable goes HI and the 8 outputs at Q0-Q7 are applied to buffers U10 and U20. These buffers invert the levels of the data stored into register U50 and provide proper drive for the relays in the attenuator stages. A HI bit loaded into a specific location in register U50 will be inverted by U10 or U20 and will close the associated relay contact(s).

Probe Encoding

The Probe Encoding stages detect use of 10X encoded probes and signal the Microprocessor of their use.

With unencoded probes, the transistors within U250 and U260 are biased on by the resistors at pin 4 tied to +5 volts. This biasing turns the transistors on and pulls their collectors LO. These LOs are applied to a Microprocessor Status Buffer where they can be read. If a 10X probe is in use, the base of the associated Probe-Encoding IC is pulled LO through the resistor at pin 6 and the probe's encoding pin. This turns the output transistor off and the status bit to the Microprocessor goes HI, signaling an encoded probe.

CH 1 AND CH 2 VERTICAL PREAMPS ◇5

The CH 1 and CH 2 Vertical Preamps (diagram 5) provide selectable- and variable-gain amplification of the attenuated CH 1 and CH 2 input signals. The gain factors of these preamplifiers are set by the Microprocessor after reading the front panel and, along with the Microprocessor-selectable attenuation factors, allow the operator to select the vertical deflection factors.

Preamp Control Register

The Preamp Control Register stores the preamplifier setup data from the Microprocessor and generates the drive signals that select preamplifier gain factors and (for CH 2) operating mode.

The Microprocessor reads the front-panel vertical deflection switches and determines what the preamplifier gain should be. It writes data from U430's DD0 input to the output addressed by the DA0, DA1, and DA2 inputs. A HI output closes the corresponding switch in either U174 or U474 and enables that preamplifier function. The address decoding used to set the preamplifier functions is shown in Table 3-1.

CH 1 Preamp

Transistor array U100 and its associated components form a paraphase amplifier with variable gain capability. With the CH 1 VAR signal from the front panel in its detent position (+5 V), transistors Q100A and Q100D are biased on hard and Q100C and Q100E are nearly reverse biased. The attenuated CH 1 signal applied to the base of Q100B varies the signal current to the emitter-coupled transistor pair U100A-U100C, and the majority of the signal current flows through U100A. The varying current is injected into the emitter of Q144 and develops an output signal across R160A.

The other side of the input stage is composed of U100D, U100E, U100F, and their associated components. Bias applied to U100F from the VAR BALANCE adjustment is used to match quiescent currents in each side of the paraphase amplifier. Phase splitting occurs because the signal present at the emitter of U100B is coupled to the emitter of U100F and varies the transistor's base-emitter bias (and thus collector current). The result is two current signals 180° out of phase derived from the single signal input (at the base of U100A). Resistors R104, R105, and R108 set the gain at the preamplifier. Resistor R108 is adjusted to match the CH 1 gain to that of CH 2. Resistor R102 and capacitor C102 are used to adjust the frequency response of the preamplifier.

As the CH 1 VAR control is moved from its detented position, the bias on U100A and U100D is reduced (and effective bias on U100C and U100E increases). The signal currents developed by U100B and U100F are proportionally split through their respective emitter-coupled pairs (at their collectors) depending on the relative bias voltages on the emitter-coupled transistors. Since the collectors of U100C and U100E are cross-coupled to the opposite side of the amplifier, the out-of-phase signal currents through them are summed with the normal signal currents, reducing the amplitude of the output signal. Advancing the CH 1 VAR control further from detent further reduces signal amplitude.

These summed signal currents are level-shifted by Q144 and Q156 and applied to a transistor gain switch. Depending on the front-panel settings detected by the Microprocessor, one of the gain control lines (CH1 ÷ 1, CH1 ÷ 2, or CH1 ÷ 4) will be pulled HI. The HI signal turns on two switching transistors, one in each leg of the amplifier, and injects the signal currents into the gain-setting network composed of R160A-G.

The drive signals resulting at the bases of Q190 and Q230 depend on the Thevenin input impedance at the point of signal injection and the voltage divider from that point to the bases of the output transistors. Figure 3-2 illustrates the various signal attenuation schemes. Since the signal currents in the two legs oppose each other, the midpoint of R160D may be thought of as a virtual signal ground when calculating the Thevenin's input impedance for the current signal. As shown in the figure, the resulting signals have relative attenuation ratios of 1, 2, and 4.

The resulting voltage signals across R160A and R160G drive the bases of output transistors Q190 and Q230 respectively. These transistors produce voltage gain and drive the Vertical Channel Switch stage (diagram 6). The RC network between the emitters of Q190 and Q230 provides frequency compensation for the preamplifier.

The voltage from the CH 1 POSITION control is buffered by U220A and provides a variable current that is summed with the bias current of Q230 (via R220). This variable current shifts the dc levels at the outputs and allows the operator to vertically position the trace on the crt. The CH 1 POSITION CENTER adjustment R164 provides a similar bias current to the base of Q190 and is set to center the trace on the crt (with the position control at midrange).

Transistors U160D, U170D, and their associated components comprise a trigger-pickoff amplifier that buffers the CH 1 signal to the trigger circuit. When the X-Y mode is used, the pickoff signal is applied to the horizontal amplifier to provide the horizontal deflection signal. The X-Y POSITION control R217 is set at the time of calibration and provides an offset current used to horizontally center X-Y displays.

CH 2 Preamp

The CH 2 Preamp is nearly identical to the CH 1 Preamp described above, the major difference being that the paraphase input section may be switched to produce either normal or inverted outputs. The two signals, CH 2 NORM and CH 2 INVERT, from the Preamp Control Register determine the preamplifier's operating mode.

The CH 2 VAR level from the front panel is connected through one (but not both) of these control lines. When connected to the CH 2 NORM line, the amplifier's configuration is identical to that for CH 1 and operates in the same manner.

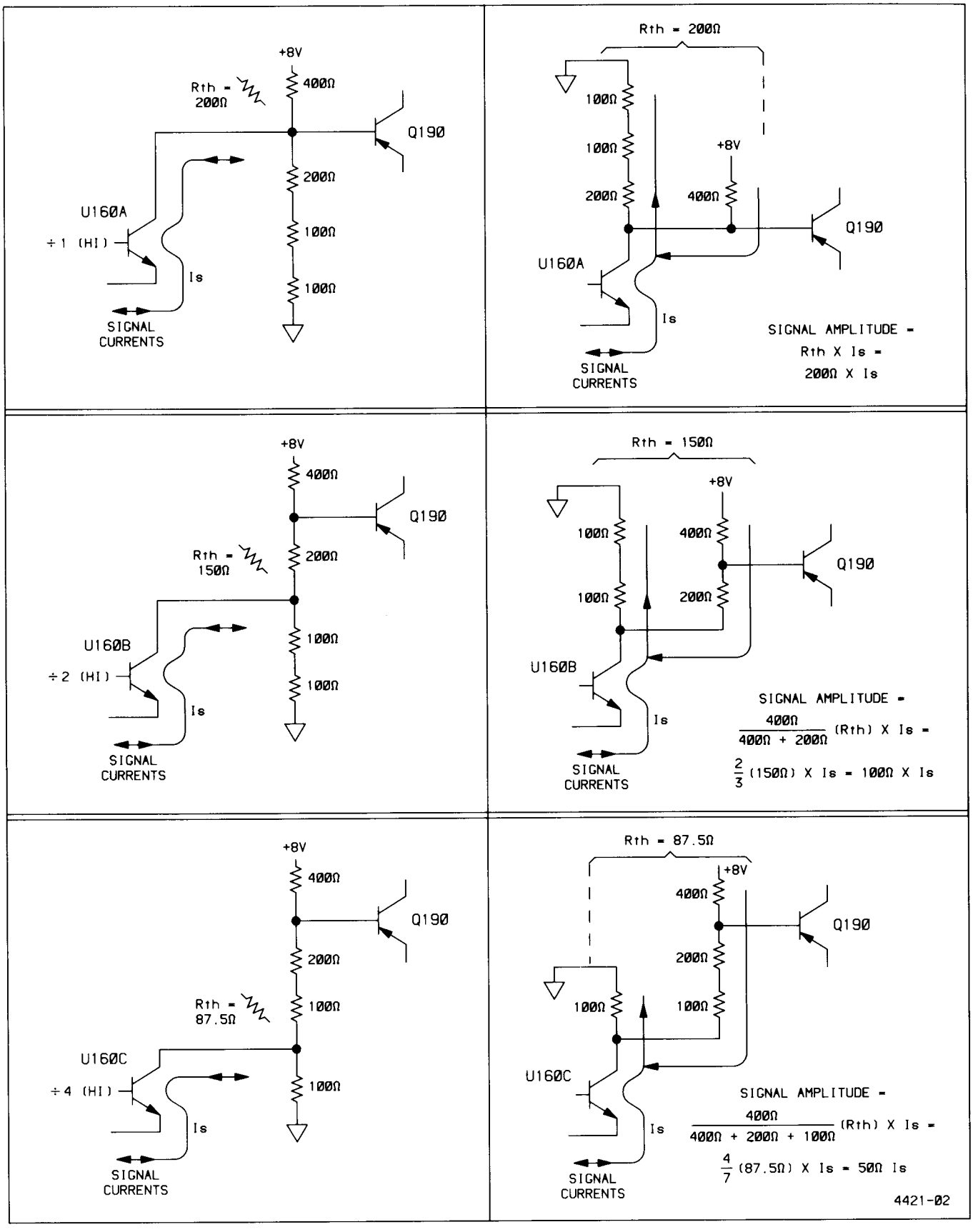


Figure 3-2. Preamp Attenuation Schemes.

When the variable voltage is connected to the CH 2 VERT line, the opposite side of the emitter-coupled pairs is biased more positively. These transistors' outputs now have the dominant effect in determining signal polarity. The other circuit operations remain the same.

VERTICAL SWITCHING AND OUTPUT AMPLIFIER ◈6

The Vertical Channel Switch (diagram 6) selects the vertical signal source, while the Vertical Output Amplifier raises the selected signal to the levels required to drive the vertical deflection plates of the crt. The Storage Channel Switch is used to select the stored waveform and readout data for deflection of the crt beam.

Vertical Channel Switch

The Vertical Channel Switch consists of three nearly identical transistor switches used to select the CH 1, CH 2, or Trigger View signals for amplification. Since the switches are so similar, only the Trigger View switch circuitry will be explained.

The input signals applied to the bases of U740B and U740E cause proportional currents to be drawn through the resistive network at their emitters. These varying currents are applied to the emitter-coupled pairs at their collectors and are routed through whichever transistor is turned on. The bases of U740F and U740D are held at +1 V by the resistive divider R766-R768. If the Trigger View Sel signal is LO (trigger view deselected), the bases of U740A and U740C are lower than those of U740F and U740D, so U740F and U740D are the transistors that are turned on. The two currents are summed together and cancel each other (nearly). Any remaining current signal is eliminated by injecting the current into both legs of the output amplifier via R734 and R736.

When selection of the Trigger View signal is desired, the Vertical Mode Control (diagram 17) sets the Trigger View Sel line HI. This turns U740A and U740C on instead of U740F and U740D. The signal currents now pass through U740A and U740C and are applied to the inputs of the Output Amplifier (bases of Q800 and Q820 respectively).

Variable capacitor C744, along with resistor R746, provides frequency compensation of the input signal. These components are not present in the CH 1 and CH 2 switches.

Vertical Output Amplifier

The Vertical Output Amplifier raises the selected signal from the Vertical Channel Switch to the proper level for driving the vertical deflection plates of the crt.

The out-of-phase signals from the Vertical Channel Switch are applied to the bases of Q800 and Q820. These signals are inverted and applied to emitter-followers Q830 and Q840, which drive the delay line. Frequency compensation is provided by the RC network between the emitters of Q800 and Q820. Diodes CR834 and CR836 limit the amplitude of differential drive signals to the delay line.

The differential signal to the rest of the output amplifier is delayed by the delay line to allow viewing the trigger event on the crt.

Transistors Q60, Q70, Q90 and Q94 form a frequency-compensated gain stage that may be turned on or off by the Storage Channel Switch. This allows either the real-time signals or stored waveform and readout signals to control the vertical deflection of the crt beam. For display of real-time signals, diode CR74 is reverse biased, and proper emitter bias for Q60 and Q70 is established. The differential signals applied at their bases are amplified by a factor determined by the setting of R74 and are applied to the bases of transistors Q90 and Q94. The current outputs at the collectors of Q90 and Q94 are applied to the emitters of Q100 and Q110 respectively. The RC network between the collectors of Q90 and Q94 and the emitters of Q60 and Q70 provide frequency compensation of the stage.

If the real-time display is to be disabled for display of stored waveforms or readout data, transistors Q60 and Q70 are reverse biased by pulling their emitters HI via CR74, R64, and R66. This also reverse biases Q90 and Q94 and the real-time signal path is closed. The stored waveform or readout signals are applied to the following amplifier stage instead of the real-time signals, as explained in the Storage Channel Switch description.

The selected vertical deflection signals are applied to the feedback amplifier made up of Q100, Q110, Q140, Q152, and their associated components. The stage has a current gain of approximately 5, as determined by R140, R150, and R152.

Transistors Q142 and Q154 convert the differential current signals to deflection voltages for driving the crt's vertical deflection plates.

Storage Channel Switch

The Storage Channel Switch consists of Q56, Q102, Q108, Q112, and their associated components. This switch is used to disable the real-time signal path and inject the storage deflection signal into the vertical deflection system.

The switching action is performed by emitter-coupled pair Q56-Q112. The base of Q112 is biased around +2.5 V by R79 and R81. Resistor R56 modifies the bias point by adding hysteresis current to the node, so actual bias at the base is either +2 volts or +3 volts, depending on the level of the REAL signal from diagram 17. With the REAL signal HI, the base of Q56 is above the +3 volt bias level on the base of Q112. This turns Q56 off and Q112 on. With Q56 off, diode CR74 in the Vertical Output Amp is reverse biased and the real-time signal is passed through the amplifier in the normal manner. Since Q112 is on, the emitters of Q108 and Q102 are pulled HI, turning the STORAGE signal path off.

When the STORAGE information is to be displayed, the REAL signal goes LO. This turns Q56 on and Q112 off. With Q56 on, the emitters of Q60 and Q70 in the Vertical Output Amp are pulled HI via CR74, R64 and R66, reverse biasing the transistors. This reverse biases Q90 and Q94, causing them to go to high-impedance states.

Since Q112 is off, bias current for Q102 and Q108 is now supplied through R112, R104, and R108. These transistors form a paraphase amplifier and split the signal applied to the base of Q108 into two out-of-phase signals. These are applied to the output stage of the Vertical Output Amplifier from the collectors of Q102 and Q108. The Storage Wfm Position adjustment, R126, slightly varies the offset voltages and vertically positions the storage waveforms and readout displays on the crt.

Acquisition Pickoff

The Acquisition Pickoff stage consists of two emitter-follower transistors that buffer the differential signal voltages to the Acquisition circuitry (diagram 12). Pickoff is done prior to the delay line so the acquisition window will be directly related to the trigger event. Further information is given in the Acquisition descriptions.

TRIGGER SELECT ◇7

The Trigger Select circuit (diagram 7) allows the Miroprocessor to set the trigger source and trigger coupling modes. Data from the Microprocessor defining the trigger setup conditions is written to a control register that closes or opens various relays and analog switches to select the desired trigger.

Trigger Data Register

The Trigger Data Register consists of two 8-bit latches, U600 and U620. The trigger-control data from the DD0 data line is written to the desired control outputs when enabled by the Address Decoder. The three address bits DA0, DA1, and DA2 select one of the eight outputs of each IC, while the Address Decoder generates the IC enables that write the data to the latched output. The latched output bits are the levels that control trigger source and trigger coupling selection.

Internal Source

The Internal Source stage consists of three similar channel switches and an output buffer that has the ability to select either CH 1, CH 2, or LINE as the internal trigger source. The three switches are similar enough that only the CH 1 switch will be described.

In order to select one of the three internal trigger sources, the corresponding select bit from the Trigger Data Register is set LO while the other two bits are set HI. With the CH 1 select bit set LO, Q30 becomes forward biased and bias current for the differential amplifier Q10-Q20 is supplied from current source Q32. The differential CH 1 signal applied to the bases of Q10 and Q20 is converted to a single-ended signal at the collector of Q20. The signal level is raised a diode drop by CR96 to compensate for the base-emitter drop of emitter-follower Q100. This buffered output is applied to the Trigger Coupling stage and provides the trigger signal when internal source is selected. Operation of the Line Trigger switch Q80-Q90 is similar except that it has a single-ended input. Capacitor C74 couples the higher-frequency components of the frequency-modulated pulse train from the Line Trigger circuit (see that description) to the base of Q80 so that they may be common-mode rejected from the resulting output signal. Since only minimal coupling occurs at the line signal frequency, this signal will be amplified, resulting in a clean line trigger signal.

External Source

The External Source stage allows sweep triggering on a signal applied to the EXT TRIG bnc input connector. Selection of the external source is done by closing relay contacts under control of the Trigger Data Register.

The external trigger signal is applied to the EXT TRIG input J108 on the instrument side panel. The adjustable RC network provides frequency compensation of the signal. Depending on whether the unattenuated EXT signal or the EXT ÷ 10 signal should be the trigger source, either S100 or both S110 and S120 will be closed respectively. With S100 closed, the unattenuated trigger signal is applied to the Trigger Coupling stage. With both S110 and S120 closed, the

trigger signal is attenuated by a factor of 10 by the network between the relay contacts before application to the Trigger Coupling stage.

Trigger Coupling

The Trigger Coupling stage consists of U640, U650, Q160, Q170, the various switching relays, and their associated components and sets the coupling mode of the selected trigger signal.

Buffer U640 inverts and buffers the control signals from the Trigger Data Register to the current levels required to drive the various switching relays. A LO output from U640 will close the associated relay contact.

Closing relay contact S150 provides dc coupling of the selected trigger signal by bypassing the ac-coupling capacitor C150. With the contact open, the selected trigger signal is ac coupled via the capacitor.

The LF REJ and HF REJ functions are mutually-exclusive; i.e., only one of them may be active at any time. In order to use the LF REJ function, relay contact S160 will be open (LF REJ signal HI) and S170 will be closed (HF REJ signal LO). At the same time, the select signals to U650A and U650B turn transistors Q160 and Q170 on and off respectively. This places a high-pass (lf reject) filter (C160 and R160) in the trigger signal path and limits the low-frequency response of the trigger signal.

Selecting HF REJ coupling closes relay contact S160 (LF REJ is LO) and opens S170. At the same time, the select signals to U650A and U650B turn transistors Q160 and Q170 off and on respectively. This configuration bypasses C160 and places a low-pass (hf reject) filter (C170) in the signal path.

Trigger Buffer

The Trigger Buffer stage consists of FET source-follower Q180A and Q180B and an emitter-follower, Q190. The stage provides a high input impedance to the trigger signal and a low output impedance to drive the trigger-peak detector on diagram 8. Diode CR182 provides level shifting to offset the level shift through the base-emitter junction of Q190. Diode CR180 prevents the trigger signal input from overdriving the buffer in the negative direction (buffer configuration limits the positive swing), preventing component damage.

A AND B TRIGGERS AND TV SYNC SEPARATOR ◈8

The A and B Trigger circuits (diagram 8) generate trigger signals to the sweep control circuitry (diagram 9) to initiate sweeps when the proper triggering criteria is met and allow the operator to select triggering levels. The TV Sync Separator circuit separates the horizontal and vertical sync pulses from a composite video signal, allowing measurements to be made in those time domains.

Peak Detector

The Peak Detector U480 continuously monitors the trigger signal at its input (pin 7) and stores the dc levels of the signal peaks. These levels are output at pins 2 and 5 to the A and B Trigger Level circuits.

A and B Trigger Level

The A and B Trigger Level circuits set the associated triggering levels, depending on the settings of the front-panel A and B TRIG LEVEL controls. The circuits automatically set trigger slopes, depending on the controls' positions. The A and B Trigger Level circuits are nearly identical; therefore, only the A Trigger Level circuit will be described.

The front-panel A TRIG LEVEL control operates in two different modes, depending on whether the AUTO TRIGGER MODE is active or not. When the AUTO mode is in use, the detected peak values of the trigger signal are routed from the Peak Detector through the analog switches U400B and U400C to the buffers U420A and U420B. These resulting buffered peak levels are applied to either end of the A and B TRIG LEVEL controls (R480 and R490 on diagram 3) through R402 and R404. This limits the control range of the TRIG LEVEL controls between the positive and negative peak values of the trigger signal and the display is always automatically triggered.

When in NORM TRIGGER MODE, the AUTO select line to U400B and U400C is LO. This deselects the Peak Detector outputs and applies two fixed voltages to buffers U420A and U420B. The buffered output levels are applied to the TRIG LEVEL controls, which now operate between these fixed levels.

The variable level from the A TRIG LEVEL control is applied to U440B configured as a rectifier. Figure 3-3 illustrates the rectifying action of the stage.

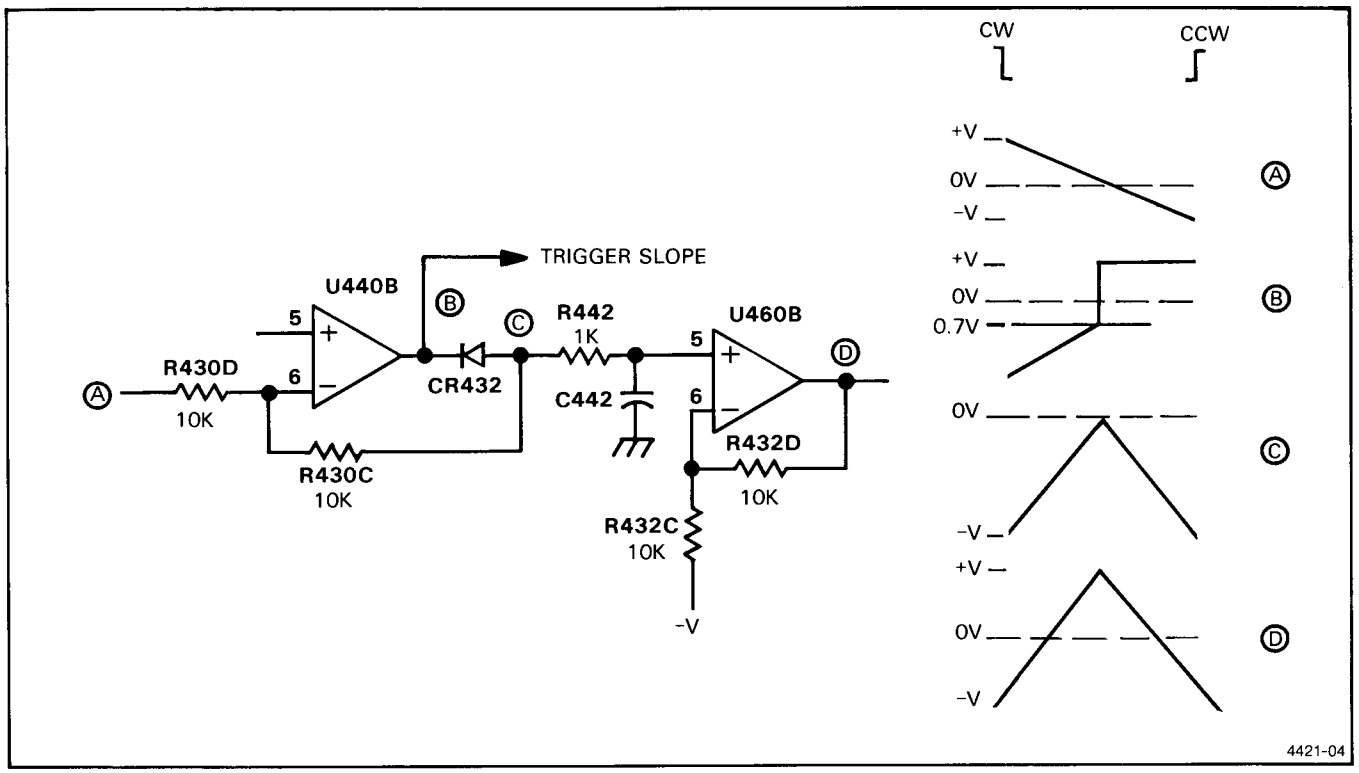


Figure 3-3. Rectifying action of Trigger Level Circuit.

The noninverting input of U440B is referenced to the level at the midpoint of the A TRIG LEVEL control by resistive divider R420C-R420D. With the control set clockwise from center, an input level positive with respect to this reference is applied to the inverting input, pin 6 of U440B. As long as the input is positive with respect to the reference, the operational amplifier acts as an inverting buffer and the output voltage complements the input voltage (both levels with respect to pin 5).

As the A TRIG LEVEL control moves counterclockwise through its center position, diode CR432 becomes reverse biased and U440B acts as a comparator. Output pin 7 goes HI, signaling the A Trigger Generator that the A Trigger Slope has changed. With CR432 reverse biased, the voltage from the A TRIG LEVEL control is applied directly to the following buffer stage through R430D and R430C.

Operational amplifier U460B and its associated components comprise a X2 buffer that converts the half-scale rectified control position information to cover the full range of the control.

A and B Trigger Level Comparators

The A and B Trigger Level Comparators compare the level of the input trigger signal to the levels set by their Trigger Level circuits and generate transitions at the crossing points. The A and B Trigger Level Comparators are identical, therefore only the A Trigger Level Comparator will be described.

Transistor Q244 is an adjustable constant-current source for the emitter-coupled comparator transistors Q240 and Q242. The input trigger signal is applied to the base of Q240 via R240A and is compared to the reference trigger level applied to the base of Q242. As the trigger signal goes more positive than the reference level, Q240 will turn on and Q242 will be turned off. The Trigger Crossing signal to U490A of the A Trigger Generator is pulled HI through R244 and CR242, indicating a positive-going crossing. As the trigger signal crosses the reference level going negative, transistor Q242 is turned off and Q240 turns on, pulling the Trigger Crossing signal LO.

A and B Trigger Generators

The A and B Trigger Generators generate the trigger signals to the Sweep Control logic (diagram 9) and provide the logic necessary to allow sweep triggering on either slope of the trigger signal. Since the A and B Trigger Generators are identical, only the A Trigger Generator will be explained.

The Trigger Crossing signal applied to U490A is inverted and applied to U494B via R480 and R494. Resistor R492 provides positive feedback around U494B and, along with R494, widens the switching window of U494B to eliminate false triggers associated with noise on the trigger signal. Adjusting R480 sets the trigger sensitivity.

The A Trigger Slope signal input to U494A determines whether sweep triggering will occur on the positive or negative crossing of the trigger signal. Changing the level of the A Trigger Slope line from LO to HI causes U494A to act as an inverter instead of a buffer. Since the A Gate Generator (diagram 9) responds to positive-going transitions, the signal inversion will switch the triggering point from the negative crossing point to the positive crossing point (negative slope to positive slope).

Gate U490A disables the normal triggering path through the gate when the TV ENABLE signal applied to pin 5 goes HI. This disabling allows the TV Trigger circuit to generate triggers via the output from U490D.

TV Trigger

When enabled, the TV Trigger stage will separate the horizontal and vertical sync pulses from a composite video signal for use as triggers.

With the TV ENABLE signal applied to pin 9 of U650C LO, the anodes of CR200 and CR216 are pulled HI through R620E. This pulls input pin 6 of U200A HI through CR200 and forces its output at pin 2 to a constant LO. Diode CR216 pulls the noninverting input of U200B HI (this is a current input, not voltage) and also forces its output HI. This is applied to U490C and U490D to disable their outputs. This is the disabled condition and does not allow any input signals to pass through the circuit.

With the TV ENABLE signal HI, −5 volts is applied to the anodes of CR200 and CR216, reverse biasing them. Input signals are ac coupled to U200A through C202. The stage provides a gain of approximately 10, and its ac-centered output is ac coupled to the following current amplifier.

Currents into pins 9 and 10 of U200B must be equal for the output of this amplifier to be stable. With CR216 reverse biased (TV Trigger enabled), the input reference current is established by R216. The current to the other input is provided via R212 and R214, however, by themselves, these resistors would source excessive current, forcing the output LO. A portion of the current is sinked through CR210 to the output until a balance is achieved.

When a signal is applied to the amplifier via R210, current is added to or subtracted from the node at the anode of CR210. In order to maintain the current balance at the inputs of U200B, the output voltage at pin 14 will move to change the current sourced to the node via R212. The resulting output voltages across R224 and R226 contain the horizontal and vertical sync components of the composite video signals.

Analog switch U400A is used to select either the vertical or horizontal sync pulse for A triggering and is selected by the V/$\overline{H}$ (vertical/horizontal) select signal from the Trigger Data Register on diagram 7.

SWEEP CONTROL ◈9

The Sweep Control circuit (diagram 9) generates the A and B GATE signals to initiate sweeps, depending on control levels set by the Microprocessor and several interactive sweep-dependent signals.

Sweep Control

The majority of sweep control functions are performed by the specialized sweep control IC, U200. These functions include sweep enabling/disabling, holdoff control, and auto trigger generation.

Control signals from the Sweep Control Latch (diagram 10) are set by the microprocessor to determine sweep operation. The sweep lockout signal (at pin 18) when HI disables all sweep functions by setting U200's SWEEP $\overline{\text{DISABLE}}$ output HI. This reverse biases U240D and holds the $\overline{\text{AGATE}}$ output of U680 HI. When the lockout signal is LO, the sweep mode is dependent on which of the mode control inputs is asserted (SINGLE SWEEP or $\overline{\text{AUTO}}$). With neither of these controls asserted, triggering mode will be normal.

In the SINGLE MODE, a single trace is displayed when the predefined triggering conditions are met. The RESET START pin resets the single sweep function and the RESET READY line tells the microprocessor when the single sweep function is ready (so the processor can set the indicator LED).

AUTO TRIGGER MODE mode freeruns the sweep in the absence of a sweep trigger and allows the baseline trace to be displayed. Each sweep, when triggered, produces an $\overline{\text{AGATE}}$ signal to pin 2. When $\overline{\text{AGATE}}$ is detected, the AUTO RC capacitor at pin 6 is discharged. If a normal

sweep trigger doesn't occur within approximately 100 ms, the capacitor C200 charges above the input threshold level through R200 to generate an automatic trigger at the (−)TD AUTO output. This auto trigger causes the sweep to run, even through a trigger event did not occur, and discharges the capacitor. The cycle will repeat itself, continually generating sweeps, until normal triggers resume.

In the NORM Trigger MODE, the auto rc does not affect circuit operation and sweeps will only occur when proper trigger events are present.

Emitter-coupled transistor pair U600C-U600D detects the end of each A Sweep and, initiates a delay period between sweeps known as holdoff. Holdoff provides for sweep retrace and, when Variable Holdoff times are used, allows stable display of some types of irregular waveforms. Once initiated by the HOLDOFF START signal at pin 16 of U200, the trigger gates are disabled by setting the SWEEP DISABLE signal at pin 17 HI until the HOLDOFF RC input signal charges through the preset threshold level. The HOLDOFF RC timing is explained in the following description.

Holdoff

The Holdoff circuit provides selectable rc timing elements for timing the length of the holdoff period, depending on sweep rate and setting of the front-panel VAR HOLDOFF control.

With the VAR HOLDOFF control in its detented position, the microprocessor will set the control bit to pin 11 of U300C LO, applying a ground level to the bias divider for Q300. This configures Q300 as a constant current source, current depending on microprocessor selection of either R300 or R302 (via U300A). This constant-current linearly charges the selected holdoff capacitor(s) to the detection level required at pin 8 of U200 and signals the end of the holdoff period. Capacitor C270 is always selected while U240A and U240B are used to select C274 and C272 respectively, depending on microprocessor control data. Once the holdoff period ends, the next trigger event will initiate a sweep and the selected holdoff capacitors will be discharged. The capacitors are held in their discharged state until the end of sweep is detected by U600A and U600C, then the charging begins again to time the next holdoff period.

With the VAR HOLDOFF control out of detent, the Microprocessor will set the select level to pin 11 of U300C HI (via the Sweep Control Latch). This connects the output of inverting-amplifier U320A to the bias network of current source Q300. Depending on the position of the front-panel control, the voltage at the output of U320A will vary between 0 V and +6 V and will vary the charging current (and thus charging time) through Q300.

A Gate Generator

The A Gate Generator produces the A sweep gate used to initiate the A sweep ramp. If the SWEEP DISABLE output from pin 17 of U200 is HI, a HI will be applied to the set input (pin 5) of U680. This disables the A GATE signal by holding the Q output HI (and the $\overline{Q}$ output LO) and prevents sweeps from occurring.

With pin 5 of U680 LO, the Q and $\overline{Q}$ outputs will toggle when a trigger is applied to the input at pin 6. When the trigger occurs, the AGATE output at pin 3 goes HI and the $\overline{\text{AGATE}}$ output at pin 2 goes LO. The LO $\overline{\text{AGATE}}$ level forward biases CR680 and turns Q600 on. With Q600 on, input pin 6 of U680 is held HI, ensuring that subsequent trigger events do not cause noise on the gate outputs. When the Sweep Control IC, U200, detects the end of sweep, the gate signals will be reset via the SWEEP DISABLE signal applied to pin 5 of U680 via U240D.

Transistor U620D and its associated components set the bias voltage on the base of Q432 at about +3.8 volts. The positive-going AGATE output from pin 3 of U680 is applied to the base of Q430 and is compared to this level. The A SWP GATE signal at the collector of Q432 follows the A GATE signal.

Transistor U240C allows the AUTO TRIG output from pin 4 of U200 to generate sweep gates when no other triggers are present. When the Sweep Control IC, U200, determines that normal triggering has not occurred within approximately 100 ms, it will set its AUTO TRIG output applied to the base of U240C HI. This turns the transistor on and pulls the base of Q430 HI, generating a sweep gate pulse to initiate a sweep.

B Gate Generator

The B Gate Generator, in conjunction with the Delay Comparator, produces the gates for B Triggered After Delay and B Run After Delay displays. These modes are mutually exclusive; i.e., only one mode may be active at any time.

Depending on which mode is to be used, either the $\overline{\text{TRIG AFT DLY}}$ or the $\overline{\text{RUN AFT DLY}}$ control lines to U640 will be set LO by the Microprocessor (or both HI to disable both functions for A sweeps). Whichever line is set LO will enable the Delay signal to clock the related flip-flop within U640 from its set state. Clocking U640B with the DELAY signal starts the RUN AFT DLY GATE and initiates the B sweep ramp. Transistor comparator U620A and U620B de-

tects the end of the B SWP ramp (at approximately +2.3 volts as set by R610 and R612) and sets the flip-flop once again. Setting the flip-flop terminates the RUN AFT DLY GATE.

Setting the $\overline{\text{TRIG AFT DLY}}$ line LO allows the DELAY signal from the Delay Comparator to clock flip-flop U640A from its set state and produces a LO enable signal to pin 12 of U680. This enables U680B to toggle and, on the next B TRIGGER pulse, a TRIG AFT DLY GATE is initiated. The B SWP ramp runs until transistors U620A and U620B detect that the sweep should end, setting the END B signal HI. This terminates the TRIG AFT DLY GATE.

The RUN AFT DLY GATE and TRIG AFT DLY GATES connect directly to the base of Q530. This transistor is emitter coupled to Q532 with its base biased at approximately +3.8 volts. These two transistors act as a switch that produce the SWP GATE signal.

Delay Comparator

The Delay Comparator generates the DELAY signal used for the TRIG AFT DLY and RUN AFT DLY modes. These modes generate B sweeps relative to the beginning of the A SWP ramp by detecting when the A sweep ramp crosses a user-definable threshold voltage.

Transistors U620E (configured as a diode) and U600E form a constant-current source for the voltage comparator U600A-U600B. The A SWP ramp voltage is applied to the base of U600A via R630 and is compared to the user-definable voltage applied to the base of U600B via R608. Resistor R626 provides switching hysteresis and ensures that the DELAY signal will be stable once set HI, in spite of any noise that may be present either on the A SWP ramp or the delay reference voltage. Transistor U620C is configured as an emitter follower and buffers the DELAY clock to the B Gate Generator.

A AND B SWEEP GENERATORS ◈10

The A and B Sweep Generators (diagram 10) produce the linear sweep ramps used to sweep the crt beam horizontally across the face of the crt. The ramps are generated by charging a selected timing capacitor with a constant current source. The resultant ramp is buffered to the horizontal preamp for amplification.

Sweep Control Latch

The Sweep Control Latch consists of U120 and U140 and stores the control data from the microprocessor used to set up the horizontal sweep modes. The TTL outputs drive transistor switches that select timing capacitors (for ramp timing and holdoff timing), sweep mode (single sweep, normal, B runs after delay, auto trigger, and sweep lockout), sweep holdoff charging resistors and sweep and holdoff variable controls.

Setup data from the Microprocessor is written from the DD0 line to the addressed output (see Table 3-1) on the falling edge of the enable to either U120 or U140. When the enable line returns HI, the data is latched at the output, holding the setup condition until once again changed by the Microprocessor.

Timing Current Latch

The Timing Current Latch consists of U100 and operates similarly to U120 and U140 of the Sweep Control stage. The latched outputs control timing current selection for the A and B sweeps as described in the A and B Current Source descriptions.

A and B Current Sources

The A and B Current Sources provide the selectable constant currents used to generate their respective sweep ramps. In addition, circuitry in the A Current Source stage provides for variable sweep rates by varying the bias voltage on the current source transistor, varying the charge rate of the selected timing capacitors. With the exception of this variable current feature, the A and B Current Sources are identical; therefore, only the A Current Source will be described.

Timing current selection data from the Timing Current Latch is applied to the select inputs of analog switches U400 and U410. This selection data connects one of the precision timing resistors within R400 to the emitter of Q422 through switch U400. At the same time, the voltage developed across the resistor is connected to the inverting input of U420 via switch U410 and R450A. Transistor Q422 will become forward biased and will conduct the amount of current necessary to bring the inverting input of U420A to the level present on its noninverting input.

The normal timing currents are adjusted at the time of calibration by setting the A TIMING adjustment R424 to the level that matches the charging current through Q422 to the charging characteristics of the timing caps. Once set, selection of any of the timing resistors provides a charging cur-

rent in precise proportion to any of the others, since the voltage developed across the resistor (sensed by U420A) is the controlling parameter.

Since there is always some finite impedance through the switches in U400, a voltage drop will develop through the switch. Voltage sensing by U420A is done through U410 (a low-current path) instead of at the emitter of Q422. This compensates for any voltage drop through switch U400 due to the internal resistance and keeps each timing current precisely proportional to the others.

By asserting the VAR SWP SELECT applied to pin 10 of U300B, the variable timing voltage from U320B sets the current through the timing resistor. Since moving the front-panel VAR TIMING control varies this voltage, the timing current (and thus sweep rate) varies directly with the control's position.

A and B Timing Capacitor Selection

The timing capacitors are selected by the latched setup data from U120 of the Sweep Control Latch. The A and B Timing Capacitor Selection stages are identical and each contains two switching transistors. For the highest sweep speeds, the control bits to each stage are both LO, reverse biasing the selection transistors. This causes all charging current to be directed to the 62 pF capacitor paralleled by the 2.5 pF–20.5 pF trimmer capacitor. For lower sweep speeds, the 0.1 μF and 1 μF capacitors are placed in parallel with these smaller capacitors by applying a HI to the base of the appropriate transistor switch.

A and B Ramp Followers

The A and B Ramp Followers are nearly identical; therefore, only the A Ramp Follower will be described.

The linear ramp generated by charging the selected timing capacitor(s) with the selected current source is applied to the gate of source follower Q450 through resistor R423. The FET provides a high-impedance input and prevents current from being drawn from the charging node. Transistor Q452 is configured as a current source for the source follower.

The output of the source follower is applied to the base of emitter-follower Q480. The output of the follower is the current-buffered A SWP signal and is used to drive the Horizontal Preamp (when selected by the Horizontal Select stage on diagram 11). The EOS DETECT signal from the junction of R480 and R482 is applied to a comparator circuit on diagram 9 and is used to detect the end of the sweep (ramp has reached its positive limit).

A and B Current Switches

The A and B Current Switches enable and disable the charging sweep ramps under control of their associated sweep gate signals (from the sweep control circuits on diagram 9). The A and B Current Switches are identical; therefore, only the A Current Switch will be described.

With no sweep gate present, the base of Q484 will be lower than that of Q482. This turns Q484 off and Q482 on, discharging the selected capacitors through R492, Q482 and R488. The capacitors will be discharged until the output of the A Ramp Follower (applied to the base of Q492 in the A Baseline Stabilizer stage) reaches 0 volts. When this occurs, the output of A Baseline Stabilizer will go positive and will start to turn off Q482 by pulling its emitter positive. This transistor will turn off until it sinks precisely the same amount of current from the charging node as that being put into the node by the A Current Source. This is the discharge half of the ramp cycle and holds the ramp's output level at precisely 0 volts (discharged).

When the sweep control logic initiates a sweep, the A SWP GATE signal applied to the base of Q484 through R494 turns Q484 on and Q482 off. With Q482 off, the charging node charges positive in a linear fashion until the A SWP GATE signal is removed. The Sweep Control logic on diagram 9 monitors the sweep ramp and determines when the sweep gate should be removed.

A and B Baseline Stabilizers

The A and B Baseline Stabilizer circuits detect when the discharging sweep ramps reach 0 volts and hold the ramp outputs at that level until the next sweep gate initiates the next ramp. The two circuits are identical; therefore, only the A Baseline Stabilizer will be described.

Transistors Q490 and Q492 are configured as an emitter-coupled comparator referenced at 0 volt by the base of Q490. As long as the sweep ramp applied to the base of Q492 is more positive than this 0 volt reference level, transistor Q492 is reverse biased and has no effect on the operation of the A Current Switch.

When the A SWP GATE applied to Q484 of the A Current Switch goes LO, Q482 turns on and begins discharging the charging node through R492. As the discharging output level of the A SWP ramp approaches 0 volt, transistor Q492 begins to turn on. This pulls the emitter of Q482 positive and begins to turn off that transistor. With an output level of precisely 0 volt, transistor Q482 will be sinking exactly the same amount of current from the charging node as that being injected into the node by the A Current Source. This is the balanced condition, and the output will remain at 0 volt until the next A SWP GATE initiates the next ramp cycle.

HORIZONTAL PREAMP AND OUTPUT AMPLIFIER ⟨11⟩

The Horizontal Preamp and Output Amplifier (diagram 11) selects the source of the horizontal deflection signal and amplifies it to the levels necessary to drive the horizontal deflection plates of the crt.

Horizontal Select

The Horizontal Select stage consists primarily of analog switch U200. One of the four input signals is routed to the output and applied to the Horizontal Preamp, depending on which of the select inputs is asserted (HI).

The select input signals are controlled by the Horizontal Mode Control and Unblanking Logic circuits on diagram 17. When selected, the A SWP and B SWP signals provide normal sweep ramp deflection of the crt beam. The XY SIGNAL is a single-ended version of the CH1 signal and allows XY displays of CH1 against CH2. The horizontal gain for the X-Y mode is adjusted with XY GAIN pot R220. The horizontal deflection signals for storage displays come from the STORAGE X-AXIS input line. Resistor R202 and capacitor C206 provide smoothing of the storage deflection signal.

Horizontal Preamp

The Horizontal Preamp provides amplification of the selected horizontal signal, allows horizontal positioning of the display, provides for X10 MAG sweeps, and provides for injection of the horizontal readout signal.

The selected horizontal signal is applied to the base of U270A and the HORIZONTAL POSITION level is applied to the base of U270B via analog switch U220B and buffer U120A. Transistors U270A and U270B are configured as an emitter-coupled, paraphase amplifier with U270E acting as the constant-current emitter source. The analog signal at the base of U270A appears as out-of-phase signals at the collectors of U270A and U270B, as does the horizontal positioning level applied to the base of U270B. The horizontal positioning level will be disabled (switched to ground) by the X-Y ENABLE signal for X-Y displays.

For normal horizontal displays, the $\overline{\text{RO BLANK}}$ (readout blank) signal applied to the base of U280B through R290 will be LO, indicating that the readout is inactive. This disables the readout signal path by removing emitter bias from U280C and U280D through U280B and U280E. The emitter bias for U270C and U270D is provided via U280A and U280E, and the normal signal path is opened.

Gain of the stage is determined by the resistors between the emitters of U270C and U270D and those resistors in their collector circuits. Asserting the $\overline{\text{MAG}}$ signal closes relay K270 and places resistors R266 and R268 in parallel with the normal gain-setting resistors R260-R258. X10 GAIN adjustment R266 is set to increase the horizontal gain by precisely 10 with the relay closed. The paraphase outputs at the collectors of U270C and U270D are applied to the Horizontal Output Amplifier.

To enable the readout signal path, the $\overline{\text{RO BLANK}}$ signal applied to the base of U280B is set HI, indicating that the readout is active. This provides emitter bias for transistors U280C and U280D via U280B and also turns U280A off by pulling its emitter positive (through the base-emitter junction of U280B). With U280A off, bias current for U270C and U270D is removed and the transistors are turned off. This closes the normal signal path and, at the same time, the readout path is opened.

The horizontal readout signal ROX is applied to the base of U280C through resistive divider R281-R283. Transistors U280C and U280D are configured as a paraphase amplifier and convert the single-ended readout signal to two complementary signals at their collectors. Gain of the stage is set with the RO GAIN adjustment R284 in the resistive network between the transistors' emitters. Adjusting the RO POSITION adjustment R280 varies the bias voltage at the base of U280D. This voltage change is also amplified as a paraphase signal and shifts the quiescent operating points of both outputs (and thus the horizontal position of the crt readout display).

Horizontal Output Amplifier

The Horizontal Output Amplifier converts the current signal from the Horizontal Preamp stage to the deflection voltages required to drive the horizontal deflection plates of the crt. Since the signals driving the amplifier are symmetrical and the amplifier configuration is symmetrical, only one of the symmetrical halves will be described.

The bias network composed of CR100-R106 sets the base of Q100 at a level one diode drop below +5 volts. This sets the emitter of Q100 at +5 volts (one diode drop up) and forces the output of preamplifier transistor (either U270D or U280D) to operate in current mode; i.e., the output from the preamplifier will sink varying amounts of current away from the emitter of Q100 but the emitter voltage of Q100 will not vary.

The output stage, made up of Q120, Q140, and Q160, uses a self-biasing configuration that supplies bias current

to Q120 through R130. The quiescent current through Q100 will develop a voltage across R100 but, by itself, will not allow the base-emitter junction of Q120 to become forward biased, since diode CR106 and R100 are pulling it down. This forces the output voltage at the collector of Q140 positive to a level that supplies enough current through R130 and CR106 to increase the voltage drop across R100 to the level that allows Q120 to turn on (0 volt at the cathode of CR106). This is the balanced condition and is the biasing point of the output stage.

The changing signal currents through Q100 will tend to vary the current in R100. This slightly varies the base drive of Q120, and the output voltage at the collector of Q140 moves to compensate for the base current change. Since the voltage drop across R100 must stay constant to maintain proper biasing, and due to the phasing relationships in the output stage, a current change will occur in R130 to make up for the varying signal current. The current change in R130 is passed through CR106 and on to R100, holding the overall voltage drop across the resistor constant; thus maintaining proper bias of the stage.

Transistor Q160, zener diode VR260, and resistor R264 form a constant-current source for the output stage. Schottky diodes CR120 and CR220 prevent excessive signal differences from occurring.

Mag Registration adjustment R200, in the other half of the output stage, is used to "register" the magnified sweep so that the center division of a normal display will cover the 10 graticule divisions when the front-panel X10 MAG button is pressed.

ACQUISITION 

The Acquisition circuit (diagram 12) samples the selected analog signal and converts each sampled point to an 8-bit digital representation for convenient storage.

Dual Peak Detector

The Dual Peak Detector is a special IC that continuously monitors the acquisition signal and stores the most positive and negative levels (peaks) detected during the sampling interval. The differential ACQ (acquisition) SIGNAL from the Acquisition Pickoff stage on diagram 6 is amplified by operational amplifier U40. Amplifier gain is set by R47 while the dc offset level is set by R42.

The amplified signal is applied to the peak detector IC, U50. This IC continuously monitors the input signal and stores the dc levels of the most positive and negative peaks detected after a RESET pulse. Inverter U800A is used to reset the IC on the falling edge of the MIN select signal. Resistors R53 and R54 form a resistive divider that biases the input of U800A positive, holding the output level used to reset the IC negative (enabled). Capacitor C53 is a differentiator used to detect the falling edge of the MIN pulse and will only pull the input to U800 LO for a short time. This generates a short reset pulse on the falling edge of MIN.

The analog switch U55 allows the Sampler to acquire samples from three different sources; the MAX PEAK OUT, the MIN PEAK OUT, and the normal acquisition signal. The three selection signals are controlled by the Acquisition Control logic on diagram 13.

Sampler

The Sampler stage samples the selected signal source from the Dual Peak Detector's channel switch under control of the Cycle Generator and buffers the sampled signal to the A-D Converter stage. The sampling bridge diodes are normally forward biased and pass the input signal to storage capacitor C60. The voltage on the storage capacitor follows the input signal until a sample is to be taken. When the SAMPLE input applied to pin 2 of U420A goes HI, the sampling bridge is turned off and the charge on C60 is held at its last value. This value is buffered to the A-D Converter stage by source-follower Q60 where the analog value is converted to a digital representation.

The sampling bridge diodes (CR60A-D) are normally held in their forward-biased state by resistor R3 within U60 and by transistor Q94. With the bridge on, the input signal is applied to storage capacitor C60 via the STORAGE HF (storage HF response) adjustment R50. This voltage is buffered by source-follower Q60 to the A-D converter stage. The bias divider in U94 holds Q94 on and Q98 off until a positive SAMPLE pulse is applied to U420A, at which time Q98 turns on and Q94 turns off. With Q98 on, the cathodes of CR60B and CR60C are pulled positive and, with Q94 off, the anodes of CR60A and CR60D are pulled negative through R2 within U60. Diodes CR1, CR2, and CR3 within U60 limit how far the sampling bridge diodes may be reverse biased and allow quick recovery of the bridge to the forward-biased state when transistors Q94 and Q98 switch states.

Transistor Q74 and its associated components comprise a constant-current source for the switching transistors Q94 and Q98. Diode CR74 provides thermal compensation for the base-emitter junction of Q74 and serves to hold the current characteristics of the source somewhat constant with varying temperatures.

The FET buffer, composed of Q60 and Q62, provides a high-impedance input for the voltage sample stored on C60. This high impedance minimizes drain-down during the conversion time when the sampling bridge is off. Transistor Q60 is a source follower and Q62 is the current source for Q60.

Cycle Generator

The Cycle Generator, under control of the A-D Converter IC, generates the SAMPLE pulse that turns off the sampling bridge diodes as described in the Sampler description. Timing of the Cycle Generator is illustrated in Figure 3-4.

Whenever an A-D conversion is finished, the $\overline{\text{INIT}}$ line to the $\overline{\text{LOAD}}$ input of U500 is set LO. This causes the data at the D0-D3 inputs to be loaded to the counter's outputs. As long as $\overline{\text{INIT}}$ remains LO, the counter outputs will not change. Loading the counter removes the HI from the $\overline{\text{CE}}$ input at pin 4 and enables part of the logic within the counter.

When an acquisition is supposed to take place, the ACQ signal from the Acquisition Timebase and Control circuit on diagram 13 will be set HI. This pulls the SAMPLE signal to U420A HI to turn off the sampling bridge and also tells the A-D Converter to begin the analog-digital conversion (CONV goes HI). The A-D Converter sets the $\overline{\text{INIT}}$ line HI (converter is busy) and enables the counter U500 to increment on the next 20 MHz clock pulse.

With $\overline{\text{INIT}}$ HI, $\overline{\text{ACQ}}$ may now be removed and the SAMPLE pulse will remain HI. The following clock cycles increment the counter until U500's overflow (MAX/MIN) output goes HI, disabling the counter (preventing the counter outputs from incrementing further) and holding the sampling bridge off.

The A-D conversion continues and, when complete, the $\overline{\text{INIT}}$ line is once again set LO. This reloads the counter and removes the HI SAMPLE pulse, turning the sampling bridge back on in preparation for the next conversion. The converted data is written into the Acquisition RAM with the next LO $\overline{\text{WRACQ}}$ (write acquisition data) pulse generated (at the beginning of the next acquisition cycle).

A-D Converter

The A-D Converter, as explained in the Cycle Generator description, converts a sampled analog voltage to an 8-bit binary representation. The converter IC uses a successive-approximation technique to perform the conversion. Conversion requires a minimum of 9 clock cycles, the first of which allows the voltage level at the A_{IN} (analog in) input to settle to a stable level.

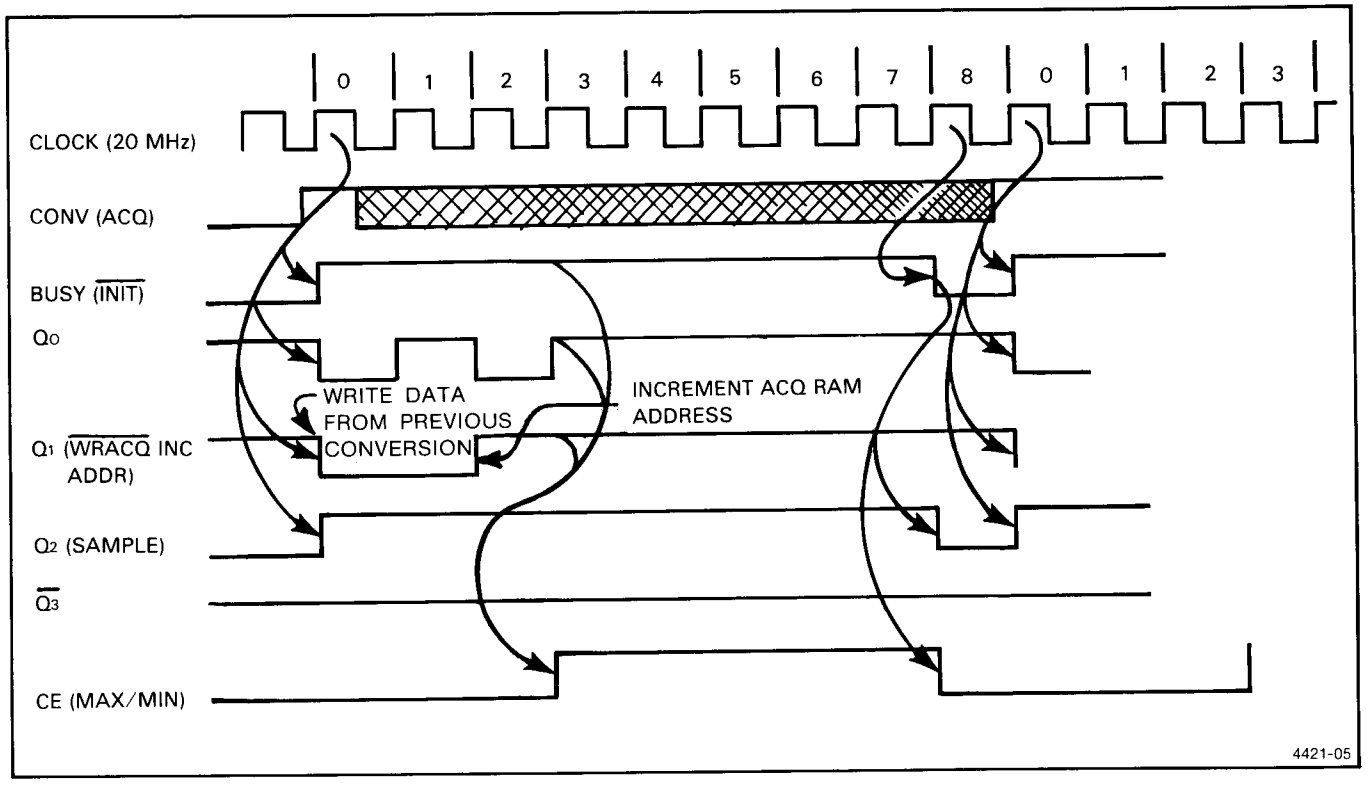


Figure 3-4. Timing of the Acquisition Cycle Generator.

Conversion is initiated with a HI applied to pin 2 of U100. This sets the BUSY output HI, indicating that a conversion is in process. One clock cycle before conversion is complete, BUSY will be reset LO as an indication to the Cycle Generator that it should get ready for the next conversion.

Tri-state buffer U220 is enabled with a LO applied to pins 1 and 19 and is on as long as an acquisition is in process. When turned on, it buffers the conversion data from U100 to the Acquisition RAM, where it is stored for future recall.

The voltage divider at pin 13 of U100 establishes a reference voltage level used to scale the internal conversion currents. The capacitors at pin 14 are high-frequency bypasses that minimize conversion noise. Other information about the A-D Converter is given in the preceding Cycle Generator description.

Acquisition RAM

The digital data generated by the A-D Converter is stored in the Acquisition RAM. When a conversion is in process, the $\overline{\text{DONE}}$ signal applied to pin 20 is HI and disables the output portion of the 8 I/O lines. Data from the converter is applied to the I/O lines via tristate buffer U220 and is written to the location addressed by the 11 address lines at the beginning of the next conversion cycle ($\overline{\text{WR ACQ}}$ goes LO).

When the stored data is to be moved to a waveform storage location, $\overline{\text{DONE}}$ from the Acquistiion Control stage will be set LO to enable the data outputs. The Acquisition Address Counter will then sequentially output the data onto the data bus so it may be transferred to the waveform storage location selected.

ACQUISITION TIME BASE AND CONTROL 13

The Acquisition Time Base and Control circuits (diagram 13) generate the addressing, timing, and control signals required for waveform acquisitions. The Equivalent Time Clock Generator and Acquisition Time Base stages generate the commands to the Sampler (diagram 12) to acquire data points at specific times, while the Acquisition Address Counter and Acquisition Window Counter stages store the proper number of pre- and post-trigger samples into the Acquisition RAM.

Bus Interface

The Bus Interface circuit latches control data from the Microprocessor (defining the rate that data acquisitions should be made) and produces two address-decoded control signals that allow the Microprocessor to reset the Acquisition Address Counter (via $\overline{\text{ARM}}$ signal) and allow the Microprocessor to read the LSB of the Acquisition Address (via $\overline{\text{LO}}$ signal) for identifying the acquired channel.

Data latch U780 stores eight bits of Microprocessor data when the $\overline{\text{TBD}}$ (time base data) line from address decoder U785A goes from LO to HI (see Table 3-1 for address decoding). Bits DT0-DT4 of the latched data are used to set the divider ratio of a programmable counter in the Normal Acquisition Clock generator stage used to generate acquire pulses at a time-base dependent rate. The next bit of data, DT5, is used to enable either the Equivalent Time Clock Generator or the Normal Acquisition Clock Generator, depending on the type of acquisition to be made. The SEL A/$\overline{\text{B}}$ control bit is used to select the source of the gate signal used for making acquisitions, while the ENV control bit is used to enable acquisitions in envelope mode.

Address bits A4 and A5, along with the $\overline{\text{WFM CONTROL}}$ signal are address decoded (see Table 3-1) to produce two other control signals, $\overline{\text{LO}}$ and $\overline{\text{ARM}}$. The $\overline{\text{ARM}}$ signal is used to reset the Acquisition Address Counter and Acquisition Status Latch, and to preload the Acquisition Window Counter with the trigger point data.

Equivalent Time Clock Generator

The Equivalent Time Clock Generator is used at sweep speeds faster than or equal to 50 μs per division. It produces acquire (ACQ) command pulses that cause one data point to be A-D converted with each successive sweep. The selected sweep ramp is compared to the output of a staircase generator that increases one step with each sweep so the acquire pulses occur at linear and well-defined points along the ramp.

Dual comparator U600, under control of the SEL A/$\overline{\text{B}}$ signal, allows selection of a sweep ramp to do the data acquisitions against. When SEL A/$\overline{\text{B}}$ is HI, the HI S1 input selects the A SWP ramp. When SEL A/$\overline{\text{B}}$ is LO, U800B inverts the level and applies a HI to the S2 input, selecting the B SWP ramp.

The selected sweep ramp is compared to the rising staircase waveform at the comparator's other inputs. The staircase is generated by integrator U650 and switchable current source Q650. Transistor Q700 is used to discharge the integration capacitor C650 when the staircase is complete and keeps the staircase generator inactive until next enabled.

To enable the staircase generator, a minimum of 2048 samples are stored and counted by the Acquisition Address Counter. Once these are stored, the following sweep gate will set $\overline{\text{TRIG'D}}$ LO, turning Q700 off. During generation of the staircase, Q700 will remain off.

To generate the staircase, the current source made up of Q650 (and the associated components at its emitter) supplies a constant current to the integrator U650 whenever a LO $\overline{\text{WRACQ}}$ (write acquired data) pulse forward biases the current source transistor (reverse biases CR734 and allows the emitter of Q650 to pull down through R730 and R732). The $\overline{\text{WRACQ}}$ pulses are all of equal duration, so the charge supplied to the integrator with each pulse is constant. With U650's noninverting input referenced essentially to ground via R650 (control bit DT5 is set LO and diode CR650 is reverse biased), each $\overline{\text{WRACQ}}$ pulse causes the output of U650 to integrate 1 mV more positive. When the pulse ends, the new voltage level is maintained.

The selected comparator within U600 compares each sweep ramp to the present staircase level to determine when each sample should be taken. Since the staircase increments in a linear fashion, each successive sweep ramp causes a single sample to be taken at a predefined horizontal position. After the Acquisition Window Counter determines that the staircase is complete (2048 post-trigger samples taken and stored), the $\overline{\text{DONE}}$ output to the Microprocessor (diagram 1) goes LO and DONE to multiplexer U480 goes HI. This switches the clock source for the Acquisition Address Counter to the processor-generated $\overline{\text{RDACQ}}$ pulses and signals the processor that acquisition is complete.

The processor then performs an algorithm to transfer the acquired data to display memory by generating 2048 $\overline{\text{RDACQ}}$ (read required data) pulses, incrementing through all addresses of the Acquisition RAM (using the Acquisition Address Counter). When the next acquisition begins, the processor asserts the $\overline{\text{ARM}}$ signal to reset everything and Q700 turns on to discharge the staircase storage capacitor (C650). Transistor Q700 remains on as the first 2048 samples are acquired and then turns off to enable the staircase for the following 2048 samples. This entire process is repeated for each equivalent time acquisition.

The RS flip-flop made up of U800C and U800D allows only one acquire pulse to be generated with each sweep gate.

Normal Acquisition Clock Generator

The Normal Acquisition Clock Generator produces the acquire pulses to initiate sampling for normal acquisitions. A crystal-controlled clock frequency is divided down to a lower frequency (sampling frequency) dependent on processor data loaded into a programmable counter. This allows samples to be taken at proper intervals for each of the various sweep rates.

To enable the NORMAL Mode, bit DT5 to the reset input of U760 is set HI by the processor. This HI disables the Equivalent Time Clock Generator by pulling the noninverting input of U650 HI through CR650 and enables programmable counter U760. Processor data, defining the division ratio of the counter, is applied to the counter at the S1-S4 inputs.

The 2 MHz clock, from 20 MHz oscillator U710 and ÷ 10 counter U740A, is divided by this programmed ratio and produces an acquire clocking signal to the D input of U790B. This signal is synchronized to the 4 MHz clock by U790B, and the NORM ACQ signal is applied to OR gate U755D. The output of U755D now produces the acquire pulses for the NORMAL Mode acquisitions.

Envelope Acquisition Clock Generator

For ENVELOPE Mode, the ENV bit from U780 is set HI by the processor. This switches the inputs of data selector U720 in the Acquisition Control stage and isolates the previously described acquisition pulses from the Sampler circuit. Acquisition pulses are now produced by the Envelope Acquisition Clock Generator.

The Normal Acquisition Clock Generator is still putting out the divided-down acquisition pulses which are applied to the ÷ 2 counter U790A. Since, in ENVELOPE Mode, two acquisitions are done for every ACQ pulse, this counter serves to keep the overall sampling rate equal to that for normal acquisitions.

The divided clock is applied to U750A and clocks the Q output HI. The HI removes the reset condition of U750B and is also applied to U755C, enabling the 400 kHz clock from counter U740B to generate ENV ACQ pulses. These pulses are applied to the Sampler circuit and two samples are taken. When each of these samples is taken, $\overline{\text{WRACQ}}$ to the Acquisition Address Counter toggles, incrementing the counter with each sample.

When the first sample is initiated, address line AA0 is HI and a HI MAX signal is applied to the Sampler. This causes the maximum point to be sampled. Part way through the acquisition of the maximum point, the $\overline{\text{WRACQ}}$ signal will go HI and the Acquisition Address Counter will increment, setting AA0 LO. This LO is applied to U755A of the Acquisition Control stage and sets up the Sampler prior to the next acquisition with a HI MIN signal from U720.

The following 400 kHz ENV ACQ pulse initiates acquisition of the MIN point. After the minimum value has been stored on the sampling capacitor, $\overline{\text{WRACQ}}$ goes HI again, incrementing the Acquisition Address Counter and resetting the Dual-Peak Detector.

Address bit AA0 now goes HI, clocking a LO to the $\overline{Q}$ output of U750B. This resets U750A which, in turn, resets 750B. With U750A reset, the 400 kHz pulses through U755C are disabled.

The pulses through U755C remain disabled (so no more samples are taken) until the next clock from U790A, at which time the whole cycle repeats itself. In this way, the MAX and MIN samples are alternately acquired at the overall sample rate dictated by the SEC/DIV control setting.

Acquisition Control

The Acquisition Control stage consists primarily of data selector U720 and routes control signals to the Sampler, depending on acquisition mode.

When enabled, and ENVELOPE Mode is selected, ENV applied to the select input is HI and DONE applied to the enable input is LO. Those signals at the device's B inputs are routed through to the outputs and control the acquisition. When the acquisition is complete, DONE will go HI and disable U720.

When either normal or equivalent time sampling is selected, ENV will be LO. This selects the signals at the A inputs of U720. When acquisition is complete, DONE goes HI and disables the device as described above.

Acquisition Address Counter

The Acquisition Address Counter increments the addresses for the Acquisition RAM when data is being written into or out of the device. When writing data into the RAM, the $\overline{WRACQ}$ (write acquired data) signal increments the RAM address as each sample is taken. When writing acquired data from the RAM to display memory, the processor-generated $\overline{RDACQ}$ (read acquired data) clock increments the RAM address.

When writing data into the Acquisition RAM, the clock applied to pin 3 of U310A will toggle HI when 2048 data points have been stored. This sets the FULL line at the output of U310A HI, indicating that the Acquisition RAM is full of valid waveform samples. At the same time that this occurs, all 11 of the acquisition address lines will toggle LO, looping back around to the first location in the Acquisition RAM. Samples continue to be taken until the next sweep gate is initiated. The rising edge of the selected sweep gate corresponds with the sweep trigger point and clocks the $\overline{Q}$ output of U310B LO. This is the $\overline{TRIG'D}$ signal and enables the Acquisition Window Counter to start counting post-trigger samples (see that description).

When the processor initiates the next waveform acquisition, it will momentarily set the $\overline{ARM}$ signal to the Acquisition Address Counter (and to U785B, configured as an inverter) LO, resetting the counter.

Acquisition Window Counter

The Acquisition Window Counter is a presettable counter used to count data-point acquisitions occurring after the trigger event detected by the Acquisition Address Counter. Since the Acquisition Address Counter always fills the Acquisition RAM with valid data samples before detection of a trigger event is allowed, sampled data of what occurred prior to the trigger event is available. The operator may select the size of the "Acquisition Window"; i.e., how many sampled events occurring after the trigger point will be displayed. Once the window is selected, the Acquisition Window Counter allows that many more samples to be taken and then stops the acquisition. When the acquired data is displayed, there will be data acquired before the trigger event and then the user-selected amount of post-trigger data displayed. There are 1024 points of data acquired for each of CH 1 and CH 2. Display of the data is based on the user-selected size of the Acquisition Window and is shown in Table 3-2.

Table 3-2
Acquisition Windows

Acquisition Window Selected	Pretrigger Points	Post-Trigger Points
PRE TRIG	896	128
MID TRIG	512	512
POST TRIG	128	896

Initially, when the processor asserts the $\overline{ARM}$ signal to reset the Acquisition Address Counter and Acquisition Window Counter, four bits of data, defining the size of the post-trigger window, are loaded into presettable counter U380. Then, when the Acquisition Address Counter detects a trigger event (see that description), $\overline{TRIG'D}$ goes LO and enables the Acquisition Window Counter. Sampling continues in the normal manner as the Acquisition Window Counter counts these post-trigger samples. After U360B, U360A, and U380 have counted the preset number of post-trigger samples, the Q_2 output of U380 goes LO and clocks U340A. This generates a HI DONE signal at the Q_0 output of U340A and changes the selection inputs of data selecter U480. $\overline{DONE}$ at the output of U420B is applied to the Microprocessor circuit to let it know that the post-trigger acquisition is complete.

Clock and Gate Multiplexer

With a HI DONE signal applied to data selecter U480, the GATE output to U310B goes to a steady HI and the source of clocks for the Acquisition Address Counter switches from the Sampler-generated $\overline{\text{WRACQ}}$ pulses to the processor-generated $\overline{\text{RDACQ}}$ pulses. Since the processor knows that the acquisition is complete ($\overline{\text{DONE}}$ went LO), it now begins to move the acquired data from the Acquisition RAM to display memory.

Since the acquired data points are stored sequentially in the Acquisition RAM and the addresses automatically loop back around to the first RAM location when the last location is written, the first point of the waveform is stored at the location immediately following the last-acquired post-trigger data point. To move the acquired waveform data points to display memory, the processor sequentially addresses the desired display memory locations and toggles the $\overline{\text{RDACQ}}$ line, moving one byte of data with each $\overline{\text{RDACQ}}$ pulse.

When all acquired data points have been moved to display memory (where the display hardware automatically displays it), the Microprocessor reasserts $\overline{\text{ARM}}$ to reset everything and another acquisition is made. This process continuously repeats itself whenever acquisitions are made using the Normal or Envelope Clock Generator circuits.

DISPLAY MEMORY AND DISPLAY CONTROL ◈14◈

The Display Memory stage (diagram 14) provides storage of acquired waveform information, cursor information, waveform start information, and readout character information. The rest of the circuitry on this schematic controls the display of this stored data.

Display Memory

The Display Memory consists of four RAM devices that keep track of four separate types of waveform-related data. U320 is the waveform RAM and stores the acquired data from the Acquisition RAM (diagram 12) when the front-panel STORE button is pressed. U310 is the start RAM and stores a HI bit in one location to indicate the start of the waveform data. U300 is the cursor RAM and operates similarly to the start RAM, indicating cursor location with HIs stored at the cursor locations.

Data to be written into one of the four RAM devices is applied to the input pins via tri-state buffer U100. A LO $\overline{\text{WRDISP}}$ (write display data) signal enables the buffer when writing data from the processor data bus. Device selection is controlled by four latched write enable lines from the Bus Interface stage, and addressing is done via the Display Address Multiplexer.

The chip selects for U320 and U325 are controlled by U110B and U110D. The HI WRDISP signal applied to both of these gates when writing data into Display Memory enables the chip selects of both U320 and U325. The data applied to the I/O pins will be written to the device that is write enabled by U150 of Bus Interface stage.

When WRDISP goes LO (display writing over), data will be read out of the device selected by RO/$\overline{\text{WFM}}$ (readout or waveform) applied to U110D. Since the line is controlled by a counter bit from the Display Address Counter, the RO/$\overline{\text{WFM}}$ line will first be LO. This is inverted by U110D to disable the character RAM U325, and reinverted by U110B to enable the waveform RAM U320.

With U320 selected, the address from the Display Address Counter (via the Display Address Multiplexer) will increment through each location of waveform RAM U320, cursor RAM U300, and start RAM U310. Data from cursor RAM and start RAM are applied to the Display Control stage and generate control signals that start the storage display ramp and produce cursors on the display waveform. Data from the waveform RAM produces the vertical deflection information for the stored waveform displays.

When RO/$\overline{\text{WFM}}$ is HI, U110D inverts the level and enables character RAM U325, and the readout deflection data is sequentially clocked out of the RAM by the Display Address Multiplexer.

Bus Interface

The Bus Interface stage consists of U130A and U150 and generates write enable signals for writing data into the four RAM devices in the Display Memory stage.

One-of-four decoder U130A decodes address bits A4 and A5 when enabled by a LO $\overline{\text{WFMCTRL}}$ signal and, when both are LO, produces a LO $\overline{\text{DISMD}}$ (display mode), enabling the input latch of U150. The three bits of select data (D2, D4, and D6) are transferred to an internal latch and, when the enable returns HI, the data is stored. The $\overline{\text{WRDISP}}$ (write display data) signal is inverted by section 4 of U220 and is applied to the G1 input of U150. When the processor is ready to write the data to the device selected by the data latched in U150, the $\overline{\text{WR}}$ (write) signal to U150 will go LO and the selected output will go LO. This write enables the desired device, and the processor data is written from the data bus (via U100) to the location addressed by the processor address bus (via the Display Address Multiplexer).

Display Address Multiplexer

The Display Address Multiplexer consists of three four-bit, one-of-two data selector ICs controlled by a common select line. The WRDISP (write to display) line is used as the select signal and when LO (writing), the processor address bus is used to address the Display Memory. At any other time (not writing), WRDISP will be HI and the continuously incrementing address from the Display Address Counter will be selected. This continuously cycles through the contents of the Display Memory for producing the crt display.

Display Address Counter

The Display Address Counter is a gated 400 kHz counter used to increment the address of the Display Memory when displaying the stored waveform and readout data.

The 400 kHz clock signal applied to U530C is gated on as long as SWP STOP from the Cursor Logic stage is HI. The 400 kHz clock is applied to the counter made up of U160A, U160B, U180A, and U180B and continuously increments through the addresses of the Display Memory for sequentially displaying the waveform and readout data.

When the Cursor Logic detects that the point being displayed is a cursor point, it will set the SWP STOP line LO to disable the 400 kHz clock to U160A. This holds the present output data and horizontal sweep position on the crt display for a longer period of time thereby, producing an intensified cursor dot. When the Cursor Logic resets the SWP STOP line HI, the counter resumes normal operation and continues incrementing through Display Memory.

The two MSBs of the counter, at pins 11 and 10 of U180B, are used for switching between the character RAM and waveform RAM and for switching between display of CH 1 and CH 2 data respectively. This causes storage displays to be done in the following sequence: CH 2 waveform, readout, CH 1 waveform, readout.

Cursor Logic

The Cursor Logic stage monitors the output of the cursor RAM to detect when a display point is supposed to be a cursor dot and, when detected, stops the horizontal sweep and the Display Address Counter for a short time to intensify that display point. AND-Gate U540B is used to detect when a HI cursor bit is read out of the cursor RAM (via U500) when waveforms are being displayed (WFM/RO HI).

Normally, when waveform dots are being displayed, the SWP STOP signal applied to pins 2 and 12 of U535 will be HI, holding the counter U535A and U535B reset. With this counter reset, the input pin 5 of latch U520 will be LO, resulting in a HI 2Q output applied to AND-Gate U540B. With this enable set HI and the WFM/RO level applied to pin 4 of U540B HI (waveform display), the output at pin 6 will follow the level of the CURS (cursor) line. This line from the cursor RAM (via latch U500) will be LO for noncursor points, keeping the counter U535 reset with a HI SWP STOP level. This HI SWP STOP level also keeps the Display Address Counter enabled via the clock gate U530C.

When a cursor point is encountered, the CURS level read from the cursor RAM will be HI. This causes a LO SWP STOP level, disabling the Display Address Counter, removing the reset to U535, and stopping the Storage Sweep (diagram 15). With its reset removed, counter U535A and U535B begins counting 400 kHz clock pulses. Since The Storage Sweep ramp has stopped and the data from the waveform RAM does not change during this counting period, an intensified dot will appear on the displayed waveform. After 128 clocks, the Q2 output of U535B will go HI, signaling the end of the cursor period. The next 400 kHz clock will clock this HI into U520, causing a LO at its 2Q output. This removes the LO SWP STOP, reenabling the Display Address Counter, the Storage Sweep (diagram 15), and resetting the Cursor Logic counter U535 in preparation for the next cursor. The Display Address Counter now continues incrementing the waveform RAM until the next cursor point is encountered, at which time the entire cycle repeats itself.

Display Control

The Display Control circuit generates signals that control the display of stored waveform and readout data. These signals are derived from other signals developed on the Display Board and control storage display mode, storage display blanking, storage sweep, and updating of readout information.

Latch U520 is used to blank the display when new display data is being written into Display Memory. When writing to the Display Memory, WRDISP will be LO and the Q outputs of U520 will be set LO. The 3Q output applied to U540A and U540C blank the Z-axis drive via both the RO BLANK and WFM BLANK outputs.

When writing is over, the reset will be removed. The next clock to U520 clocks its RO REFRESH output LO, enabling the Readout D-A/Vector Generators (diagram 15). The following clock will set the 3Q output (STORAGE BLANK) HI to reenable the blanking logic, U540A and U540C. Control of the 2Q output is explained in the Cursor Logic description.

Storage blanking is controlled by U500, U540A, and U540C. When storage displays are occurring, the

$\overline{\text{DISP UPDATE}}$ signal is LO and enables the data at U500's D inputs to be clocked through the IC. The RO/$\overline{\text{WFM}}$ select level at the 2D input is used to enable either U540A or U540C while holding the other one in its blanking condition. With RO/$\overline{\text{WFM}}$ set HI, the $\overline{\text{2Q}}$ output to U540C will keep the $\overline{\text{WFM BLANK}}$ line at its output LO. Since the 2Q output and the $\overline{\text{STORAGE BLANK}}$ levels to U540A are both HI, the $\overline{\text{RO BLANK}}$ signal at its output will follow the $\overline{\text{BLANK DOT}}$ input level. This level is controlled by the DD7 bit from the character RAM and will be set HI whenever a stroke of a readout character should be blank. For any displayable stroke, the DD7 bit will be LO. Further information about the readout characters is given in the Readout D-A/Vector Generators description.

Waveform blanking is generated by U540C and is similar to readout blanking, just described. When the RO/$\overline{\text{WFM}}$ input to U500 is LO, the $\overline{\text{RO BLANK}}$ level at the output of U540A will be held LO and U540C will be enabled by the HI $\overline{\text{STORAGE BLANK}}$ and WFM/$\overline{\text{RO}}$ levels at its inputs. The $\overline{\text{WFM BLANK}}$ output level follows the $\overline{\text{START}}$ input level from the $\overline{\text{4Q}}$ output of U500. This inverted output is derived from the data output from the start RAM U310 on the START line. When the waveform data corresponds to the display starting point, the START data will be HI. The resulting HI at the 4Q output (SWP RESET) resets the Storage Sweep (diagram 15) and the LO $\overline{\text{START}}$ level applied to U540C generates the $\overline{\text{WFM BLANK}}$, blanking the first point of display data (for both CH 1 and CH 2). All other waveform points will have the START bit from the start RAM set LO, removing the LO $\overline{\text{WFM BLANK}}$.

The storage display mode is controlled by U120A, U120B, and U190. Flip-flops U120A and U120B latch the two least-significant bits of data-bus data when the address-decoded $\overline{\text{DISMD}}$ (display mode) signal goes HI. These latched bits are applied to data selector U190 and set the output control levels to produce the four possible display modes shown in Table 3-3.

Blanking for single-channel storage displays is controlled by U530B, U50C, U50D, Q550, and their associated components. Figure 3-5 shows a simplified diagram of this block of circuitry and an explanatory truth table.

The ACQ BLANK (acquire blanking) output at the emitter of Q550 will go HI, blanking either CH 1 or CH 2 data points as they are called from display memory, for producing a CH 1 only or CH 2 only display. By blanking the data for the unselected channel when called from memory, a CH 1 only or CH 2 only display will result.

STORAGE DISPLAY AND READOUT ◈15

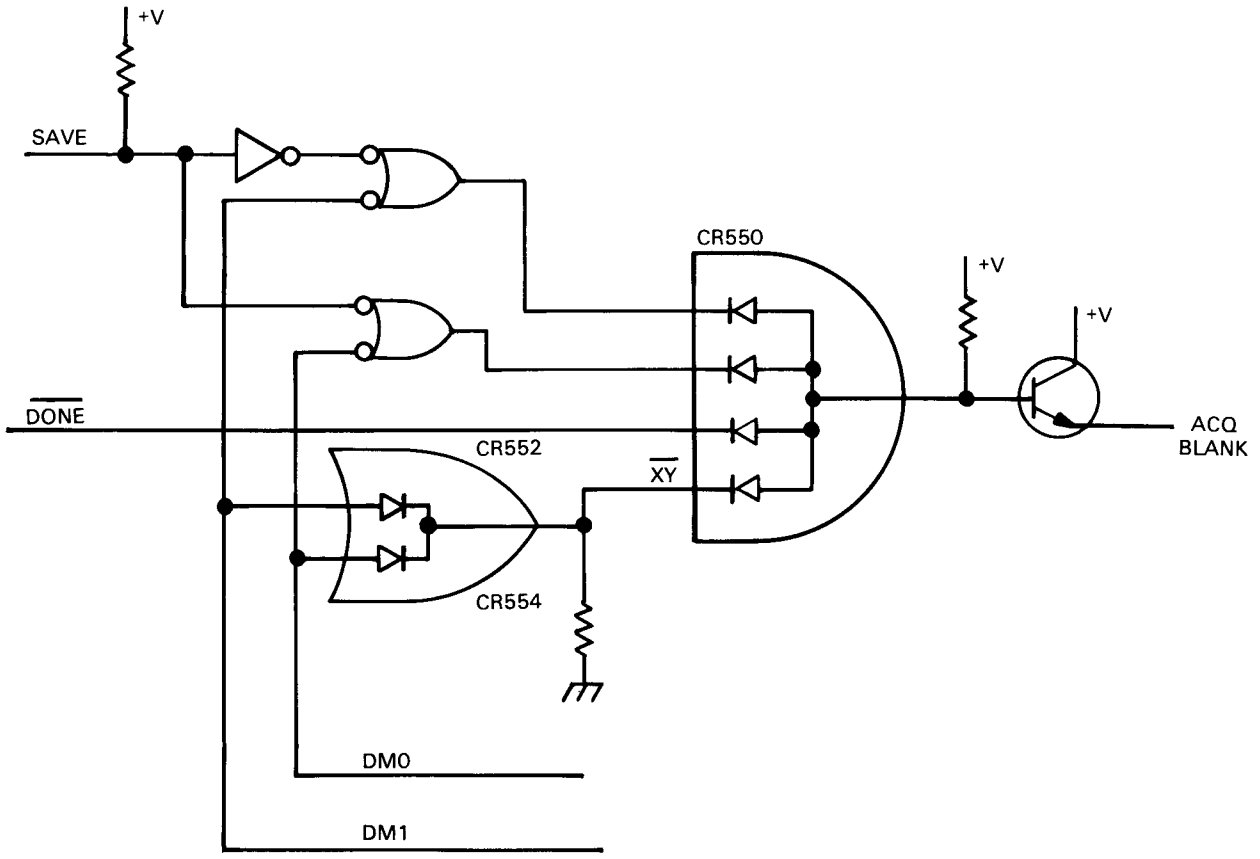
The Storage Display and Readout circuitry (diagram 15) converts the stored waveform and readout data bytes to the analog deflection voltages used to position each of the individual dots (of a stored waveform display) and strokes (used to generate the readout characters) of a stored data display. The Storage Sweep stage generates the sweep ramp that the stored (vertical) waveform data is displayed against to produce waveform displays.

Oscillator

The Oscillator generates the 400 kHz clock used to increment and synchronize the operations of the Storage Display circuitry. The output of inverter U50B provides positive feedback to the input of inverter U50A through C50 and R51 to cause oscillation. Negative feedback for both inverters is provided by resistors R52 and R54 but is always less than the positive feedback, so oscillation is maintained. Adjusting R54 changes the output frequency and thus the rate at which the stored waveform (and readout) data is retrieved from memory and displayed. Since these individual data points are displayed against the constant-rise ramp of the Storage Sweep generator, varying the rate of data display will vary the overall length of the displayed waveform. This adjustment allows the storage sweep to be calibrated to the crt graticule.

Table 3-3
Storage Display Mode Selection

Mode Select Bit		Signal Source		Display
DM1	DM0	Vertical	Horizontal	Mode
0	0	CH 2 Waveform	CH 1 Waveform	X-Y
0	1	CH 2 Waveform	Storage Sweep	CH 2
1	0	CH 1 Waveform	Storage Sweep	CH 1
1	1	Alternate CH 1-CH 2	Storage Sweep	Alt CH1/CH 2



SINE (CH1/CH2	DONE	DM0	DMI	DISPLAY MODE	ACQ BLANK
X	0	X	X	X	LO
1	1	0	0	CH2 - XY	LO
1	1	1	0	CH2 - NORM	LO
1	1	0	1	CH1 - NORM	HI
1	1	1	1	ALT - NORM	LO
0	1	0	0	CH2 - XY	LO
0	1	1	0	CH2 - NORM	HI
0	1	0	1	CH1 - NORM	LO
0	1	1	1	ALT - NORM	LO

4421-06

Figure 3-5. Storage Display Blanking Logic.

Resistor R50 and diode CR50 provide an additional negative feedback path on positive half cycles of the output voltage to produce a more asymetrical output waveform. Since the character "stroke" data is read from memory on the rising edge of the clock while the data is not written to the DACs until the falling edge, a period equal to the HI time of the clock pulse exists in which the DAC output levels remain constant. During this time, a bright dot will be produced since the crt beam is unblanked but is not moving. By making the clock pulse asymetrical, this hold time (and thus bright dots in the readout characters) is minimized.

Readout D-A/Vector Generators

The Readout D-A/Vector Generators convert the stored character data output from the character RAM to the individual "stroke" voltages used to "draw" the readout characters. Each byte of data read from the character RAM uses the 4 LSBs to define the vertical endpoint of that "stroke", while the next 3 bits define the horizontal endpoint of the "stroke".

Each "stroke" results from the fact that as each consecutive endpoint is read from the character RAM, the output deflection voltages (RO X and RO Y) change linearly from the present position to the next position instead of moving immediately to it. With the Z-axis circuitry turned on, this results in a short line segment or "stroke" on the crt.

Data bit DD7, output from the character RAM, allows some of these strokes to be blanked, preventing the various readout characters (including spaces) from blending together in a garbled display. Data bytes with DD7 set LO will be displayed on the crt as character strokes while those with DD7 set HI will be blanked (see Display Control circuit on diagram 14).

Digital-to-analog converters U660 and U700 will be enabled when the $\overline{\text{RO REFRESH}}$ enable is LO. The falling edge of the 400 kHz clock latches the data at each DAC's D0-D7 inputs into an internal storage register, and both DAC outputs go to the analog voltage defined by the digital data in their respective input registers.

Each of these DACs has an operational amplifier integrator connected between its output pin and its feedback input R_{FB}. The integrator provides some smoothing of the transitions between consecutive output levels. The smoothed outputs from these integrators are both followed by an active low-pass filter to provide further smoothing of the transitions.

The four LSBs of data applied to U700 from the character RAM (DDO-DD3) are used to define the vertical position of the end of the character stroke within an 8-wide by 16-high character matrix (see Figure 3-6). The next bit, at the D4 input, is tied LO and allows character display only on alternate rows (only 8 of a possible 16). The next 3 bits (W8, W9 and W10) applied to U700 select on which of these 8 rows the character will be displayed.

The horizontal positioning is done by U660 in a similar manner. RAM data bits DD4, DD5, and DD6 select one of the eight possible horizontal positions within the 8-by-16 character matrix for the endpoint of the stroke. Bits WA3, WA4 and WA5 from the Display Address Multiplexer, along with bits W6 and W7 from the Display Address Counter, select one of 32 horizontal character positions along the selected row.

If every character position had something displayed in it, there would be 8 rows of 32 characters each, with each row vertically separated from those above and below by the height of a character.

The RO X output voltage is applied to the Horizontal Preamp through a signal switch that may either select or deselect the signal, depending on display mode. The RO Y signal is applied to analog switch U400C which allows either readout or waveform deflection signals to control the vertical deflection for storage waveforms.

Waveform D-A/Vector Generators

Operation of the Waveform D-A/Vector Generators is nearly identical to that of the Readout D-A/Vector Generators just described. The major difference is that when the $\overline{\text{WFM UPDATE}}$ enable is LO, the stored waveform data is read alternately into the internal A and B registers with consecutive 400 kHz clocks. Register selection is controlled by address bit WA0, the least-significant bit of the Display Address Multiplexer. Since data in the waveform RAM U320 is stored alternating the CH 1 data with the CH 2 data, using WA0 as the register select for U330 directs the CH 1 and CH 2 data to their proper DAC outputs.

Both the CH 1 and CH 2 DAC outputs are followed by two stages of smoothing, as described for the Readout D-A/Vector Generators. Analog switch U400A allows either CH 1 or CH 2 to provide vertical deflection for storage waveform displays.

Operational amplifier U380A is a buffer used to let the CH 1 signal drive the horizontal system (via analog switch U400B) for X-Y display of storage data. Normal horizontal sweeping of the storage displays is provided by the Storage Sweep generator and is also selected by U400B.

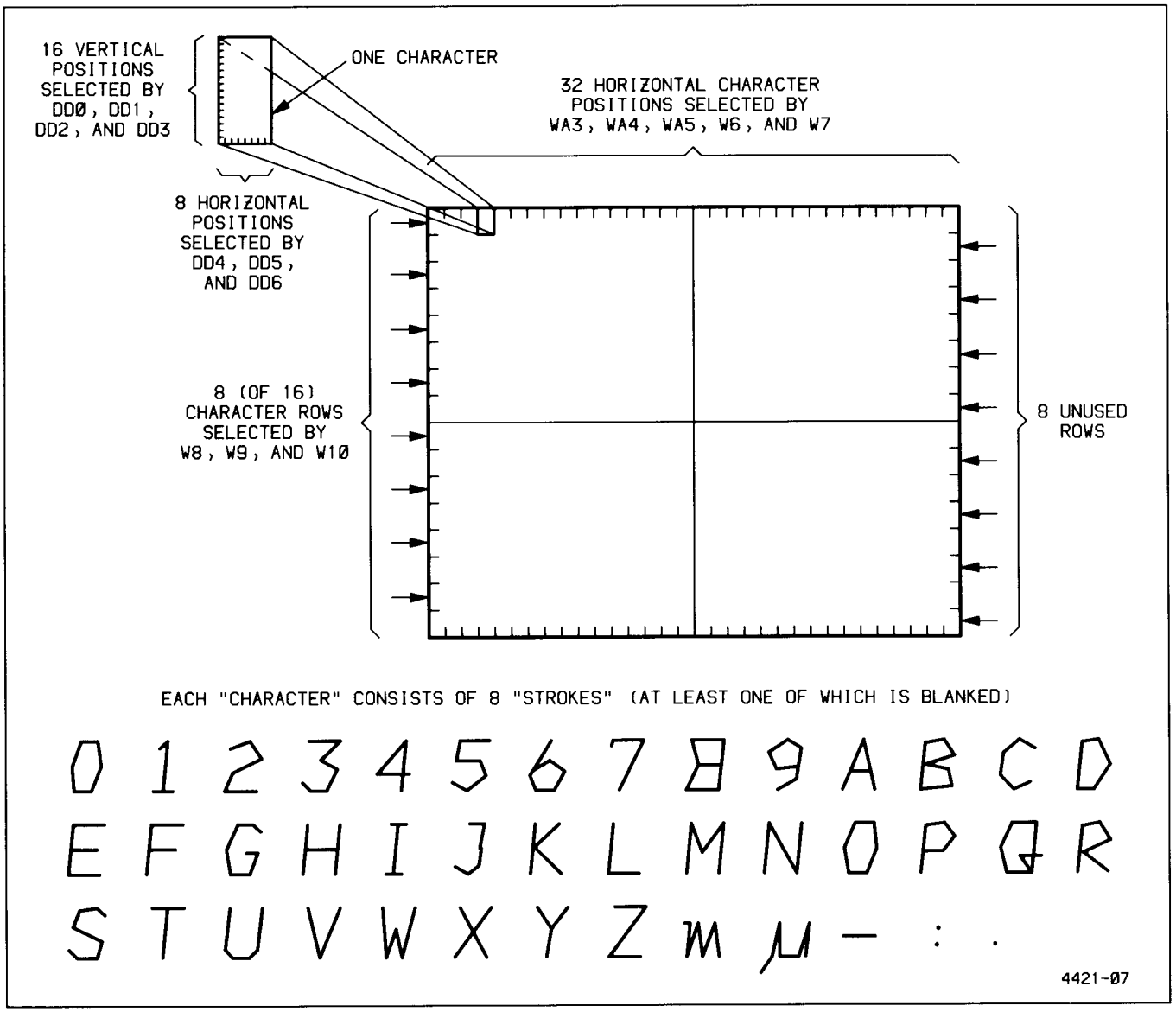


Figure 3-6. Displaying Readout characters.

Storage Sweep

The Storage Sweep circuit generates the linear sweep ramp used when displaying storage waveforms. It is an op amp integrator using a switchable current source and a resettable integration capacitor.

To start a sweep, the SWP RESET signal from the Display Control stage (diagram 14) will go LO when the START data from the start RAM goes LO (second point of data). This turns the discharge transistor Q380 off and allows the integration capacitor C385 to charge.

The charging current for the integrator is supplied through R387 and R385 and will cause the output of the integrator to charge positive until a cursor point is encountered. When this happens, $\overline{\text{SWP STOP}}$ from the Cursor Logic will go LO. This turns Q390 on and shorts the charging current to ground, stopping the ramp output. This ramp output level is held for a short time (determined by the Cursor Logic) and causes the displayed cursor point to be intensified. When $\overline{\text{SWP STOP}}$ returns HI, Q390 turns off and the ramp continues charging from this last level. When another cursor point is encountered, the sweep will again pause to intensify the point and will then complete its charging. When the next waveform is to be displayed, SWP RESET will go HI and discharge the integrator capacitor. The next display point reenables the sweep, and the cycle repeats itself.

EXTENDED MEMORY, BATTERY BACKUP AND GPIB (OPTION 01) ◈16◈

The Extended Memory, Battery Backup and GPIB circuitry (diagram 16) are on a factory-installed optional circuit board. The Extended Memory provides additional storage for sixteen more acquired waveforms (8 each CH 1 and 8 each CH 2). The Battery Backup circuit allows the contents of Display Memory to be maintained with normal instrument power off. The GPIB circuit allows an external GPIB controller to read the contents of the display memory from the 336.

Extended Memory

The Extended Memory consists of two 16k-by-8-bit RAMs and a data latch used to latch the three MSBs of the RAM address from the processor data bus. A tristate buffer enabled by a power-sensing IC in the Battery Backup stage removes the enables from both RAM devices when power is going down, preventing erroneous writes to these RAM devices as the power supplies decay.

During normal operation, tristate buffer U130 is enabled by a LO applied to its enable inputs. The $\overline{\text{OPTRAM}}$ (option RAM) and $\overline{\text{SYS}}$ (system) RAM enable signals are buffered through U130 and are used to enable the appropriate RAM devices, depending on address decoding.

To read or write to one of the option RAM ICs, the processor first writes three bits from the data bus into the latch U140. The three bits are written into the latch when the address-decoded $\overline{\text{OPTBNK}}$ (option bank) signal goes HI. The lower two bits are used as address bits for the RAM ICs and the third bit is a chip select used to select one of the RAM devices via the 1Q and $\overline{1Q}$ outputs of U140. When data bit D2 is HI, U310 will be enabled; when LO, U300 will be enabled.

The processor then reads from or writes to the desired RAM location by outputting the desired address within the address-decoded space between D800 and DFFF.

When the option RAMs are being addressed, $\overline{\text{OPTRAM}}$ will be LO and the resulting buffered signal ($\overline{\text{OPTRAMB}}$) is applied to both RAM devices, U300 and U310. This enable, along with the latched enable from U140, allows the addressed location in the selected RAM device to be written to or read from, depending on levels of the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ enable lines from the processor board.

When instrument power is turned off, a special sensing IC in the Battery Backup circuit will set the enables to U130 HI before the power supplies decay to the point where data and enable levels go out of tolerance. Disabling U130 also disables the RAM ICs ($\overline{\text{OPTRAMB}}$ and $\overline{\text{SYSB}}$ goes HI) and prevents erroneous data from being written into the RAMs as the power goes down. When the power supplies finish decaying, power to U130 is removed and the pullup resistors R130C and R130D keep the RAMs disabled. As long as these RAMs are disabled, they draw minimal supply current, allowing the Battery Backup circuit to maintain RAM contents for extended periods of time with instrument power off.

Battery Backup

The Battery Backup circuit provides a standby power source used to maintain the contents of the system and option RAMs when instrument power is off. This allows stored waveform data and instrument setup to be saved for extended periods of time.

During normal instrument operation, the $+5\ V_{D8}$ power line will be operating within its tolerance limits. This initially pulls the V_{TH} sensing input to approximately $+1.25$ volts through resistive divider R100, R102, and R104. This level is compared to an internal voltage reference of $+1.15$ volts and switches the V_O control output LO, indicating that the normal power supply is operational.

When V_O goes LO, an internal transistor turns on and switches the V_{HYS} output to the $+5$ volt supply level, raising the V_{TH} input level to about $+1.3$ volts. This hysteresis provides positive, noise-free switching of the output control level. The LO V_O output also turns on transistor switch Q120 and the $+5\ V_{11}$ and $+5\ V_{12}$ supply lines are connected to the normal $+5\ V_{D8}$ supply line. Battery BT110 charges through CR110, R110, and R112 as long as normal instrument power is on.

When instrument power is turned off, the $+5\ V_{D8}$ supply line voltage will drop as power is drawn from its storage capacitors. When the voltage level reaches approximately $+4.3$ volts, the level at the V_{TH} input drops below the internal $+1.15$ volt level and the V_O output goes HI. This is the HI POWER OFF SENSE level used to disable the reading and writing to the system and option RAMs (see Extended Memory description).

This HI also turns Q120 off and battery BT110 begins supplying a positive voltage to the $+5\ V_{11}$ and $+5\ V_{12}$ inputs through R112. This is the positive standby voltage and it is used to maintain the contents of the system and option RAMs when normal power is off. Switch S130 is used to clear the contents of these RAMs (for diagnostic purposes) when power is off.

GPIB

The GPIB (General Purpose Interface Bus) circuit provides the communication link necessary for an external GPIB controller to read acquired data points from waveform memory. All interface and control functions of the 336 GPIB circuitry are adherent to IEEE standard 488-1978 (and the 488-1980 supplement).

THE IEEE STANDARD. The IEEE 488-1978 standard defines a byte-serial bit-parallel interface system electrically, functionally, and mechanically as well as specifying terminology and system limitations. This system implements a 3-wire handshake system with each data transfer from a "talker" to one or more "listeners". A "talker" is a GPIB device sending data while a "listener" is one that receives data from a "talker". All GPIB information is transferred at standard TTL levels using negative logic (i.e., LO = TRUE).

The GPIB interface has 16 external connections which are used for three separate types of functions. Inputs DIO1 through DIO8 (data input/output) are used specifically for transfer of data between GPIB devices.

Five other lines are used to manage the flow of information over the interface lines. The ATN (attention) level, when active, disables the current talker and listeners and makes all devices listen to the controller. IFC (interface clear) is used to put the interface system into a known quiescent state. The SRQ (service request) line is used to indicate to the controller that a device on the bus is in need of service and an interrupt is requested (the controller determines which devices may talk or listen at any time). The REN (remote enable) command selects either a remote or local source of device programming. The EOI (end or identify) line is used to signal the end of a multiple byte transfer and is used in conjunction with ATN to execute the parallel polling sequence.

The three remaining lines are associated with the handshake process and are the DAV (data valid), NRFD (not ready for data), and NDAC (data not accepted) lines. Their timing relationships during the handshake process are shown in Figure 3-7. Each data byte transferred by the interface system uses the handshake process to exchange data between source (typically a talker) and acceptor (typically a listener). The following list of events is related by number to the state changes shown in Figure 3-7 and the flowchart shown in Figure 3-8.

THE HANDSHAKE PROCESS. A typical handshake is as follows:

1. The source (talker) initializes the active LO DAV (data valid) to a HI level, indicating that data is not valid.

2. The acceptors (listeners) initialize the active LO NRFD (not ready for data) level to a LO (none are ready for data) and set the active LO NDAC (data not accepted) level to LO (none have accepted data).

3. The source checks for an error condition (both NRFD and NDAC at a HI level) and then sets a data byte on the DIO (data in/out) lines. After data has been placed on the DIO lines, the source delays to allow the data to settle on these lines.

4. When the acceptors have all indicated readiness to accept the first data byte, the NRFD level goes HI.

5. The source, upon sensing the HI NRFD level, sets the DAV level to a LO, indicating that the data on the DIO lines has settled and is valid.

6. The first (fastest) acceptor sets the NRFD level LO, indicating that it is no longer ready for new data, and accepts the present data. The remaining acceptors follow at their own rates.

7. The first acceptor sets its NDAC level to a (passive) HI, indicating that it has accepted the data. (NDAC remains LO due to the other acceptors actively driving NDAC LO. The term "passive" means that if any other device is "actively" driving this line to the opposite state, the passive level is overridden.)

8. As the last (slowest) acceptor accepts the present data, the NDAC level goes to a (passive) HI, indicating that all acceptors have accepted the data.

9. The source, having sensed the HI NDAC level, sets DAV HI. This indicates to the acceptors that the data on the DIO lines must now be considered invalid.

10. The source may change the data on the DIO lines at this time and now delays to allow this data to settle if changed.

11. The acceptors, upon sensing the HI DAV level (step 9 above), set the NDAC level LO in preparation for the next cycle. The NDAC line goes LO when set by the first acceptor.

12. The first acceptor indicates that it is now ready for the next data byte by settings its NRFD level to a (passive)

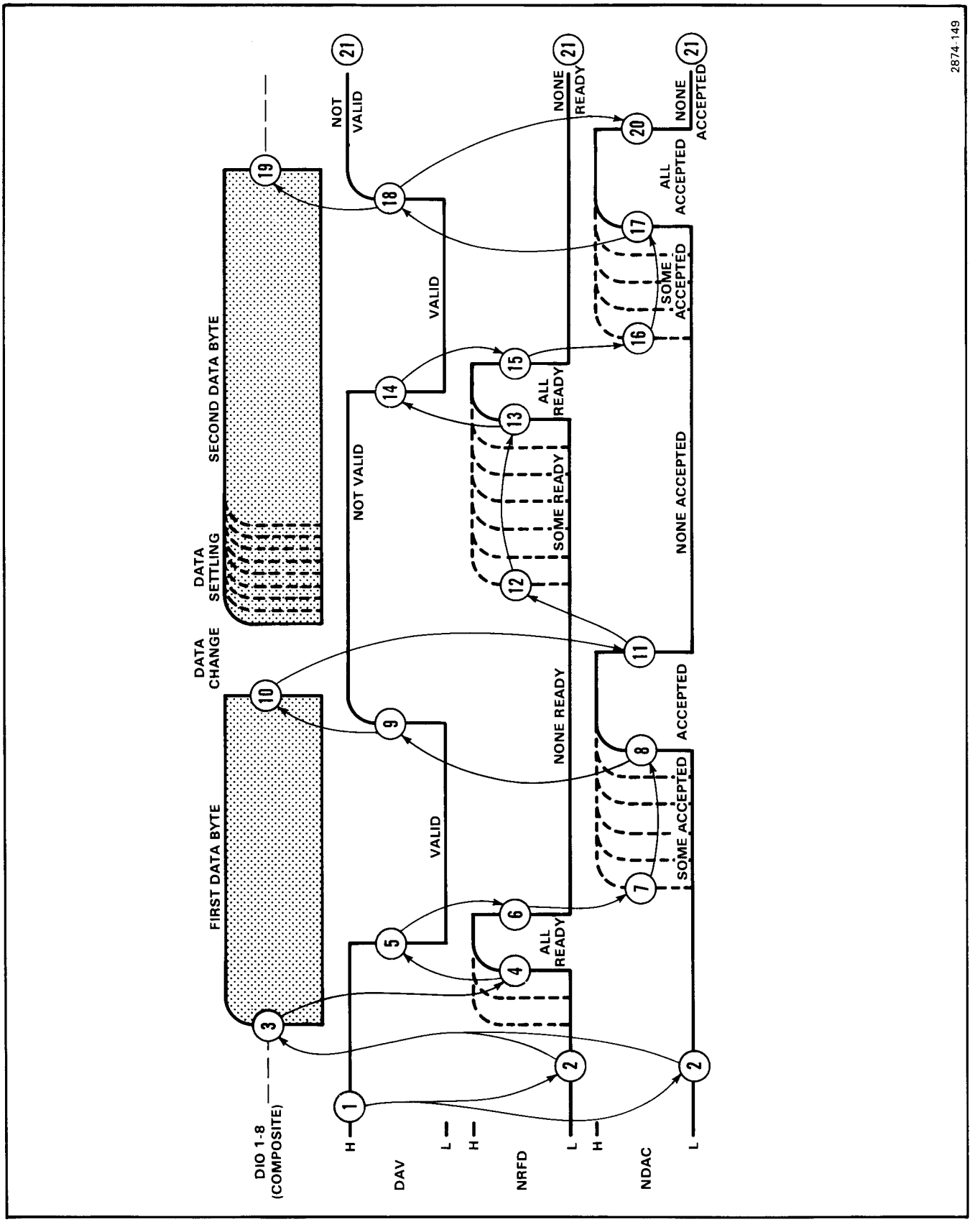
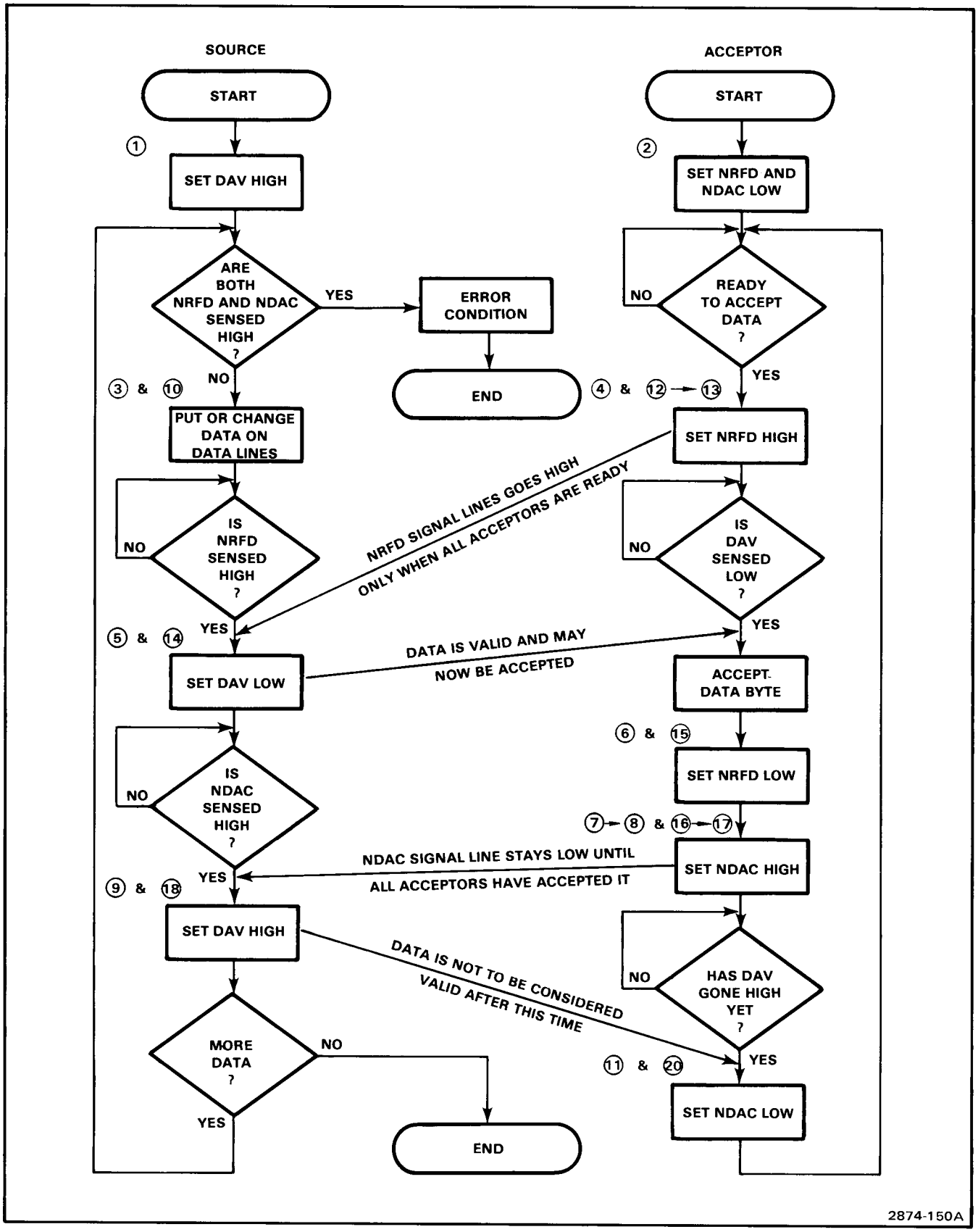


Figure 3-7. GPIB Timing.



Figue 3-8. Flowchart of GPIB Handshake.

HI. (NRFD remains LO due to other acceptors actively driving it LO.)

13. When the last acceptor indicates that it is ready for the next data byte, the NRFD level goes (passive) HI.

14. The source, sensing that NRFD is HI, sets the DAV level LO, indicating that the new data on the DIO lines has settled and is valid.

15. The first acceptor sets the NRFD level LO, indicating that it is not ready to accept any change of data, then accepts the present data. The other acceptors follow at their own rates.

16. The first acceptor sets its NDAC level to a (passive) HI, indicating that it has accepted the data (as in step 7 above).

17. The last acceptor sets the NDAC level (passive) HI, indicating that it has accepted the data (as in step 8 above).

18. The source, having sensed that NDAC is HI, sets DAV HI (as in step 9).

19. The source removes the data byte from the DIO signal lines after setting DAV HI.

20. The acceptors, upon sensing the HI DAV level, set NDAC to a LO level in preparation for the next cycle.

21. Note that all three handshake lines are at their initial states (as in steps 1 and 2 above).

GPIA. The GPIA (general purpose interface adapter) consists of U400, a 40-pin IC specifically designed for GPIB applications. The purpose of the GPIA is to provide interface between the IEEE 488 Standard instrument bus and the Microprocessor.

The sixteen pins of this IC related directly to the 16 pins of the GPIB interface connector, discussed in the IEEE 488-1978 Standard description above, and are bi-directionally buffered to the GPIA IC for control of data transfer to and from the Data Bus.

The $\overline{RD}$ and $\overline{WR}$ lines, in conjunction with the three register select pins (RS0, RS1 and RS2) tied to the address bus of the Microprocessor system, address one of 16 registers internal to the GPIA IC. These registers are used for data storage, status monitors, and interrupt functions.

The RESET line is used to initialize the GPIA chip when power is first applied and holds the IC reset until C404 can charge LO through R404. The $\overline{CS}$ (chip select) input is used to select the GPIA IC and must be LO to select the device. The $\overline{GPIBINT}$ (GPIB interrupt) line is tied to the interrupt logic of the Microprocessor and, when LO, indicates that the GPIA requires service by the Microprocessor. The $T/\overline{R}_1$ (transmit/receive) output provides selection of whether 336 is transmitting or receiving data over the GPIB by controlling the bi-directional buffers to the GPIB. The Clock input for the GPIA stage is CHOPCLK, which runs at one-half the speed of the Microprocessor clock and synchronizes all operations to the processor.

UNBLANKING LOGIC AND CHART OUT ◇17◇

The Unblanking Logic (diagram 17) controls the crt beam unblanking and intensity for the various crt display modes. The Chart Out circuit allows the stored waveform data to control an external X-Y Plotter. Other circuitry on this schematic controls selection of the vertical and horizontal deflection signals.

Decode

The Decode circuit generates signals used to control the horizontal, vertical, and chart out circuits by address decoding address lines A3 and A4 when the H-V MODE CONT (horizontal-vertical mode control) enable is present.

Control Latch

The Control Latch allows the Microprocessor to store control bits used in setting up the operating modes of the vertical, horizontal, and chart out circuits. The stage consists primarily of latch U180. Data from data line D7 is written to the location addressed by address lines A0-A2 when the address-decoded enable $\overline{MODE\ CONT}$ is present. The stored data at the outputs is used to set up operation of other circuitry.

Display Clock

The Display Clock generates the time-related signals used to control the various functions associated with each of the several realtime display modes. These functions include vertical mode selection, horizontal mode selection, and Z-axis blanking for chop and alternate modes. The Display Clock consists primarily of two counters, one for generating chop timing and one for generating alternate (ALT) timing, and a data selector used to route these timing signals to other circuitry.

Depending on the desired display mode, the four control signals from the outputs of U410 are selected from one of the two counters within U400 by the ALT/$\overline{\text{CHOP}}$ signal applied to select input pin 1.

For alternate displays, the ALT/$\overline{\text{CHOP}}$ line will be HI, selecting the signals at U410's B inputs. The HI ALT/$\overline{\text{CHOP}}$ level, also applied to the reset input for counter 1 of U400, holds all of the 1Q outputs reset (LO).

Two-line-to-four-line decoder U110 is configured to detect the end of A SWP GATE when realtime displays are in progress. When realtime displays are to be produced, the processor will set the NONSTORE bit to the A1 select of U110B HI. This HI, along with the HI applied to the A0 select input, addresses output Y_3; but since the decoder is not enabled yet (A SWP GATE still HI), the Y_3 output will stay HI. When the A SWP GATE ends, it goes LO, enabling the addressed Y_3 output to go LO. When the A SWP GATE returns HI, so will the Y_3 output.

This NONSTORE-enabled sweep gate signal is routed through U410 to the Y_1 output of U410 and is used to clock the currently selected vertical mode data (from U420) into the Vertical Mode Control latch U490 at the end of each A SWP GATE. The same signal also clocks counter 2 within U400, causing its 2Q outputs to increment in a binary fashion at the end of each A SWP GATE.

The two LSBs of this counter (2Q0 and 2Q1) are routed through U410 and are used to continuously cycle through the four bytes of vertical mode data stored in the 4-word-by-4-bit register file (U420) of the Vertical Mode Control stage. The third bit of the counter 2Q2 is applied to the Horizontal Mode Control stage and is used to alternately select the A and B sweeps.

The counting configuration just described causes the four traces defined by the four words of mode data stored in U420 to be displayed against the A sweep ramp, followed by the same four against the B sweep ramp, followed by the same four against the A sweep ramp, and so on.

Chop operation is similar to alternate operation, just described. For chopping, the ALT/$\overline{\text{CHOP}}$ level is LO, removing the reset from counter 1 within U400 and selecting U410's A inputs. The clock signal for counter 1 is derived from the Microprocessor clock and runs at approximately 1.2 MHz. The two MSBs of this counter (1Q2 and 1Q3) are routed through U410 to U420 and continuously cycle through the four bytes of vertical mode select data at a 150 kHz rate. The LSB, 1Q0, is routed to U490 and clocks the currently addressed vertical mode data into U490 at a 600 kHz rate. The 1Q0 and 1Q1 outputs are ANDed by U402B in the Unblanking Logic and produce a 300 kHz blanking pulse that blanks the crt for a brief period each time the vertical mode data changes.

The second counter within U400 is still enabled and continues counting completed A sweep gates. Since U400's 2Q2 output is still routed through U410 to the Horizontal Mode Control stage, operation is the same as for alternate sweeps; i.e., four sweeps will be displayed with A sweep ramp alternated with four sweeps using B sweep ramp.

Vertical Mode Control

The Vertical Mode Control stage generates the realtime vertical select signals at the rates determined by the Display Clock stage. Four bytes of mode-sequencing data are written from the processor to a 4-word-by-4-bit register file. This sequencing data is then continuously cycled through (by the Display Clock signals) and produces the proper sequencing of the vertical channels for the various display modes.

Since the read addresses RA_0 and RA_1 of the 4-by-4 register file U420 are continuously cycled by the Display Clock, the 4 bytes of data stored in the register are cycled through at the device's Q outputs. This cycling action is what allows the vertical mode changes of each display mode to be repeated, once the display mode is set by the Microprocessor.

To set the channel sequencing associated with any display mode, the Microprocessor writes four bytes of channel-sequencing data to the four sequential locations of the register file, using the address-decoded write enable from the Decode stage. When $\overline{\text{YCONT}}$ (vertical control) applied to pin 12 of U420 goes LO, the four bits of data from the processor on data lines D4-D7 are written to the location addressed by address bits A0 and A1. When $\overline{\text{YCONT}}$ returns HI, the data will remain stored at that location. Each bit of the byte is associated with a control line that determines whether the related vertical channel should be turned on for that portion of the display sequence. Four bytes of data, defining the sequence of each of the vertical channels, are written into the sequential locations of U420 in this manner. The bytes are then sequentially output as addressed by the read address inputs RA_0 and RA_1, producing four distinct times at which the vertical select data can change the display.

These outputs are latched into U490 either at the end of each chop clock or at the end of each sweep, depending on the mode of the Display Clock. Three of these bits are directed to multiplexer U480 for control of the vertical channel selection; while the fourth bit, STORAGE/$\overline{\text{REAL}}$, is directed to the Blanking Logic for producing storage displays.

For producing displays when acquisitions are not being made, the $\overline{\text{DONE}}$ line from the acquisition system will be LO. This selects the A inputs of U480 and allows the vertical mode control data from U420 to control vertical channel selection. During acquisitions, the display will be blanked and the $\overline{\text{DONE}}$ signal will be HI. The selection of CH 1 and CH 2 is determined by the SAVE signal; and for normal acquisitions, the SAVE line toggles at the same rate as the LSB of Display Address Counter. This alternately selects CH 1 and CH 2 for application to the sampler. For envelope mode acquisitions, the SAVE signal stays LO until all points of the CH 1 envelope have been acquired and then switches HI to deselect CH 1 (and select CH 2).

Horizontal Mode Control

The Horizontal Mode Control circuit controls sweep selection when displaying realtime waveforms. Data selector U450 is enabled when the $\overline{\text{REAL}}$ (realtime display) signal is LO. When enabled, the A and B select bits from the Control Latch select two of the possible eight inputs as the A SEL and B SEL signals. Table 3-4 illustrates mode selection.

The alternating A/$\overline{\text{B}}$ signal applied to pin 3 of U450 and pin 11 of U402C is derived from the Display Clock and alternately selects the sweeps when in A alternate B mode.

Unblanking Logic

The Unblanking Logic provides unblanking and intensity control of the crt Z-axis circuit. With none of the unblanking circuitry activated, a blanking current is supplied to the Z-Axis Amp (diagram 18) through resistor R450. To unblank the crt beam to the desired intensity level, the Unblanking Logic will sink varying amounts of this blanking current away from the Z-Axis Amp, dependent on the type of unblanking to be done.

The biasing configuration of transistor Q600 in the Z-Axis Amp circuit (diagram 18) holds the voltage at the output of the Unblanking Logic (at pin 2 of P420) at a constant level. With all unblanking circuits inactive, approximately 4.9 mA of current is sourced to the Z-Axis Amp, blanking the crt. As any of the unblanking circuits are activated, a portion of this blanking current will be sinked away from the Z-Axis Amp, causing the intensity to increase. Before the Z-Axis Amp will come out of its blanked condition, the unblanking logic must sink at least 2.6 mA away from the output node. Maximum intensity will occur when the entire 4.9 mA is sinked from the node by the Unblanking Logic.

The unblanking currents are controlled by the outputs of U430, U440, and U470; which are in turn controlled by the rest of the Unblanking Logic. NAND gates U472 and U470 control unblanking for realtime displays. The Horizontal Mode Control stage determines which of the available sweep ramps (A or B) should be used as the sweep source and is explained in that description.

For A sweep unblanking, the NONSTORE control bit and the A SEL signal applied to U470B will be HI. When the A SWP GATE signal goes HI, U470B's output will go LO, forward biasing CR444 and drawing current through R474. The current through R474 is approximately 2.9 mA, enough to barely unblank the Z-Axis Amp. The additional current used to set the intensity of the crt beam is sinked through U442A and R446 to pin 4 of U440.

An additional current will be sinked from the node through CR442 and R472 when U470A detects the B SWP GATE with the A sweep ramp sweeping the display (A SEL HI). The latch formed by U472A and U472C detects any occasion when the A SWP GATE signal ends before the B SWP GATE signal and is used to turn off B and A intensified sweeps when the B delayed time extends beyond the end of A sweep. Since the A sweep is always initiated before the B sweep can run, the LO B SWP GATE signal applied to U472C when the A SWP GATE signal goes HI will set the enable at pin 8 of U472C HI. This output will remain HI, keeping U470C and U470A enabled until the situation arises where the A SWP GATE ends before the B SWP GATE ends.

Table 3-4
Horizontal Mode Selection

Select Input		Output		Mode
A	B	A SEL	B SEL	
0	0	0	0	X-Y
0	1	0	1	B only
1	0	1	0	A only
1	1	A/$\overline{\text{B}}$	B/$\overline{\text{A}}$	A alt B

If this occurs, as would happen with long delay times between the start of A sweep and the start of B sweep; the falling edge of A SWP GATE would set the output at pin 8 of U472C LO, disabling U470A and U470C. Since these gates control unblanking for the B only and B intensification sweeps, the intensified portion of A alt B sweeps and the corresponding B only sweeps will end coincident with the end of A SWP GATE.

For B only displays, the B SEL input and the enable from U472C to U470C will both be HI. When the B SWP GATE occurs, the output of U470C goes LO, sinking current away from the output node via CR440 and R470. This current (approximately 2.9 mA) will barely unblank the Z-Axis Amp while the current sinked through U442A and R446 sets the display intensity. B blanking will occur either when the B SWP GATE ends or when the end of A SWP GATE removes the enable coming from U472C (described above), whichever occurs first.

Intensity for these real-time displays is set by U442A, U442B, R446, and the associated circuitry. When real-time sweeps are being displayed, the readout is blanked and the RO BLANK enable applied to U440 is LO. This enables the IC, and the LO STORAGE/REAL control bit from the Vertical Mode Control stage selects the A inputs of U440. For real-time displays, the NONSTORE control bit applied to the A_1 input of U440 is HI, resulting in a LO at the Y_1 output. This LO forward biases transistor U442A via R446 and sinks a portion of the current away from the output node, depending on the INTENSITY level applied to the base of U442A. The INTENSITY level is set by the front-panel INTENSITY control and allows the operator to set the drive to the Z-Axis Amp during real-time displays.

The EXT Z-AXIS IN signal applied to the base of U442B allows positive-going signals to reduce (and blank) the realtime display intensity. When the EXT Z-AXIS IN signal level at the base of U442B approaches the INTENSITY level applied to the base of U442A, a portion of the current flowing through R446 begins to come from Q442B, reducing current flow in U442A. The more positive the external signal goes, the more the intensity current through U442A will be reduced, until blanking occurs.

Blanking of the real-time display during the period when a data point is being acquired is done by pulling the ACQ BLANK line HI. This reverse biases transistor U442A, closing the intensity current-sink path.

Chop blanking of the real-time display is controlled by U402B, part of U430, and Schottky diode CR450. When chop mode is selected, the processor will set the CHOP BLK EN (chop blank enable) bit applied to U402B HI. The approximate 300 kHz and 600 kHz clocks applied to the other inputs of U402B result in a narrow, 300 kHz chopping pulse at its output.

Since, for real-time displays, U430's A inputs will be selected (readout is blanked and RO BLANK is LO), the output at Y_4 will be a narrow, positive-going blanking pulse. This CHOP BLANK pulse will forward bias diode CR450 and source the extra current to current-sinking (unblanking) circuits, overriding them. This blanks the crt as the vertical mode alternates between CH 1 and CH 2 displays. When the CHOP BLANK pulse returns LO, normal display intensity is restored.

When magnified displays are being displayed, the MAG bit applied to U440 will be HI and an additional current will be sinked through CR448 and R442 to the Y_2 output of U440. This turns up the beam intensity to compensate for the faster sweep rate and holds the intensity of the magnified display near that set for the unmagnified display.

Another type of real-time display is the X-Y mode. Since none of the sweeps are enabled for X-Y displays, another unblanking path is provided. With the XY ENABLE bit set HI, indicating an X-Y display, unblanking current will be sinked to the Y_3 output of U440 through CR446 and R444. Since an X-Y display does not have the holdoff times associated with sweep displays, the value of R444 is slightly larger than those of R474 and R470 used for unblanking the A and B sweep displays, providing the same relative display intensities. This XY unblanking signal is also used to generate the XY SEL signal in the Vertical Mode Control stage and may only be asserted when the STORAGE/REAL select signal to U440 is LO.

The Y_4 output of U440 is used to control the intensity of stored waveform displays. With the STORAGE/REAL select input LO, the Y_4 output will be HI and the storage intensity current path through U442C and R440 will be closed. With the select input HI, however, the real-time intensity and XY intensity paths will be closed and the display intensity will be controlled by U442C and its associated components.

To unblank the Z-Axis Amplifier for waveform displays, the WFM BLANK signal must be HI. This produces a LO at the Y_4 output of U440 and forward biases U442C. The unblanking current is sinked to the Y_4 output through U442C and resistor R440.

Since the stored waveform data is read from memory and displayed alternating CH 1 with CH 2 (either of which may be blanked), the overall time that a given channel's data is unblanked on the crt is about half that of the corresponding real-time single-channel display; therefore, the value of stored waveform unblanking resistor R440 is about half that of real-time unblanking resistors R470 and R474.

To horizontally magnify a stored waveform display, the MAG control bit applied to the B_2 input of U440 will be set HI. This causes the Y_2 output to sink an intensifying current, as described above for real-time displays.

Blanking of the stored waveform displays is done by setting the $\overline{\text{WFM BLANK}}$ signal from the Display Control stage (diagram 14) LO. This results in a HI at the Y_4 output of U440 and reverse biases U442C, turning off the unblanking current path.

Blanking and unblanking of the readout display is handled in a similar fashion. When a readout dot is being displayed, the $\overline{\text{RO BLANK}}$ signal will be HI. This disables U440 and selects the B inputs of U430. With the B_1 input tied HI, the Y_1 output will be LO, forward biasing transistor U442D. The amount of unblanking current drawn from the output node through U442D and R430 is dependent on the transistor's base bias voltage set by the RO INTENSITY preset, R924. When the $\overline{\text{RO BLANK}}$ line is set LO by the Display Control stage (diagram 14), the A_1 input of U430 is selected and the Y_1 output will go HI. This reverse biases transistor U442D and blanks the readout display.

The Y_2 and Y_3 outputs of U430 are used to generate two control signals used for selecting real-time or storage display modes. When readout dots are being displayed, the HI $\overline{\text{RO BLANK}}$ signal will select the B_2 input and a LO REAL control signal will result at the Y_2 output of U430, indicating that this is not a real-time display. This output is routed to U430's A_3 and B_3 inputs and is inverted to the $\overline{\text{REAL}}$/STORE signal at the Y_3 output. These signals drive other circuits that disable the real-time displays.

When the readout is blank ($\overline{\text{RO BLANK}}$ LO), either realtime or storage waveforms may be displayed. The STORAGE/$\overline{\text{REAL}}$ signal applied to the A_2 input of U430 controls the signals at the Y_2 and Y_3 outputs. The STORAGE/$\overline{\text{REAL}}$ signal is produced from the Microprocessor-generated vertical mode data stored in the Vertical Mode Control stage and allows selection of real-time waveform, stored waveform, or alternating real-time stored waveform displays.

Chart Out

The Chart Out circuit allows the stored waveform data to be output to an X-Y plotter under control of the Microprocessor. The stage consists of two D-A converters (DAC) that convert the Microprocessor data written to them to two analog voltages representing the horizontal and vertical coordinates of the stored waveform data points.

When writing data to the Chart Out circuit, the Decode stage will generate a chip select to either DAC U100 or DAC U140, depending on whether horizontal or vertical data is being written to the DACs. When the processor write pulse ($\overline{\text{WR}}$) goes LO, the data on the data bus is written to the storage register internal to the selected DAC and the output voltage goes to the corresponding voltage level. Transitions between consecutive steps are smoothed by frequency-compensated operational-amplifier buffers U160A and U120B.

The two DACs are used to set the Delay Time Position and Trace Sep control voltages when the plotter output is not being used. Analog switch U220A and NAND-Gate U402A are used to apply DAC U140's output to the trace separation circuit when enabled by a HI TRACE SEP EN bit with the A/$\overline{\text{B}}$ select line HI. This enables the trace separation voltage to the Horizontal Preamp during alternate A sweeps and allows the A sweeps to be positioned below the B sweeps.

Inverting buffer U160B and its associated resistors are used to develop the DELAY TIME POSITION control voltage for A intensified by B and B delayed displays (when waveform data is not being output to the plotter). The DELAY START and DELAY STOP adjustments are set at the time of calibration to match the DAC output values to the limits of the A sweep.

Z-AXIS AMPL, CALIBRATOR, HIGH VOLTAGE, AND CRT ◈18

The Z-Axis Ampl (diagram 18) converts the current signal from the Unblanking Logic (diagram 17) to a voltage signal used to control the intensity of the crt display. The High Voltage power supply provides the various high voltage operating potentials required by the crt. The crt provides the operator with a visual display of the stored and real-time waveforms, as well as alphanumeric display of the oscilloscope setup conditions and of the operating mode menus. The Calibrator circuit provides 0.3 volt peak-to-peak, square-wave output signal at approximately 1 kHz to the instruments side panel.

Z-Axis Ampl

The Z-Axis Ampl converts the signal currents from the Unblanking Logic (diagram 17) to the voltage signal used to control the crt intensity. The bias network at the base of Q600 holds the base voltage at approximately 2 volts, and the emitter is held at a constant level one diode drop higher. The Z-AXIS current from the Unblanking Logic develops a

voltage across resistor R606 and, for blanked displays, will reverse bias diodes CR604 and CR608. Schottky diode CR600 prevents this voltage from exceeding approximately +0.4 volt.

Transistors Q620, Q640, Q660, and their associated components form an inverting current-to-voltage amplifier. For blanked displays, the output voltage at the collectors of Q640 and Q660 will go to a level of approximately +4.2 volts, providing bias current for Q620 through the feedback resistor R614 to the bias resistor R610. Since diodes CR604 and CR608 are reverse biased, only this bias current will flow in the feedback resistor and only a small voltage will be developed with respect to the fixed base level of Q620 (two diode drops above ground) to the output of the amplifier.

To unblank the crt, the Unblanking Logic will reduce the Z-Axis current flowing through Q600 and R606. This lowers the voltage at the cathode of CR604 and forward biases both CR604 and CR608, sinking bias current away from Q620. The lowered base bias on Q620 forces the collector of Q640 HI in an attempt to maintain the forward-bias current through R610. The voltage at the output will rise to a level that will source a current through R614 equal to the normal bias current for Q620 plus the additional current required to increase the voltage drop across R606 to the level that begins to turn diodes CR604 and CR608 off. The maximum output voltage will approach +60 volts and is produced when all of the current for R606 is sourced through R614 (along with the normal bias current through R610). The crt intensity may be set between either of these limits, depending on the value of the combined intensity-blanking current from the Unblanking Logic.

Grid Bias and DC Restorer

The Grid Bias and DC Restorer circuit provides crt control-grid bias and couples both the dc and low-frequency components of the Z-Axis drive signal to the crt control grid. The circuit operates by impressing the grid bias setting and the Z-Axis drive signal on an ac waveform. This shaped waveform is then ac coupled to the high-potential crt environment where the dc components of the original signal are restored.

An ac-drive voltage of approximately 500 volts peak-to-peak is applied to the Grid Bias and DC Restorer circuit from pin 4 of plug P10. This signal is coupled to the junction of a positive clamp (made up of VR38, VR40, CR36, and their associated components) and a negative clamp (CR10) by capacitor C10 and resistor R10.

The positive clamp is used to set the nominal GRID BIAS level, which in turn determines the overall crt intensity. Positive clamping of the ac waveform occurs when diodes CR36 and VR38 become forward biased. Depending on the setting of Grid Bias potentiometer R40, connected across the +75 volt reference (VR40), this clamping will occur between +75 volts and +150 volts.

Clamping of the negative-going waveform is done by diode CR10. Clamping level is determined by the level of the INTENSITY signal from the Z-Axis Ampl. Figure 3-9 illustrates the shaped waveform applied to pin 9 of the High-Voltage Module, U100.

This shaped waveform is ac coupled to the high-potential crt environment by the input capacitor (A) at pin 9 of the DC Restorer within High-Voltage Module U100. Initially, this capacitor charges to a level determined by the difference between the Z-Axis signal level and the −1960 volt grid potential. Capacitor D charges to a similar level through resistor E.

When the ac waveform applied to pin 9 begins its transition from the lower clamped level (set by the Z-Axis signal) toward the upper clamped level (set by the Grid Bias circuit), the charge on the input capacitor increases. The additional charge is proportional to the voltage difference between the two clamped voltage levels.

When the ac waveform begins its transition from the upper clamped level back to the lower clamped level, diode B becomes reverse biased. Diode C becomes forward biased and an additional charge, proportional to the negative excursion of the ac waveform (difference between the upper clamped level and the lower clamped level), is added to capacitor D through diode C. The amount of charge added to capacitor D depends on the varying Z-Axis signal from the Z-Axis Ampl, since it sets the lower clamping level of the ac waveform. This added charge determines the potential of the INTENSITY control grid with respect to the crt cathode.

The potential difference between the control grid and the cathode controls the beam current and thus the display intensity. With no Z-Axis signal applied (display blanked), capacitor D will be charged to its maximum negative value, since the difference between the two clamped voltage levels is at its maximum value. This is the minimum intensity condition and reflects the setting of the Grid Bias potentiometer. During calibration, the Grid Bias potentiometer is adjusted so that the difference between the upper clamping level (set by the Grid Bias potentiometer) and the "no signal" level of the Z-Axis drive signal produces a control grid bias that barely shuts off the crt electron beam.

To turn on the crt beam, the Z-Axis signal will unblank and rise to an intensity level controlled by the Unblanking

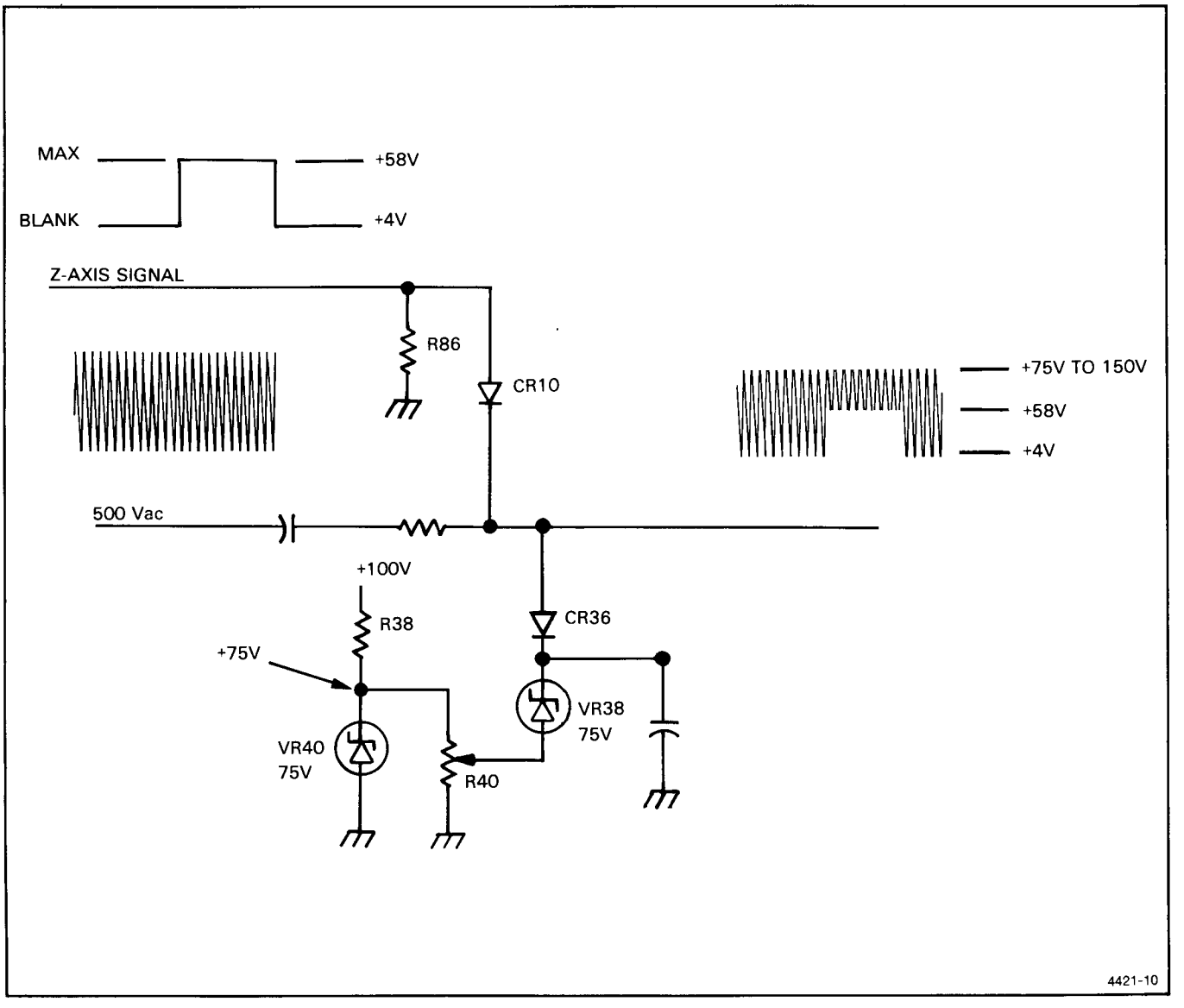


Figure 3-9. Composite Grid Bias/Intensity waveform.

Logic. This increased signal amplitude decreases the difference between the upper and lower clamped levels of the ac waveform, and less charge is added to capacitor D. The decreased voltage across capacitor D decreases the potential difference between the control grid and the cathode, and more crt beam current is allowed to flow. Increased beam current increases the crt display intensity.

During the periods that capacitor A is charging and discharging, the control-grid voltage is held stable by the long-time-constant discharge path of capacitor D through resistor E. Any charge removed from capacitor D during the positive transitions of the ac waveform will be replaced on the negative transitions.

The fast-rise and fast-fall transitions of the Z-Axis signal are coupled to the crt control grid through capacitor D and capacitor C105. This ac-coupled fast-path signal quickly sends the crt electron beam to the new intensity level, then the slower DC Restorer path "catches up" to handle the dc and low-frequency components of the Z-Axis drive signal.

Focus Limiter and DC Restorer

The Focus Limiter and DC Restorer provides the level shifting of the operator-settable FOCUS voltage to the high-potential environment of the crt. Shifting is done in a manner similar to that just described for the Grid Bias and DC Restorer stage. The active positive clamp, made up of Q50, Q54 and their associated components, provides a variable voltage clamp that limits the positive swing of the ac waveform. Diodes CR60 and VR58 limit the negative swing.

The 500 volt ac signal is applied to the clamping node through R20, R22, and C22.The negative excursion of the ac waveform is clamped near −56 volts by zener diode VR58 and diode CR60. The positive excursion is limited at the level where the feedback current in R54, along with the current from the front-panel FOCUS pot, turns both Q50 and Q54 on.

With the output level below the clamping level, the voltage from the front-panel FOCUS pot will be divided by bias divider R50-R52. The resulting voltage at the gate of Q50 will tend to be below the pinchoff voltage of the FET and Q50 will be off. This also keeps Q54 off.

As the ac waveform rises positive, an additional current will be sourced to R52 through feedback resistor R54. This rising voltage causes the bias voltage on the gate of Q50 to go positive toward the FET's pinchoff voltage until the FET turns on. With the FET on, Q54 also turns on, and any currents greater than those required to keep Q50 turned on will be sinked through R56 and Q54 to ground. This is the positive clamping condition, the level of which may be varied by increasing or reducing the current to R52 from the front-panel FOCUS control (vary control setting).

When the ac waveform drops below the set clamping level, current through R54 will be reduced below the level necessary to keep Q50 (and thus Q54) turned on. The positive- and negative-clamped ac waveform is applied to pin 7 of U100 and is dc restored in a manner similar to that described earlier for the Grid Bias and DC Restorer stage. The resulting high-potential output is used to control the FOCUS element of the crt.

High Voltage Regulator

The High Voltage Regulator monitors the cathode supply voltage and draws current away from the regulator's voltage-doubler stage to keep the output at its nominal operating level of −1960 volts. The −1960 volt output is applied to the crt's cathode/heater element to provide the negative drive potential and is used as a reference for the INTENS and FOCUS control grids (see the Grid Bias and Focus Limiter descriptions).

The 2000 volt ac signal from P122 is used to develop the −1960 volt supply voltage. On the first positive half cycle, diode G becomes forward biased, but since the output level applied to the inverting input of regulator U80 is low (too positive), transistor Q72 will be turned on and most of the current that might have otherwise charged capacitor K positive is shunted away through resistor H. This leaves a slight positive charge on capacitor K and a large charge of almost −1000 volts on input capacitor F.

On the following negative half cycle, the negative component of the ac waveform (−1000 volts) is added to the charge already stored on input capacitor F and the series combination of capacitors J and K is charged up to almost −2000 volts via diode I. Output storage capacitor M is also charged to this level through resistor L.

Since the output level now tends to negative, the regulating operational amplifier U80 will turn transistor Q72 off. On the following half cycle (positive), diode G will be forward biased; and, with Q72 off, negative charge will be subtracted from (positive charge added to) capacitor K until the output level reaches −1960 volts. At this time U80 will turn Q72 back on to sink all extra positive (subtractive) current away from capacitor K, charging input capacitor F to a voltage slightly less than −1000 volts.

As before, the following negative half cycle adds its charge to that already stored on input capacitor F and pumps the output voltage back up to compensate for any charge drawn off between cycles. After several similar cycles, the circuit reaches an equilibrium where the charge added on each cycle precisely matches that drawn from the output on the previous cycle and the supply is in regulation.

The regulation point is determined by the sensing divider R82 and resistor N within the HIGH-VOLTAGE MODULE. If the sensed output level tends low (too positive), transistor Q72 turns on so the charge stored across input capacitor F will be greater on the next cycle, restoring the output to its proper level. If the output tends high (too negative), the transistor will be turned off, allowing capacitor K to charge slightly positive, thus reducing the charge stored on input capacitor F on the following cycle. As before, this action will return the output to its regulated value in the course of a few cycles.

Diode CR68 serves to shift the lower extreme of the sine wave input from an approximate -250 volts up to 0 V. This shift ensures proper circuit biasing when either high-line or low-line power sources are used (since some difference in the ac signal amplitudes will occur relative to the opposite line configuration).

Heater Rectifier/Cathode

The Heater Rectifier/Cathode circuit develops a dc voltage for heating the combination heater-cathode element of the crt. The phasing relationships of the isolation transformer T100 alternately forward biases transistors Q100 and Q102, producing a rectified voltage that is filtered by C102. By using a dc heater voltage, power-supply-induced modulation of the crt beam is reduced.

Anode Multiplier

The Anode Multiplier U120 is a conventional X10 voltage multiplier hybrid used to produce the +10 kV accelerating potential for the crt.

CRT

The CRT circuit consists primarily of the cathode ray tube. It presents a visual representation to the user of the events currently being measured (with scale factors), as well as those previously acquired. The only other circuitry shown on this schematic block consists of resistive, level-setting dividers used to set up several operating characteristics of the crt.

Calibrator

The Calibrator circuit is an free-running, operational-amplifier multivibrator. It generates a 0.3 volt peak-to-peak, square-wave output signal to the CAL OUT connector on the instrument's side panel. The approximately 1 kHz CAL OUT signal may be used to compensate the oscilloscope probes to the vertical input to which they are connected.

The output of operational amplifier U980 will go either HI or LO, depending on the relative voltage levels at its inputs. When the output is switched HI, the noninverting input at pin 3 becomes referenced at approximately +3.1 volts due to the positive feedback through R984. Capacitor C982 charges positive through R982 until this level is reached.

At this time, the output switches LO and the hysteresis caused by R984 sets the noninverting input of U980 at about +1.9 volts. The inverting input charges negative until this level is reached and the output returns HI. This cycle continuously repeats itself to, produce the Calibrator waveform.

The resistive divider and potentiometer at the output of U980 allows the amplitude of the calibrator signal at the CAL OUT jack to be precisely set at the time of instrument calibration.

LOW-VOLTAGE POWER SUPPLY ◈19◈

The low voltages required by the 336 are produced by a high-efficiency, switching power supply (diagram 19). This type of supply directly rectifies and stores charge from the ac line supply; then this stored charge is switched through a special transformer at a high rate, producing several ac voltages at the transformer's outputs. These ac voltages are rectified and stored as dc levels that are then regulated down to the final supply voltages.

Line Rectifier-Filter

Ac source voltages of either 115 V or 230 V may provide the primary power for the instrument, depending on the position of the internal LINE VOLTAGE SELECT jumper, P50. Power switch S30 applies the selected line voltage to rectifier bridge CR50-CR53.

With the LINE VOLTAGE SELECT jumper in the 115 V position, the rectifier and storage capacitors operate as a full-wave voltage doubler. When operating in this configuration, each capacitor is charged on opposite half cycles of the ac input through diodes CR53 and CR52. The voltage across capacitors C50 and C52 (in series) will approximate the peak-to-peak value of the source voltage.

For 230 V operation, jumper P50 connects the rectifier diodes as a conventional bridge rectifier. Both capacitors (in series) charge on both half cycles of the ac input, and the voltage across both caps in series will approximate the peak value of the source voltage. For either configuration, the dc voltage supplied to the Power Switching stage is the same (320 volts).

Resistor R35 limits the surge current when the power supply is first turned on. Varistors RV40 and RV42 are surge protectors. If excessive source voltage is applied to the instrument, the varistors conduct and the extra current flow quickly exceeds the rating of fuse F10. The fuse will open, protecting the power supply from excessive input voltages. For 115 volt operation, only RV40 is placed across the line input; for 230 volt operation, RV40 and RV42 are placed in series across the line input.

Common-Mode inductor L12, resistor R12, and capacitors C12, C13, and C35 form a line-filter circuit to minimize transfer of power-line interference into the instrument and power-supply switching transients onto the power line.

Starter

The Starter circuit consists of a free-running unijunction transistor (UJT) oscillator Q102 that provides the initial base-drive current to switching transistor Q140. When instrument power is applied, capacitor C94 begins charging positive through R90. When the charging level at the emitter of UJT Q102 reaches the device's trigger level, conduction from base 2 (B2) to base 1 (B1) occurs (as well as from emitter to base 1) and provides a current pulse to the base of switching transistor Q140. Transistor Q140 turns on and discharges any remaining charge stored on C94 through diode CR100.

Normally, when Q140 turns on, currents start flowing in transformers T130 and T190, sourcing in-phase drive currents to the base of Q140 (via R134, CR135, and R135). This keeps it saturated for a short period of time, as explained in the Inverter description.

If normal Inverter operation doesn't start, these extra base-drive currents to Q140 will not be present, allowing C94 to immediately begin recharging. Another pulse to the base of Q140 will be generated in another attempt to start the Inverter operation. This cycling will continue until normal Inverter operation starts, at which time the charge-discharge cycle is modified slightly, as explained in the Inverter description.

Inverter

The Inverter stage provides the power switching necessary to convert the rectified ac line current to an approximately 20 kHz sine wave for application to the output transformer. It consists of a switching transistor used to open and close a current path in the resonant primary circuit of the output transformer.

Initially, the Starter circuit generates a current pulse to the base of switching transistor Q140, as described earlier. This pulse will turn Q140 on, and current begins to flow from the positive supply $+V_P$ to (virtual) ground P through the resonant primary circuit of T190 and that of T130. The increasing current flowing in the primary of T130 induces a current in one of its secondary windings that is applied to the base of Q140 through R134. This current is in phase with that originally applied to Q140 by the Starter circuit and holds Q140 on after the short start pulse ends.

With Q140 on, current continues to flow in the resonant primary circuit of T190 and C190 (from $+V_P$ to virtual ground) until the current reaches its maximum value. At this point, flux in the transformers begins to decay (reverses) and the current induced in the secondary to the base of Q140 reverses, turning Q140 off. This closes the primary current path and the reversed flux in the transformers builds rapidly. Currents induced in the transformers due to the flux reversal and decay are returned to the positive supply through diode CR130. Diode CR146 and capacitor C142 provide a return path around the primary of T130.

When this second flux reversal begins to decay, current in the secondary to the base of Q140 reverses again and turns it back on, starting the cycle over again. This cycle is continuously repeated as long as the instrument is running. The resulting ac waveform applied to the primary of T190 generates turns-related voltages at the secondary outputs of the transformer, which are rectified and regulated to produce the low-voltage power supply voltages.

Pulse Width Modulator

The Pulse Width Modulator detects the levels of the regulated power supplies and varies the "on" time of switching transistor Q140 in order to vary the power transferred from the Inverter to the regulated power supplies.

Since the Pulse Width modulator must be operational before any of the secondary supplies will come up, an independent power source must be established. Power for this fundamental circuit is provided from secondary windings of T190 and T130 by diodes CR156 and CR158 and filter capacitor C156.

Once this supply is established, operation of the Pulse Width Modulator begins. When transistor Q140 turns on, a negative-going signal is generated at output P3 of transformer T190. When this level reaches approximately −5.7 volts (indicating that the cycle is under way), transistor Q156 will turn off, allowing capacitor C152 to charge positive through resistor R152. Charge rate is set by the amount of current sinked through the output transistor of U160 and is dependent on the output of the error amplifier, made up of transistors Q160, Q162 and the associated components.

The error amplifier is an emitter-coupled transistor pair with one of the bases referenced at +2.5 volts. The other base senses the levels of the +5 volt and +10 volt unregulated supplies via resistive sense network R162, R168, R164, and R167. Due to the relative values of R162 and R168, the $+5\ V_D$ supply voltage is the primary sense control for the error amplifier. Potentiometer R167 in this sensing network allows the output level of the +5 volt digital ($+5\ V_D$ supply (and, due to turns ratios, the other unregulated supply voltages) to be set at the time of calibration.

Depending on the output voltages of the $+5\ V_D$ and +10 V supplies, the base of Q162 will be biased at some level relative to the base of Q160. If the base of Q162 goes more positive than that of Q160 (due to output voltages being too high), the current through the light-emitting diode of U160 will be reduced. This lowers the bias level on the output transistor of U160 and the current through it is reduced.

Reducing the current through U160 allows C152 to charge faster and turns the switching transistor Q140 off sooner than it would otherwise. Turning Q140 off earlier reduces the charge transferred to the secondary windings on that cycle and reduces the secondary output voltages. These reduced voltages are applied to the bias divider of Q162 and lower it back towards the +2.5 volt reference at the base of Q160.The opposite occurs if the outputs tend too low, and pulse width will increase.

+2.5 Volt Reference

Each of the power supply regulators controls its respective output by comparing its output voltage to a known reference level. In order to maintain stable supply voltages, the reference itself must be highly stable. Three-terminal reference IC U250 provides this reference level.

Unregulated Supplies

The unregulated dc supplies are derived from the various secondary windings by rectifying the output voltages and storing charge on storage capacitors. The resulting unregulated voltages are used at various points in the instrument and are the power source for the various regulated supplies.

In addition, several ac voltages used in the High Voltage and CRT circuits are generated by secondary windings of transformer T190.

−8 V Regulator

The −8 volt regulator consists of diode CR189, capacitor C189, resistor R189, and zener diode VR189. The diode rectifies the voltage from the 10 volt secondary winding and stores charge on C189. Resistor R189 and zener diode VR189 form a zener regulating circuit that holds the output voltage at −8.2 volts.

+8 V Regulator

The +8 volt regulator is composed of U200, Q200, and their associated components. Initially, as instrument power is applied, the voltage at pin 5 of U200 from voltage divider R204-R206 is below the +2.5 volt reference applied to U200 pin 6. This causes the output at pin 7 of U200 to go low, turning series-pass transistor Q200 on. With Q200 on, the voltage at the +8 V output will rise (as various load capacitances are charged up) until the output voltage reaches +8 volts.

With the output at +8 volts, the voltage at pin 5 of U200 will equal that at U200 pin 6. This is the balanced condition, and any deviation from this output level will cause a change in base drive to series-pass transistor Q200.

If the output voltage tends too high, the output of U200 will also go high, reducing base drive to Q200. Reduced base drive tends to turn Q200 off, and the output voltage will drop until the +8 volt level is reattained.

If the output level tends low, the opposite circuit action occurs to turn Q200 on harder. This active regulation holds the output level constant under varying load conditions. Capacitor C206 allows the regulator to respond to high- and mid-frequency load variations while holding the longer term (dc) characteristics of the output constant.

+5 V Regulator

Operation of the +5 V Regulator is similar to that just described for the +8 V Regulator. The supply's output voltage is sensed by operational amplifier U220B and is used to control base drive to series-pass transistor Q220.

However, instead of using the operational amplifier's output to directly control the base drive of the series-pass transistor (as in the +8 V Regulator), the positive supply current drawn by both of the operational amplifiers within U220 is used for quiescent bias current for Q220. Then, depending on the output level sensed, additional current will be sinked from the operational amplifier's positive-supply input to ground via the operational amplifier's output transistor, resistor R224 and diode CR224. This additional current turns series-pass transistor Q220 on, and the output level rises until it approaches the proper voltage.

As the output nears its regulation level, the additional current drawn through R224 and CR224 by the operational amplifier's output will be reduced, turning Q220 down. Due to the high gain of the operational amplifier, the output level at which the transistor begins to turn off will be very close to the final regulated level. The output level will continue to rise until an equilibrium is reached where the total positive supply current holds the output level in regulation. Changes in the output voltage will cause the operational amplifier to turn Q220 up or down from this equilibrium state to keep the output voltage in regulation.

−5 V Regulator

Operation of the −5 V Regulator is nearly identical to that just described for the +5 V Regulator. The major difference is that the negative supply current is used as the control for the series-pass transistor.

Line Trigger

The Line Trigger stage uses the "floating" power-line signal to modulate the frequency of unijunction transistor oscillator Q124 by varying the charging rate of C122. The output of this oscillator drives the light-emitting diode within U120 and produces a corresponding frequency-modulated pulse train at the collector output of U120. Coupling-capacitor C120 couples the pulse train to the frequency-compensated line-trigger channel switch (diagram 7), where the high-frequency component of the pulse train is rejected while keeping the lower frequency ac component of the waveform (power line frequency).

PERFORMANCE CHECK PROCEDURE

INTRODUCTION

The "Performance Check Procedure" is used to verify the instrument's Performance Requirements as listed in the "Specification" (Section 1) and to determine the need for readjustment. These checks may also be used as an acceptance test or as a preliminary troubleshooting aid.

This procedure does not check every facet of instrument operation; rather it is concerned with those portions of the 336 that are essential to measurement accuracy. Removing the instrument's wrap-around cabinet is not necessary to perform this procedure. All checks are made using the operator-accessible controls and connectors. A complete check of the instrument's operation is performed in conjuction with the "Adjustment Procedure" of Section 5.

TEST EQUIPMENT REQUIRED

The test equipment listed in Table 4-1 is a complete list of the equipment required to accomplish both the "Performance Check Procedure" in this section and the "Adjustment Procedure" in Section 5. Test equipment specifications described in Table 4-1 are the minimum necessary to provide accurate results. Therefore, equipment used must meet or exceed the listed specifications. Detailed operating instructions for test equipment are not given in this procedure. If more operating information is required, refer to the appropriate test equipment instruction manual.

When equipment other than that recommended is used, control settings of the test setup may need to be altered. If the exact item of equipment given as an example in Table 4-1 is not available, check the "Minimum Specification" column to determine if any other available test equipment might suffice to perform the check or adjustment.

PERFORMANCE CHECK INTERVAL

To ensure instrument accuracy, check its performance after every 2000 hours of operation or once each year, if used infrequently.

PREPARATION

Before commencing this procedure, ensure that the Line Voltage Selection indicator on the rear panel indicates that the internal Nominal Line Selector is set to the correct ac-power-source voltage (see "Preparation for Use" in Section 2).

This procedure is structured in subsections to permit checking individual sections of the instrument whenever a complete Performance Check is not required. At the beginning of each subsection there is a list showing only the test equipment required to perform the checks of that subsection. Item numbers following the equipment name in parentheses refers to the test equipment item number listed in Table 4-1.

The initial front-panel control settings required to prepare the instrument for performing Step 1 are given at the beginning of each subsection. Each succeeding step within a subsection should then be performed both in the sequence presented and in its entirety to ensure that control settings will be correct for ensuing steps.

Table 4-1
Test Equipment Required

Item and Description	Minimum Specification	Use	Example of Applicable Test Equipment
1. Leveled Sine-Wave Generator	Frequency: 250 kHz to above 70 MHz. Output amplitude: variable from 10 mV to 5 V p-p. Output impedance: 50 Ω. Reference frequency: 50 kHz. Amplitude accuracy: constant within 3% of reference frequency as output frequency changes.	Vertical, horizontal, and triggering checks and Display adjustments and Z-Axis check.	TEKTRONIX SG 503 Leveled Sine-Wave Generator.[a]
2. Calibration Generator	Standard-amplitude signal levels: 5 mV to 50 V. Accuracy : ±3%. High-amplitude signal levels: 1 V to 60 V. Repetition rate: 1 kHz. Fast-rise signal level: 1 V. Repetition rate: 1 MHz. Rise time: 1 ns or less. Flatness: ±5%.	Signal source for gain and and transient response.	TEKTRONIX PG 506 Calibration Generator.[a]
3. Time-Mark Generator	Marker outputs: 10 ns to 0.5 s. Marker accuracy: ±0.1%. Trigger output: 1 ms to 0.1 μs, time-coincident with markers.	Horizontal checks and adjustments. Display adjustment.	TEKTRONIX TG 501 Time-Mark Generator.[a]
4. Function Generator	Range: less than 1 Hz to 1 kHz; sinusoidal output; amplitude variable up to greater than 10 V p-p open circuit with dc offset adjust.	Low-frequency checks.	TEKTRONIX FG 502 Function Generator.[a]
5. Digital Voltmeter (DMM)	Range: 0 to 140 V. Dc voltage accuracy: ±0.15%. 4 1/2 digit display.	Power supply checks and adjustments. Crt grid-bias adjustment.	TEKTRONIX DM 501A Digital Multimeter.[a]
6. Test Oscilloscope with 10X probes	Bandwidth: dc to 10 MHz. Minimum deflection factor: 5 mV/div. Accuracy: ±3%.	General troubleshooting, checking holdoff time.	SONY/TEK 335 or 336 Oscilloscope.
7. GPIB Controller	Control GPIB. Conform to IEEE-488 Codes and Formats.	Check GPIB operation of Option 01.	TEKTRONIX 4050 series.
8. X-Y Plotter		Check X-Y output.	
9. Variable Autotransformer	Capable of supplying 1.5 A at 115 Vac.	Power supply regulation check.	General Radio WBMT3VM Variac Autotransformer.

Table 4-1 (cont.)

Item and Description	Minimum Specification	Use	Example of Applicable Test Equipment
10. Isolation Transformer	Minimum power: 100 W 1:1 turns ratio.	Safety.	Tektronix Part Number 006-5953-00.
11. Coaxial Cable (2 required)	Impedance: 50 Ω. Length: 42 in. Connectors: BNC.	Signal interconnection.	Tektronix Part Number 012-0057-01.
12. Precision Coaxial Cable	Impedance: 50 Ω. Length: 36 in. Connectors: BNC.	Used with PG506 Calibration Generator	Tektronix Part Number 012-0482-00.
13. Termination (2 required)	Impedance: 50 Ω. Connectors: BNC.	Signal termination.	Tektronix Part Number 011-0049-01.
14. 10X Attenuator	Ratio: 10X. Impedance: 50 Ω. Connectors: BNC.	Vertical compensation and triggering checks.	Tektronix Part Number 011-0059-02.
15. 2X Attenuator	Ratio: 2X. Impedance: 50 Ω. Connectors: BNC.	External Triggering checks.	Tektronix Part Number 011-0069-02.
16. Adapter	Connectors: BNC male-to-miniature-probe tip.	Signal interconnection.	Tektronix Part Number 013-0084-02.
17. Alignment Tool	Length: 1-in shaft. Bit size: 3/32 in. Low capacitance; insulated.	Adjust variable capacitors and resistors.	Tektronix Part Number 003-0675-00
18. 10X Standard Accessory Probe (supplied with instrument)		Vertical input capacitance adjustment. VOLTS/DIV compensation.	TEKTRONIX P6148.
19. TV Signal Generator	Provide Composite TV Video and Line Sync Signals.	Check TV Trigger circuit.	TEKTRONIX 067-0601-00. Calibration Fixture with 067-5002-00 (525/60) and 067-5010-00 (1201/60) plug-ins.
20. Dual-Input Coupler	Connectors BNC female-to-dual-BNC male.	Signal interconnection.	Tektronix Part Number 067-0525-01.
21. Shorting Plug	Two-terminal square-pin connector with shorting strap.	Calibrator adjustment.	Tektronix Part Number 131-0993-00.

[a]Requires a TM500-series power module.

INDEX TO PERFORMANCE CHECK PROCEDURE

Vertical

Triggers

Horizontal

External Z-Axis, Calibrator, and CHART OUT

VERTICAL

Equipment Required (see Table 4-1)

Leveled Sine-Wave Generator (Item 1)
Calibration Generator (Item 2)
Function Generator (Item 4)
50 Ω BNC Coaxial Cable (Item 11)
50 Ω Precision BNC Cable (Item 12)
50 Ω Termination (Item 13)
Adapter BNC-male-to-miniature probe tip (Item 16)
Dual-input Coupler (Item 20)

NOTE

If starting the Performance Check Procedure at this point, prior to applying power to the 336, verify that the Nominal Voltage Selector is set to the correct power source voltage. Connect the 336 to an appropriate power source and apply power to the instrument and test equipment. Make the initial 336 control settings as soon as the Power-on diagnostics routine has completed, and allow a 20-minute warmup period before commencing the procedure to obtain the maximum accuracy.

INITIAL CONTROL SETTINGS

Control settings not listed do not affect the initial procedure and will be set when needed.

Set:	
INTENSITY	Visible display
FOCUS	Best defined display
VERT MODE	DUAL TRACE
VOLTS/DIV (both)	5 mV
VOLTS/DIV VAR (both)	CAL (in detent)
AC-GND-DC (both)	DC
CH 2 INVERT	Noninverted (no down arrow displayed)
Vertical POSITION (both)	Midrange
DISPLAY MODE	
NON STORE	ON (LED illuminated)
STORE	OFF
VIEW	OFF
Horizontal Display Mode	A (SEC/DIV knob in)
Horizontal POSITION	Midrange
SEC/DIV	0.5 ms
VAR SWP/HOLDOFF	CAL/NORM (in detent)
TRIGGER	
MODE	AUTO
SOURCE	CH 2
COUPLING	AC
A LEVEL	For a stable display (with signal applied)
A SLOPE	+ (plus)
Main MENU Selections	
READOUT	ON
TIMEOUT	SLOW
ACQ WINDOW	POST TRIG

1. Check Channel 1 and Channel 2 NON STORE Deflection Factor Accuracy

a. Connect a 20 mV, standard-amplitude square-wave signal from the calibration generator to the CH 2 input connector via a 50 Ω precision BNC cable.

b. Vertically center the standard-amplitude square-wave display.

c. CHECK—That the display amplitude is 4 divisions within 3% (3.88 to 4.12 divisions).

d. CHECK—Change the calibration generator setting and the VOLTS/DIV setting on the channel being checked as shown in Table 4-2 and check that the deflection accuracy is within 3% for all VOLTS/DIV switch settings listed.

e. CHECK—Display amplitude decreases from 5 divisions to 2 divisions or less when the VAR VOLTS/DIV control is rotated fully counterclockwise.

f. Set the VERT MODE and TRIGGER SOURCE to CH 1 and set the calibration generator output for 20 mV.

g. Move the test signal from the CH 2 input to the CH 1 input and vertically center the display.

h. CHECK—Repeat parts c and d for all CH 1 VOLTS/DIV switch settings.

i. CHECK—Repeat part e for CH 1 VAR VOLTS/DIV control.

j. Return the calibration generator output amplitude to 20 mV.

Table 4-2
Vertical Deflection Accuracy

VOLTS/DIV Setting	Calibration Generator Amplitude	Divisions of Deflection
10 mV	50 mV	4.85 to 5.15
20 mV	0.1 V	4.85 to 5.15
50 mV	0.2 V	3.88 to 4.12
0.1 V	0.5 V	4.85 to 5.15
0.2 V	1 V	4.85 to 5.15
0.5 V	2 V	3.88 to 4.12
1 V	5 V	4.85 to 5.15
2 V	10 V	4.85 to 5.15
5 V	20 V	3.88 to 4.12
10 V	50 V	4.85 to 5.12

2. Check Storage Deflection Accuracy

a. Set:

CH 1 VOLTS/DIV	5 mV
VAR VOLTS/DIV (both)	CAL (in detent)
DISPLAY MODE	STORE
Main MENU Selections	
CURSORS	ON
TRIGGER	
A LEVEL	Adjust for a stable, triggered display

b. Use the DLY TIME/CURSOR push buttons and MENU 1 button (CURSOR SEL) to position one cursor dot on the top of the standard-amplitude square wave and the other on the bottom of the waveform.

c. CHECK—Cursor ΔV readout is 20 mV ± 0.4 mV (changes in the readout should be centered around 20 mV).

d. CHECK—Store display amplitude is 4 divisions ± 0.12 division (3.88 to 4.12 divisions).

e. CHECK—Change the VOLTS/DIV and calibration generator settings to each of the settings given in Table 4-3 and check the storage deflection accuracy and voltage readouts for each VOLTS/DIV setting given.

f. Set:

VERT MODE	CH 2
CH 2 VOLTS/DIV	5 mV
TRIGGER SOURCE	CH 2

g. Set the calibration generator output amplitude to 20 mV and move the test signal from the CH 1 input connector to the CH 2 input connector.

h. CHECK—Repeat parts c, d, and e for all CH 2 VOLTS/DIV switch settings.

i. Disconnect the test equipment from the 336.

Table 4-3
STORAGE DEFLECTION ACCURACY

VOLTS/DIV Setting	Generator Setting	Waveform Deflection Limits (divisions)	Voltage Readout Limits
10 mV	50 mV	4.85 to 5.15	48.1 mV to 51.9 mV
20 mV	0.1 V	4.85 to 5.15	96.2 mV to 103.8 mV
50 mV	0.2 V	3.88 to 4.12	192 mV to 208 mV
0.1 V	0.5 V	4.85 to 5.15	481 mV to 519 mV
0.2 V	1 V	4.85 to 5.15	962 mV to 1.038 mV
0.5 V	2 V	3.88 to 4.12	1.92 V to 2.08 V
1 V	5 V	4.85 to 5.15	4.81 V to 5.19 V
2 V	10 V	4.85 to 5.15	9.62 V to 10.38 V
5 V	20 V	3.88 to 4.12	19.2 V to 20.8 V
10 V	50 V	4.85 to 5.15	48.1 V to 51.9 V

3. Check Bandwidth

a. Set:

CH 2 VOLTS/DIV	5 mV
SEC/DIV	10 μs
DISPLAY MODE	NON STORE
CURSORS	OFF (press MENU button 2)

b. Connect the leveled sine-wave generator output to the CH 2 input connector via a 50 Ω precision BNC cable and a 50 Ω termination.

c. Set the generator frequency for 50 kHz and set the output amplitude for a 6-division vertical display. Use the Vertical POSITION control to certically center the display.

d. Increase the sine-wave generator frequency to 50 MHz.

e. CHECK-NON STORE display amplitude is 4.2 divisions or more peak-to-peak.

f. Set the DISPLAY MODE to STORE and set the A SEC/DIV setting to 0.1 μs.

g. CHECK—STORE display amplitude is 4.2 divisions or more peak-to-peak.

h. Set the DISPLAY MODE to NON STORE and set the A SEC/DIV setting to 10 μs.

i. Repeat parts c through h for each VOLTS/DIV setting up to 1 V.

NOTE

The sine-wave generator output amplitude is limited to 5 V peak-to-peak. Therefore, at the 1 V setting, set the reference signal display amplitude to 5 divisions and check for a display amplitude of at least 3.5 divisions at 50 MHz.

j. Set:

VERT MODE	CH 1
CH 1 VOLTS/DIV	5 mV
DISPLAY MODE	NON STORE
TRIGGER SOURCE	CH 1

k. Move the test signal from the CH 2 input connector to the CH 1 input connector.

l. Repeat parts c through i for Channel 1.

m. Set:

VERT MODE	TRIG VIEW

DISPLAY MODE	NON STORE
A SEC/DIV	10 μs
TRIGGER	
SOURCE	EXT
MODE	NORM

n. Set the sine-wave generator frequency to 50 kHz and move the test signal from the CH 1 input connector to the EXT TRIG IN connector.

o. Adjust the A TRIG LEVEL control for a stable display near the center of the graticule area.

p. Set the generator output amplitude for a 5-division vertical display. Adjust the A TRIG LEVEL control as necessary to center the display.

q. Increase the generator output frequency to 35 MHz.

r. CHECK—TRIG VIEW display amplitude is 3.5 divisions or more peak-to-peak.

s. Set the TRIG SOURCE to EXT/10 and reestablish a 5-division, 50 kHz reference signal display.

t. Repeat parts q and r.

u. Disconnect the coaxial cable from the EXT TRIG IN connector.

v. Set:

VERT MODE	ADD
VOLTS/DIV (both)	5 mV
TRIGGER	
SOURCE	CH 1
MODE	AUTO

w. Connect the leveled sine-wave generator output to the CH 1 and CH 2 input connectors via a 50 Ω coaxial cable, a 50 Ω termination, and a dual-input coupler.

x. Set the generator output frequency to 50 kHz and adjust the output amplitude to obtain a 6-division ADD display. Use either the CH 1 or the CH 2 Vertical POSITION control to center the display vertically.

y. Increase the generator output frequency to 30 MHz.

z. CHECK—ADD display amplitude is 4.2 divisions or more peak-to-peak.

aa. Remove the dual-input coupler from the test setup and reconnect the leveled sine-wave generator output to the CH 1 input connector via the 50 Ω coaxial cable and 50 Ω termination.

ab. Set:

VERT MODE	CH 1
A SEC/DIV	2 ms
DISPLAY MODE	STORE
Main MENU Selection	
STORAGE Mode	ENVELOPE

ac. With the ENVELOPE Menu displayed, use the DECR button (MENU 2) to decrease the number of acquisitions to 1 TIMES (it not already there).

ad. Set the sine-wave generator output for a 50 kHz reference signal, 6-divisions in amplitude.

ae. Increase the generator frequency to 10 MHz.

af. CHECK—ENVELOPE display amplitude is 4.2 divisions or more peak-to-peak.

ag. Disconnect the test equipment from the 336.

4. Check AC COUPLING Lower −3 dB Bandpass

a. Set:

VERT MODE	DUAL TRACE
VOLTS/DIV (both)	50 mV (with 10X probe attached)
SEC/DIV	0.5 s ROLL
CH 1 AC-GND-DC	AC
CH 2 AC-GND-DC	DC

b. Connect one of the accessory 10X probes to the CH 2 input connector and remove the grasping probe tip.

c. Connect the output of the function generator to the probe tip via a 50 Ω termination and a BNC male-to-miniature-probe-tip adapter.

d. Set the generator output for a 1 Hz sine wave and adjust the output amplitude control for a 5-division display amplitude.

e. Switch the CH 2 AC-GND-DC switch to AC.

f. CHECK—ROLL display amplitude is 3.5 divisions or more peak-to peak.

g. Move the probe from the CH 2 input connector to the CH 1 input connector.

h. CHECK—ROLL display amplitude is 3.5 divisions or more peak-to-peak.

i. Disconnect the test setup.

5. Check AVERAGE Mode

a. Set:

VERT MODE	CH 1
A SEC/DIV	1 ms
Main MENU Selections	
STORE MODE	AVERAGE

b. With the AVERAGE Menu displayed, press MENU button 2 (DECR) to decrement the number of averages to 8 TIMES (if not already at that setting).

c. CHECK—Number at lower right corner counts down to 1, then switches to AVG at the end of the count.

d. Recall the AVERAGE Menu using the LAST button (if it has timed out).

e. CHECK—That the number of times increments to 16, 32, 64, 128, and 256 as the MENU 1 button is pressed to increase the setting.

f. Decrement the number of averages to 8 TIMES and set the STORE MODE back to NORMAL.

6. Check PROCESS Operation

a. Set:

CH 1 VOLTS/DIV (both)	5 mV
AC-GND-DC (both)	DC
Main MENU Selection	
STORAGE	PROCESS

b. Connect a 10 mV standard-amplitude square-wave signal from the output of the calibration generator to the CH 1 and CH 2 input connectors via a 50 Ω coaxial cable and a dual-input coupler.

c. Adjust the CH 1 and CH 2 Vertical POSITION controls to place the CH 1 and CH 2 displays at convenient locations with the graticule area.

d. Switch Channel 1 and Channel 2 AC-GND-DC switches to GND to acquire a ground reference for calculations. (Do not reposition the Vertical POSITION controls after acquiring the ground reference. If repositioning occurs, reacquire the ground reference.)

e. Set both AC-GND-DC switches back to DC.

f. Select WFM (waveform) processing by pressing MENU button 1, then press MENU button 1 again to select CH 1 + CH 2.

g. CHECK—Added waveform amplitude is 4 divisions ±0.24 division (3.76 to 4.24 divisions)

h. Press MENU button 2 to select CH 1 - CH 2.

i. CHECK—Subtracted waveform amplitude is zero division ±0.24 division (disregarding transitions spikes).

j. Press MENU button 3 to select CH 1 x CH 2.

k. CHECK—Multiplied waveform amplitude is 4 divisions ±0.3 division (3.7 to 4.3 divisions).

l. Press the MENU LAST button to discontinue WFM processing and disconnect the test equipment from the instrument.

m. Connect the output of a leveled sine-wave generator to the CH 1 input connector via a 50 Ω precision coaxial cable and a 50 Ω termination.

n. Set:

VERT MODE	CH 1
SEC/DIV	5 μs

o. Set the generator frequency for 250 kHz and adjust the output amplitude for a display of 6 divisions. Use the CH 1 Vertical POSITION control to center the display as necessary.

p. With the PROCESS Menu displayed, press MENU button 2 to select PARAMETERS processing, then press MENU button 1 to select RMS.

q. Set CH 1 AC-GND-DC switch to GND to acquire a ground reference (readout goes to zero), then set it back to DC.

NOTE

Do not vertically reposition the channel display after switching the input coupling back to DC. If this should occur, reacquire a ground reference before checking the RMS readout of the signal display.

r. CHECK—RMS readout is 10.6 mV ±0.6 mV (10.1 mV to 11.2 mV).

s. Press MENU button 2 to select P-P.

t. CHECK—P-P readout is 30 mV ±1 mV (29 mV to 31 mV)

u. Press MENU button 3 to select MEAN.

v. CHECK—MEAN readout is 0.0 mV ±0.6 mV (−0.6 mV to 0.6 mV).

w. Disconnect the test equipment from the 336.

7. Check TRIG VIEW Deflection Factor Accuracy

a. Set:

VERT MODE	TRIG VIEW
DISPLAY MODE	NON STORE
SEC/DIV	0.5 ms
TRIGGER	
MODE	NORM
COUPLING	AC
SOURCE	EXT

b. Connect a 0.5 V standard-amplitude square-wave signal from the calibration generator to the EXT TRIG IN connector via a 50 Ω precision BNC cable.

c. Use the A TRIG LEVEL control to vertically center the TRIG VIEW display on the + (plus) SLOPE.

d. CHECK—TRIG VIEW display amplitude is 5 divisions ±0.25 division (4.75 to 5.25 divisions).

e. Set the TRIGGER SOURCE to EXT/10 and switch the calibration generator output to 5 V.

f. CHECK—Repeats parts c and d for the EXT/10 TRIG VIEW display.

g. Disconnect the test equipment from the 336.

TRIGGERS

Equipment Required (see Table 4-1)

Leveled Sine-Wave Generator (Item 1)
Calibration Generator (Item 20
Function Generator (Item 4)
50 Ω BNC Coaxial Cable (Item 11)
50 Ω BNC Termination (Item 13)
10X Attenuator (Item 14)
2X Attenuator (Item 15)
TV Signal Generator (Item 19)
Dual-input Coupler (Item 20)

NOTE

If starting the Performance Check Procedure at this point, prior to applying power to the 336, verify that the Nominal Voltage Selector is set to the correct power source voltage. Connect the 336 to an appropriate power source and apply power to the test equipment and 336. Make the initial 336 control settings as soon as the Power-on diagnostics routine has completed, and allow a 20-minute warmup period before commencing the adjustments and checks for maximum accuracy.

INITIAL CONTROL SETTINGS.

Control settings not listed do not affect the initial procedure and will be set when necessary.

Set:	
INTENSITY	Visible display
FOCUS	Best defined display
VERT MODE	DUAL TRACE
VOLTS/DIV (both)	0.5 V
VOLTS/DIV VAR (both)	CAL (in detent)
AC-GND-DC (both)	DC
CH 2 INVERT	Noninverted (no down arrow displayed with CH 2 VERT MODE)
Vertical POSITION (both)	Midrange
DISPLAY MODE	
NON STORE	ON (LED illuminated)
STORE	OFF
VIEW	OFF
Horizontal Display Mode	A (knob in)
Horizontal POSITION	Midrange
A SEC/DIV	10 ms
X10 MAG	OFF (indicator unlighted)
VAR SWP/HOLDOFF	CAL/NORM (in detent)
TRIGGER	
MODE	AUTO
SOURCE	CH 1
COUPLING	AC
A LEVEL	For a stable display (with signal applied)
A SLOPE	+ (plus)
B MODE	Triggerable after delay
B SLOPE	+ (plus)
B LEVEL	Center of the + SLOPE
Main MENU Selections	
READOUT	ON
TIME OUT	SLOW
CURSORS	OFF
HORIZ VAR	HOLDOFF
TRACE SEP	2.0 DIV

1. Check A and B Internal Trigger Sensitivity

a. Connect the function generator output to CH 1 and CH 2 input connectors via a 50 Ω coaxial cable, a 50 Ω termination, and a dual-input coupler.

b. Set the generator output for a sine-wave signal of 30 Hz and set the output amplitude for a 3-division display amplitude.

c. Set both VOLTS/DIV settings to 5 V to obtain a signal amplitude of 0.3 division on both channels.

d. CHECK—A and B Trigger Sensitivity.

1. Set the TRIGGER MODE to NORM.

2. Verify that a stable A Sweep display can be obtained using the A TRIG LEVEL control on both + and − SLOPE.

3. Set the Trigger SOURCE to CH 2 and repeat subpart 2.

4. Set the Horizontal Display Mode to ALT (pull SEC/DIV knob).

5. Verify that a stable B Sweep display (also an intensified zone appears on the A trace) can be obtained using the B TRIG LEVEL control on both + and − SLOPE. (Adjust the A TRIG LEVEL control as necessary to maintain a stable A Sweep display.)

6. Set the Trigger SOURCE to CH 1 and repeat subpart 5.

7. Set:

Horizontal Display Mode	A (push SEC/DIV knob in)

8. For 50 kHz, 10 MHz, and 50 MHz triggering, set the TRIGGER COUPLING to DC and repeat subparts 2 through 7.

e. Set the function generator for an output frequency of 10 Hz and set the TRIGGER COUPLING to DC.

f. CHECK—Repeat part d, subparts 2 through 6.

g. Set:

A SEC/DIV	10 μs
VOLTS/DIV (both)	0.5 V
Horizontal Display Mode	A (push SEC/DIV knob in)
TRIGGER	
MODE	AUTO
COUPLING	AC
SOURCE	CH 1

h. Disconnect the coaxial cable from the function generator and connect it to the leveled sine-wave generator output.

i. Set the sine-wave generator frequency to 50 kHz and adjust the output amplitude for signal displays 3 divisions in amplitude.

j. Set both VOLTS/DIV settings to 5 V.

k. CHECK—Repeat part d.

l. Increase the generator frequency to 10 MHz, set the A SEC/DIV setting to 0.1 μs, and switch TRIGGER COUPLING to AC.

m. CHECK—Repeat part d, subparts 2 through 8.

n. Set

VOLTS/DIV (both)	0.5V
TRIGGER	
COUPLING	AC
MODE	AUTO

o. Increase the generator frequency to 50 MHz and set the output amplitude for signal displays 3 divisions in amplitude.

p. Set both VOLTS/DIV settings to 1 V.

q. CHECK—Repeat part d.

2. Check HF REJ and LF REJ COUPLING

a. Set:

TRIGGER	
COUPLING	HF REJ
MODE	NORM

b. CHECK—A stable A Sweep display cannot be obtained at any A TRIG LEVEL setting on either + or − SLOPE.

c. Set:

VOLTS/DIV (both)	0.5 V
TRIGGER	
COUPLING	LF REJ

d. Set the leveled sine-wave generator output for 3-division display amplitudes.

e. Set the VOLTS/DIV settings to 1V.

f. CHECK—A stable A Sweep display can be obtained using the A TRIG LEVEL control on both + and − SLOPE.

g. Set the Trigger SOURCE to CH 2 and repeat part f.

h. Set the VOLTS/DIV settings to 0.5 V.

i. Set the sine-wave generator output for a 5-division display at 10 MHz.

j. Set the VOLTS/DIV settings to 5 V and Trigger SOURCE to CH 1.

k. CHECK—Repeat parts f and g.

l. Set the sine-wave generator to 50 kHz.

m. Set the A SEC/DIV setting to 10 μs and Trigger SOURCE to CH 1.

n. CHECK—Repeat parts f and g.

m. Set the A Trigger COUPLING to HF REJ and Trigger SOURCE to CH 1

n. CHECK—Repeat part f and g.

o. Set:

VOLTS/DIV (both)	0.5 V
A SEC/DIV	20 ms

p. Disconnect the coaxial cable from the leveled sine-wave generator output and connect it to the function generator output.

q. Set the function generator output for a sine-wave signal of 30 Hz and and adjust the amplitude control for 5-division displays.

r. Set the VOLTS/DIV settings to 5 V and Trigger SOURCE to CH 1.

s. CHECK—Repeat parts f and g.

t. Set the Trigger COUPLING to LF REJ.

u. CHECK—Repeat part b.

v. Disconnect the test equipment from the 336.

3. Check EXT and EXT/10 Trigger Sensitivity

a. Set:

VERT MODE	CH 2
CH 2 VOLTS/DIV	10 mV
TRIGGER	
MODE	AUTO
COUPLING	AC
SOURCE	EXT

b. Connect the function generator output to the CH 2 and EXT TRIG IN connectors via a 50 Ω coaxial cable, a 10X attenuator, a 2X attenuator, a 50 Ω termination, and a dual-input coupler.

c. Set the function generator for a 7-division display amplitude (70 mV peak-to-peak), then set the Trigger MODE to NORM.

d. CHECK—A stable A Sweep display can be obtained using the A TRIG LEVEL control on both + and − SLOPE with both AC and DC Trigger COUPLING.

e. Set:

CH 2 VOLTS/DIV	20 mV
TRIGGER	
COUPLING	HF REJ

f. Remove the 2X attenuator from the test setup.

g. CHECK—A stable A Sweep Display can be obtained using the A TRIG LEVEL control on both + and − SLOPE.

h. Set the Trigger COUPLING to LF REJ

i. CHECK—A stable A Sweep Display cannot be obtained using the A TRIG LEVEL control on either + or − SLOPE.

j. Set:

TRIGGER	
SOURCE	EXT/10
COUPLING	HF REJ
CH 2 VOLTS/DIV	0.2 V

k. Remove the 10X attenuator from the test setup.

l. CHECK—Repeat part g.

m. Add the 2X attenuator back to the test setup between the coaxial cable and the 50 Ω termination.

n. CHECK—Repeat part d.

o. Move the coaxial cable from the function generator output connector to the leveled sine-wave generator output connector.

p. Set:

CH 2 VOLTS/DIV	0.1 V
A SEC/DIV	10 μs.
TRIGGER	
MODE	AUTO

q. Set the sine-wave generator for a 7-division signal amplitude at 50 kHz, then set the Trigger MODE to NORM.

r. CHECK—Repeat part d.

s. Set:

CH 2 VOLTS/DIV	0.2 V
TRIGGER	
COUPLING	HF REJ

t. Remove the 2X attenuator from the test setup.

u. CHECK—Repeat part g.

v. Set:

TRIGGER	
SOURCE	EXT
CH 2 VOLTS/DIV	20 mV

w. Add the 10X attenuator to the test setup.

x. CHECK—A stable A Sweep display can be obtained using the A TRIG LEVEL control in both + and − SLOPE with both HF REJ and LF REJ COUPLING.

y. Set:

TRIGGER	
COUPLING	HF REJ
A SEC/DIV	0.1 μs

z. Increase the sine-wave generator to 10 MHz.

aa. CHECK—Repeat part i.

ab. Set the Trigger COUPLING to LF REJ.

ac. CHECK—Repeat part g.

ad. Insert the 2X attenuator back into the test setup.

ae. CHECK—Repeat part d.

af. Set:

CH 2 VOLTS/DIV	0.1 V
TRIGGER	
SOURCE	EXT/10

ag. Remove the 10X attenuator from the test setup.

ah. CHECK—Repeat part d.

ai. Set:

TRIGGER	
COUPLING	LF REJ
CH 2 VOLTS/DIV	0.2 V

aj. Remove the 2X attenuator from the test setup.

ak. CHECK—Repeat part g.

al. Increase the sine-wave generator frequency to 50 MHz.

am. Set:

TRIGGER	
SOURCE	EXT
CH 2 VOLTS/DIV	0.1 V

an. Set the sine-wave generator output for a 7-division display amplitude.

ao. CHECK—Repeat part g.

ap. Insert the 2X attenuator back into the test setup.

aq. CHECK—Repeat part d.

ar. Disconnect the test equipment from the 336.

4. Check External Trigger LEVEL Range

a. Set:

CH 2 VOLTS/DIV	1 V
SEC/DIV	1 ms
TRIGGER	
SOURCE	EXT
MODE	AUTO
COUPLING	DC

b. Connect the function generator output to the CH 1 and EXT TRIG IN connectors via a 50 Ω coaxial cable, a 50 Ω termination, and a dual-input coupler. Set the DC Offset control on the function generator for no offset (push control knob in).

c. Set the function generator for a sine-wave signal of 1 kHz and adjust the output amplitude for a 3-division display. Use the CH 1 Vertical POSITION control to center the display vertically.

d. Set the TRIGGER MODE to NORM.

e. CHECK—Display remains triggered as the TRIG LEVEL control is rotated to change the trigger point by ±1 V (start of sweep up 1 division and down 1 division from the center horizontal graticule line).

f. Repeat part e for the − SLOPE side of the TRIG LEVEL control.

g. Set:

Horizontal Display Mode	ALT (pull SEC/DIV knob to out position)
A TRIGGER	
LEVEL	For a stable A Sweep
SLOPE	+ (plus)

h. CHECK—Repeat parts e and f for the B(DLY'D) TRIG LEVEL control.

i. Remove the 50 Ω termination from the test setup.

j. Set:

CH 2 VOLTS/DIV	5 V
Horizontal Display Mode	A (SEC/DIV knob in)
TRIGGER	
SOURCE	EXT/10

k. Rotate the amplitude control on the function generator to full amplitude to obtain a 2-division display (10 V p-p open circuit). Pull the DC Offset knob of the function generator to the out position and rotate it fully counterclockwise (ccw).

l. Use the CH 2 Vertical POSITION control to align the positive peaks of the sine wave with the center horizontal graticule line.

m. CHECK—Display remain triggered as the TRIG LEVEL control is rotated to change the trigger point from −10 V to 0 V (start of trace changes from 2 divisions below center graticule to center graticule).

n. Rotate the DC Offset knob on the function generator to fully clockwise (cw).

o. CHECK—Display remains triggered as the TRIG LEVEL control is rotated to change the trigger point from 0 V to 10 V (start of trace change from center graticule to 2 divisions above center graticule).

p. CHECK—Repeat part o for the − SLOPE.

q. Rotate the DC Offset knob to fully ccw.

r. CHECK—Repeat part m for the – SLOPE.

s. Set:

Horizontal Display Mode	ALT (SEC/DIV knob to the out position)
A TRIGGER	
LEVEL	For a stable A Sweep
SLOPE	+ (plus)

t. CHECK—Repeats parts m through r for the B (DLY'D) TRIG LEVEL control.

u. Disconnect the test equipment from the 336.

5. Check TV Trigger Sensitivity

a. Set:

VERT MODE	CH 1
CH 1 VOLTS/DIV	0.2 V
SEC/DIV	20 μs
Horizontal Display Mode	A (push SEC/DIV knob in)
TRIGGER	
MODE	NORM
SOURCE	CH 1
COUPLING	TV SYNC

b. Connect a source of TV sync-negative composite video to the CH 1 and EXT TRIG IN connectors via a 50 Ω coaxial cable and a dual-input coupler. (Use a 50 Ω termination depending on the generator output impedance.)

c. Adjust the generator output amplitude and use attenuators as necessary to obtain a 1.5-division display amplitude of the horizontal sync pulses.

d. CHECK—That stable TV line triggering can be obtained by adjusting the A TRIG LEVEL control (disregard field pulses moving through the display).

e. Switch the SEC/DIV setting to 5 ms.

f. CHECK—That stable TV field triggering can be obtained by adjusting the A TRIG LEVEL control.

g. Remove attenuators and adjust the generator output amplitude to obtain a 7.5-division display amplitude of the horizontal sync pulses.

h. Set the CH 1 VOLTS/DIV setting to 0.1 V to obtain a 15-division signal amplitude.

i. CHECK—TV field display remains stably triggered.

j. Set the Trigger SOURCE to EXT.

k. CHECK—TV field display remains stably triggered.

l. Set CH 1 VOLTS/DIV setting to 0.2 V.

m. Insert attenuators and adjust the generator output amplitude as necessary to obtain a 2-division display amplitude.

n. Set:

SEC/DIV	0.2 ms
TRIGGER	
A SLOPE	– (minus)
A LEVEL	For a stable display

o. CHECK—Display switches to line sync when the SEC/DIV control is set to 0.1 ms. (Disregard the field pulses running through the display; the VAR HOLDOFF control may be adjusted to reduce or eliminate the vertical-sync field pulses from the display).

p. Set:

A SEC/DIV	0.2 ms
Horizontal Display Mode	ALT (pull SEC/DIV knob out)
B SEC/DIV	20 μs

q. CHECK—A stable B Sweep line pulse display can be obtained by adjusting the B TRIG LEVEL control and that the A Sweep display remains stably triggered on the field pulse.

r. Disconnect the test equipment from the 336.

6. Check Storage Acquisition Window

a. Set:

CH 1 VOLTS/DIV	1 V
A SEC/DIV	0.1 ms

Horizontal Display Mode	A (SEC/DIV knob in)
DISPLAY MODE	STORE
TRIGGER	
MODE	NORM
COUPLING	AC
SOURCE	CH 1
SLOPE	+ (plus)
LEVEL	For a triggered display with signal applied
Main MENU Selections	
ACQ WINDOW	PRE TRIG

b. Connect the function generator output to the CH 1 input connector via a 50 Ω coaxial cable and a 50 Ω termination.

c. Set the function generator for a positive-going pulse output at 100 Hz. Adjust the generator output amplitude control for about a 5-division display. Set the function generator DC Offset control for no offset (press DC Offset control knob in).

d. Use the Horizontal POSITION control to align the start of the trace with the first vertical graticule line.

e. CHECK—Rising edge of the pulse is near the 9th vertical graticule line.

f. Set the ACQ WINDOW to MID TRIG (STORE trace is dimmed while the ACQ WINDOW Menu is displayed).

g. CHECK—Rising edge of the pulse is near the center vertical graticule line.

h. Set the ACQ WINDOW to POST TRIG.

i. CHECK—Rising edge of the pulse is near the 2nd vertical graticule line.

j. Disconnect the coaxial cable from the function generator and connect it to the fast-rise (+) output of the calibration generator.

7. Check Trigger Jitter

a. Set:

CH 1 VOLTS/DIV	0.1 V
TRIGGER	
LEVEL	For a triggered display with a signal applied

b. Set the calibration generator frequency for a 1 kHz signal and adjust the output amplitude control to obtain about a 5-division display amplitude.

c. Use the Horizontal POSITION control to move the rising edge of the waveform to the center vertical graticule line.

d. Press in the X10 MAG button and use the Horizontal POSITION control to align the rising edge of the magnified display with the center vertical graticule line.

e. CHECK—Jitter of the rising edge of the waveform is approximately ±0.1 division horizontally.

f. Set:

DISPLAY MODE	NON STORE
A SEC/DIV	10 ns (with X10 MAG on)

g. Disconnect the coaxial cable from the calibration generator and connect it to the output of the leveled sine-wave generator.

h. Set the sine-wave generator for an output frequency of 50 MHz and adjust the amplitude controls for about a 5-division display amplitude.

i. Use the Horizontal POSITION control to align the rising edge of one of the sine-wave cycles with the center vertical graticule line.

j. CHECK—Jitter on the rising edge of the waveform is ±0.1 division or less.

k. Disconnect the test equipment from the 336.

HORIZONTAL

Equipment Required (see Table 4-1)

Time Mark Generator (Item 3)
Test Oscilloscope (Item 6)
50 Ω BNC Coaxial Cable (Item 11)
50 Ω Precision BNC Coaxial Cable (Item 12)
50 Ω BNC Termination (Item 13)

NOTE

If starting the Performance Check Procedure at this point, prior to applying power to the 336, verify that the Nominal Voltage Selector is set to the correct power source voltage. Connect the 336 to an appropriate power source and apply power to the test equipment and 336. Make the initial 336 control settings as soon as the Power-on diagnostics routine has completed, and allow a 20-minute warmup period before commencing the checks for maximum accuracy.

INITIAL CONTROL SETTINGS

Control settings not listed do not affect the initial procedure and will be set when necessary.

Set:

INTENSITY	Visible display
FOCUS	Best defined display
VERT MODE	CH 1
CH 1 VOLTS/DIV	0.5 V
VOLTS/DIV VAR (both)	CAL (in detent)
AC-GND-DC (both)	DC
Vertical POSITION (both)	Midrange
DISPLAY MODE	NON STORE
Horizontal Display Mode	A (SEC/DIV knob in)
Horizontal POSITION	Midrange
SEC/DIV	0.1 μs
X10 MAG	OFF
VAR SWP/HOLDOFF	CAL/NORM (in detent)
TRIGGER	
MODE	AUTO
SOURCE	CH 1
COUPLING	AC
A LEVEL	For a stable display (with signal applied)
A SLOPE	+ (plus)
B LEVEL	RUNS AFTER DELAY

Main MENU Selections

READOUT	ON
TIME OUT	SLOW
STORE MODE	NORMAL
CURSORS	OFF
HORIZ VAR	SEC/DIV
TRACE SEP	2.0 DIV

1. Check A and B NON STORE Timing Accuracy and Linearity

a. Connect the output of the time-mark generator to the CH 1 input connector via a 50 Ω coaxial cable and a 50 Ω termination.

b. Set the time-mark generator for 0.1 μs time markers.

c. Use the CH 1 Vertical POSITION control to place the tips of the time markers at the center horizontal graticule line (for ease in determining timing from the graticule markings).

d. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line. (Maintain alignment of the 2nd time marker with the 2nd vertical graticule line when checking the timing accuracy at all sweep speeds.)

e. CHECK—Timing accuracy at the 10th graticule line is within 2% (0.2 division) and linearity between any 2 divisions of the center 8 divisions is within 4% (0.08 division)

f. Change the SEC/DIV setting and the time-mark generator setting, one step at a time, to maintain 1 time marker per division, and repeat parts d and e for each sweep speed (up to 0.2 s for the A Sweep and 50 ms for the B Sweep).

NOTE

At the slower sweep speeds, 50 ms per divisions and slower, the TRIGGER MODE should be set to NORM to prevent the AUTO trigger from being generated. This ensures that the sweep is triggered on the applied signal.

g. Set:

CH 1 VOLTS/DIV	0.5 V
SEC/DIV	0.1 μs
Horizontal Display Mode	ALT (SEC/DIV knob out)
Delay Time Position	Minimum delay (press left DLY TIME/CURSOR button until delay time readout stops changing)

h. Set the time-mark generator for 0.1 μs time markers.

i. Use the CH 1 Vertical POSITION control to align the tips of the time markers displayed on the B Sweep with the center horizontal graticule line (for ease in checking timing).

j. CHECK—Repeat parts d, e, and f to check the B Sweep timing accuracy and 2-division linearity.

NOTE

At the slower A SEC/DIV settings, the A Sweep trace may be removed from the display to eliminate the flicker due to sweep switching while making the actual timing accuracy check. Rotate the SEC/DIV knob counterclockwise 1 click to set the A SEC/DIV 1 setting slower than the B SEC/DIV setting that the measurement is to be made on. Then, rotate the SEC/DIV knob back to the correct B SEC/DIC setting and press in the SEC/DIV knob to obtain the B Delayed Sweep only. After making the check, pull the SEC/DIV knob out to set the new sweep speed settings for the next check.

k. Set:

Horizontal Display Mode	A (SEC/DIV knob in)
A SEC/DIV	0.1 μs (with X10 MAG off)

l. Set the time-mark generator for 20 ns time markers and press in the X10 MAG button on the front panel of the 336 (1 time marker per 2 divisions).

m. Use the Horizontal POSITION control to align a displayed time marker with the 2nd vertical graticule line. (The first and last 50 ns of the 10 ns and 20 ns per division sweeps are excluded from the timing accuracy and 2-division linearity checks.)

n. CHECK—Magnified timing accuracy at the 10th vertical graticule line is within 3% (within 0.3 division) and linearity between any 2 divisions of the center 8 divisions is within 5% (within 0.1 division).

o. Change the SEC/DIV setting and the time-mark generator setting, one step at a time, to maintain 1 time marker per division for the remaining sweep speeds, and repeat parts m and n for each sweep speed (up to 20 ms for the A Sweep and 5 ms for the B Sweep).

p. Set the time-mark generator for 20 ns time markers.

q. Set:

SEC/DIV	10 ns (with X10 MAG on)
Horizontal Display Mode	ALT (pull SEC/DIV knob out)
A TRIGGER LEVEL	For a stable display

r. CHECK—Repeat parts m, n, and o for the B Magnified timing accuracy and 2-division linearity checks.

2. Check Storage Timing Accuracy

a. Set:

X10 MAG	Off (button unlighted)
A SEC/DIV	0.2 s (with X10 MAG off)
CH 1 AC-GND-DC	GND
Horizontal Display Mode	A (push SEC/DIV knob in)
TRIGGER MODE	AUTO
DISPLAY MODE	STORE

b. Turn on the CURSORS (press MENU ON/OFF, MENU 1, MENU 4).

c. Use the Horizontal POSITION control to align the start of the trace with the 1st vertical graticule line.

d. Use the DLY TIME/CURSOR buttons to align one cursor dot exactly with 2nd vertical graticule line.

e. Press MENU button 1 to activate the second cursor and position it to the left for a time difference readout of 1.600 s.

f. CHECK—Graticule indication of cursor difference at the 10th graticule line is accurate within 2% (0.2 division).

g. Change the SEC/DIV setting, one step at a time, and repeat part f for each sweep speed. Use the Horizontal POSITION control as necessary to keep the 1st cursor dot aligned with the 2nd vertical graticule line.

h. Set the time-mark generator for 0.1 μs time markers and set the CH 1 AC-GND-DC switch to DC.

i. Set the SEC/DIV setting to 0.1 μs and turn the CURSORS mode off (press MENU button 2).

j. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

k. CHECK—Equivalent-time sampling accuracy is within 3% (0.3 division) at the 10th vertical graticule line.

l. Change the SEC/DIV setting and time-mark generator setting, one step at a time, to maintain 1 time marker per division, and repeat parts j and k for A Sweep speed settings down to 50 μs per division (the end of the equivalent-time sampling region).

3. Check Delay Time Differential Accuracy

a. Set:

CH 1 VOLTS/DIV	1 V
SEC/DIV (both)	0.1 μs
DISPLAY MODE	NON STORE
Horizontal Display Mode	ALT (SEC/DIV knob out)
DLY TIME	Minimum (press left DLY TIME/CURSOR position button until readout stops changing)

b. Set the time-mark generator for 0.1 μs time markers and use the CH 1 vertical POSITION control to position the tips of the time markers displayed by the B Sweep near the center horizontal graticule line.

c. Use the Horizontal POSITION control to align the 2nd time marker on the B Sweep with a reference vertical graticule line. (The 1st time marker may not be completely visible on the B Sweep trace, therefore, at the faster A Sweep speeds the 2nd vertical graticule line makes a convenient reference line.)

d. Press both DLY TIME/CURSOR position buttons at the same time and release to zero the delay time readout. Use the Horizontal POSITION control to realign the time marker with the reference graticule line as necessary.

e. Press the right DLY TIME/CURSOR button to position the 10th time marker to the reference vertical graticule line (8-division spacing between the 2nd and 10th time markers). The correct delay for an 8-divisions spacing is given in column 3 of Table 4-4.

f. CHECK—Delay time readout is within the limits given in Table 4-4, column 4 (Delay Readout Limits).

g. Using the remaining time-mark generator and B SEC/DIV switch settings given in Table 4-4, check the 8-division delay time accuracy for each A SEC/DIV switch setting given in column 1 of the table.

NOTE

When switching the A SEC/DIV switch setting to the next slower sweep speed, use the following procedure.

1. Rotate the SEC/DIV knob ccw to obtain the next slower A SEC/DIV setting to be checked.

2. Rotate the SEC/DIV knob cw to obtain the next B SEC/DIV setting to be used.

At the slower A SEC/DIV settings, the A Sweep trace may be removed from the display to eliminate the flicker due to sweep switching while making the actual timing accuracy check. Simply press in the SEC/DIV knob to obtain the B Delayed Sweep only. After making the check, pull the SEC/DIV knob out again to set the new sweep speed settings for the next check.

NOTE

Some setup time for each check may be saved by alternately checking the delay from the 2nd time marker to the 10th; then, at the next slower A SEC/DIV switch setting to be checked, from the 10th time marker back to the 2nd time marker. Zero the delay-time readout and align the starting time marker with the reference graticule to start at either end of the delay.

h. Disconnect the test equipment from the 336.

Table 4-4
Differential Timing Accuracy

Time-Mark Generator And A SEC/DIV Settings	B SEC/DIV Setting	Eight Division Delay	Delay Readout Limits
0.1 μs	0.1 μs	800 ns	787 ns to 813 ns
0.2 μs	0.1 μs	1.600 μs	1.574 μs to 1.626 μs
0.5 μs	0.1 μs	4.000 μs	3.935 μs to 4.065 μs
1 μs	0.1 μs	8.00 μs	7.87 μs to 8.13 μs
2 μs	0.2 μs	16.00 μs	15.74 μs to 16.26 μs
5 μs	0.5 μs	40.00 μs	39.35 μs to 40.65 μs
10 μs	1 μs	80.0 μs	78.7 μs to 81.3 μs
20 μs	2 μs	160.0 μs	157.4 μs to 162.6 μs
50 μs	5 μs	400.0 μs	393.5 μs to 406.5 μs
0.1 ms	10 μs	800 μs	787 μs to 813 μs
0.2 ms	20 μs	1.600 ms	1.574 ms to 1.626 ms
0.5 ms	50 μs	4.000 ms	3.935 ms to 4.065 ms
1 ms	0.1 ms	8.00 ms	7.87 ms to 8.13 ms
2 ms	0.2 ms	16.00 ms	15.74 ms to 16.26 ms
5 ms	0.5 ms	40.00 ms	39.35 ms to 40.65 ms
10 ms	1 ms	80.0 ms	78.7 ms to 81.3 ms
20 ms	2 ms	160.0 ms	157.4 ms to 162.6 ms
50 ms [a]	5 ms	400.0 ms	393.5 ms to 406.5 ms
0.1 s [a]	10 ms	800 ms	787 ms to 813 ms
0.2 s [a]	20 ms	1.600 s	1.574 s to 1.626 s

[a]**Set A Trigger MODE to NORM.**

4. Check X-Axis Gain

a. Connect the standard amplitude output of the calibration generator to the CH 1 OR X input via a 50 Ω Precision coaxial cable.

b. Set the calibration generator for a 20 mV standard-amplitude square-wave signal.

c. Set:

SEC/DIV	1 ms
VERT MODE	DUAL TRACE
VOLTS/DIV (both)	5 mV
Horizontal Display Mode	A (push SEC/DIV knob in)
Horizontal POSITION	Midrange

d. Set the Storage Display to X-Y (press MENU ON/OFF, MENU 1, MENU 3, MENU 2).

e. Use the CH 1 Vertical POSITION control to align the end of the trace with a convenient vertical graticule line as a measurement reference point.

NOTE

The Horizontal POSITION control should be set to midrange to give the CH 1 POSITION control full range for the STORE X-Y display.

f. CHECK—Storage X Axis for a horizontal display of 4 divisions ±0.2 division.

g. Set the Storage Display back to TIME (press MENU LAST, MENU 1).

h. Set:

CH 1 VOLTS/DIV	5 mV
DISPLAY MODE	NON STORE
SEC/DIV	X-Y (SEC/DIV knob ccw to X-Y)

i. Set the calibration generator for a 20 mV standard-amplitude signal.

j. Use the CH 1 Vertical POSITION control to center the trace horizontally, and use the CH 2 Vertical POSITION control to align the trace vertically with the center horizontal graticule line.

k. CHECK—X-Axis (horizontal) display amplitude is 4 divisions ±0.16 division (3.84 to 4.16 divisions).

l. Disconnect the test equipment from the 336.

5. Check X-Axis Bandwidth

a. Connect the leveled sine-wave generator output to the CH 1 OR X input connector via a 50 Ω Precision BNC cable and a 50 Ω termination.

b. Set the generator frequency to 50 kHz and adjust the output amplitude for a 6-division X-Axis (horizontal) display.

c. Increase the generator frequency to 1 MHz.

d. CHECK—X-Axis display is at least 4.2 divisions long.

e. Move the coaxial cable from the output of the leveled sine-wave generator to the output of the time-mark generator.

6. Check VAR SEC/DIV Range

a. Set:

VERT MODE	CH 1
CH 1 VOLTS/DIV	0.5 V
SEC/DIV	0.1 ms
TRIGGER MODE	AUTO

b. Set the generator for 0.1 ms time markers (1 time marker per division).

c. CHECK—Number of time markers per divisions increases to at least 5 markers per 2 divisions as the VAR SWP/HOLDOFF control is rotated counterclockwise.

d. Return the VAR SWP/HOLDOFF control to the detent position (fully clockwise).

7. Check Delay Time Jitter

a. Set:

Horizontal Display Mode	ALT (pull SEC/DIV knob out)
A SEC/DIV	1 ms
B SEC/DIV	1 μs
Delay Time Position	Minimum delay (press left DLY TIME/CURSOR position button until delay readout stops changing)

b. Set the time-mark generator for 0.1 ms time markers.

c. Use the Horizontal POSITION control to align start of the A Sweep with the first vertical graticule line.

d. Press in the SEC/DIV knob to obtain a display of the B Sweep only, and use right the DLY TIME/CURSOR position button to move the rising edge of the 1st time marker to the center vertical graticule line. Adjust the INTENSITY control as necessary to view the trace.

e. CHECK—Delay time jitter is 1 division or less horizontal movement of the rising edge of the time marker.

f. Press and release both DLY TIME/CURSOR position buttons at the same time to zero the delay time readout, then pull the SEC/DIV knob out for ALT Horizontal Display.

g. Set the delay time to 8.0 ms, then press the SEC/DIV knob back in for a B Sweep display only.

NOTE

At the amount of magnification displayed by the B Sweep display, the difference between delay-time positioning resolution and delay-time readout resolution becomes a factor in determining the exact position of the time marker rising edge.

h. Set the Delay Time Position as necessary to view the rising edge of the time marker near the graticule center.

i. CHECK—Repeat part g.

j. Disconnect the test equipment from the 336.

8. Check TRACE SEP Operation

a. Set:

Horizontal Display Mode	Alt (pull SEC/DIV knob out)

A SEC/DIV	1 ms
B SEC/DIV	0.1 ms
INTENSITY	For normal viewing

b. Use the CH 1 Vertical POSITION control to align the B Sweep trace with the center horizontal graticule line.

c. Press MENU ON/OFF, MENU 3, then MENU 2 to obtain the TRACE SEP Menu display.

d. Press MENU button 2 to decrement the trace separation between the A Sweep and the B Delayed Sweep.

e. CHECK—Each decrement decreases the trace separation by approximately 0.5 division and at 0.0 DIV separation, the traces are overlayed.

NOTE

The TRACE SEP Menu display times out. To recall it if it times out before you have completed the check, simply press the MENU LAST button.

EXTERNAL Z-AXIS, CALIBRATOR, AND CHART OUT

Equipment Required (see Table 4-1)

Calibration Generator (Item 2)
Test Oscilloscope with Probes (Item 6)
X-Y Plotter (Item 8)
50 Ω Precision BNC Coaxial Cable (Item 12)
Dual-input Coupler (Item 19)

NOTE

If starting the performance check procedure at this point, prior to application of power to the instrument, verify that the Nominal Voltage Selector is set for the correct ac source voltage. Connect the 336 to an appropriate power source and apply power to the instrument and test equipment. Make the initial control settings upon completion of the Power-on diagnostics routine, and allow a 20-minute warmup period before commencing the adjustments and checks for maximum accuracy.

INITIAL CONTROL SETTINGS

Control settings not listed do not affect the initial procedures and will be set when needed.

Set:

INTENSITY	Visible display
FOCUS	Best defined display
VERT MODE	CH 1
CH 1 VOLTS/DIV	1 V
AC-GND-DC (both)	AC
Vertical POSITION	Midrange
DISPLAY MODE	
NON STORE	On (LED illuminated)
STORE	Off
VIEW	Off
Horizontal Position	Midrange
Horizontal Display	A (SEC/DIV knob in)
SEC/DIV	0.5 ms
VAR SWP/HOLDOFF	CAL/NORM (in detent)
TRIGGER	
MODE	AUTO
SOURCE	CH 1
COUPLING	AC
A SLOPE	+ (plus)
A LEVEL	For a stable display with signal applied

Main MENU Selections

READOUT	ON
TIMEOUT	SLOW
STORE MODE	NORMAL

1. Check External Z-Axis Input (NON STORE Mode only)

a. Connect the output of the calibration generator to the CH 1 and EXT Z-AXIS IN input connectors via a 50 Ω BNC coaxial cable and a dual-input coupler.

b. Set the calibration generator output for a 5 V standard-amplitude square-wave signal.

c. CHECK—Top half of signal is blanked, and blanking starts at approximately 3 volts (3 divisions from the negative peak).

d. Disconnect the test equipment from the 336.

2. Check Calibrator Output

a. Set the test oscilloscope for a Volts/Div of 0.1 V (with 10X probe attached) and a Sec/Div of 1 ms. (The 336 may be used as the test oscilloscope.)

b. Connect the probe ground lead to chassis ground on the 336. Remove the grasping probe tip and place the pointed probe tip in the CAL OUT jack.

CAUTION

While the probe tip is in the CAL OUT jack, use care not to place excessive side force on the probe body. It is possible to break off the probe tip if care is not taken.

c. CHECK—Calibrator output waveform is a 0.3 V p-p square-wave signal with a frequency of approximately 1 kHz.

d. Disconnect the test equipment from the 336.

3. Check CHART OUT Operation

a. Set:

CH 1 VOLTS/DIV	1 V
SEC/DIV	0.5 ms
DISPLAY MODE	
NON STORE	Off
STORE	On
VIEW	Off

b. Connect the output of the function generator to the CH 1 input connector via a 50 Ω cable and a 50 Ω termination.

c. Set the function generator for a 1 kHz sine-wave signal and adjust the output amplitude for a 5-division display.

d. Press the ENTER button to store the displayed waveform.

e. Set the DISPLAY MODE to VIEW.

f. Connect the appropriate cables of the X-Y Plotter to the X, Y, and SIG GND connectors on the 336 right side panel.

g. Select the CHART Menu (use the Menu diagram in the front-cover to determine the selection path).

h. Press MENU button 3 to obtain the X-Y Plotter calibration voltage at the X and Y output connectors and apply power to the X-Y Plotter.

i. Adjust the X-Y Plotter sensitivity to calibrate the plot to the 336 crt graticule. Successive presses of the CAL button (MENU 3) switch the calibration voltages between full upper right and full lower left corner deflection of the 336 crt graticule. (Refer the X-Y Plotter Operator's Manual for its operation.)

j. When the X-Y Plotter is calibrated, lift the plotting pen and install a new graph paper (if desired).

k. With the plot pen still up, press MENU button 1 (FAST START) to commence the plot. When the pen reaches the starting point, lower it to draw the waveform. At the end of the plot, lift the pen. (Approximately 7 seconds is allowed for all pen lifting and pen lowering movements.)

l. CHECK—The waveform plotted corresponds to the waveform displayed by the 336.

m. Disconnect the X-Y Plotter and test equipment from the 336.

ADJUSTMENT PROCEDURE

INTRODUCTION

IMPORTANT—PLEASE READ BEFORE USING THIS PROCEDURE

The Adjustment Procedure is used to return the instrument to conformation with its Performance Requirements as listed in the "Specification" (Section 1).

LIMITS AND TOLERANCES

The limits and tolerances listed in this Adjustment Procedure are instrument specifications only if they are listed in the "Performance Requirements" column of the "Specification" (Section 1). Tolerances given are for the instrument undergoing calibration and do not include test equipment error. Calibration (adjustment) of the instrument must be accomplished at an ambient temperature between +20°C and +30°C, and the instrument must have had a warmup period of at least 20 minutes.

ADJUSTMENT INTERVAL

To ensure accuracy, readjust instruments after every 2000 hours of operation or once a year, if used infrequently. A more frequent interval may be necessary if your instrument is subjected to severe usage or harsh environments. Adjustments should be performed only after the checks in the "Performance Check Procedure" have indicated a need for readjustment of the instrument.

TEST EQUIPMENT REQUIRED

The test equipment listed in Table 4-1 (in Section 4) is a complete list of the equipment required to accomplish both the "Adjustment Procedure" in this section and the "Performance Check Procedure" in Section 4. Test equipment specifications described in Table 4-1 are the minimum necessary to provide accurate results. Therefore, equipment used must meet or exceed the listed specifications. Detailed operating instructions for test equipment are not given in this procedure. If more operating information is required, refer to the appropriate test equipment instruction manual.

When equipment other than that recommended is used, control settings of the test setup may need to be altered. If the exact item of equipment given as an example in Table 4-1 is not available, check the "Minimum Specification" column to determine if any other available test equipment might suffice to perform the check or adjustment.

PARTIAL PROCEDURES

This procedure is structured in subsections to permit adjustment of individual sections of the instrument (except the power supply) whenever a complete readjustment is not required. For example, if only the Vertical section fails to meet the Performance Requirements (or has had repairs made or components replaced), it can be readjusted with little or no effect on other sections of the instrument. However, if the Power Supply section has undergone repairs or adjustments that change the absolute value of any of the supply voltages, a complete readjustment of the instrument may be required.

At the beginning of each subsection is a list of all the front-panel control settings required to prepare the instrument for performing Step 1 in that subsection. Each succeeding step within a subsection should then be performed both in the sequence presented and in its entirety to ensure that control settings will be correct for ensuing steps.

INTERNAL ADJUSTMENTS AND ADJUSTMENT INTERACTION

Do not preset any internal controls prior to performing the Adjustment Procedure. Doing so may necessitate a

complete readjustment of the instrument, when only a partial readjustment might otherwise have been needed. To avoid unnecessary readjustment, change an internal control setting only when a Performance Characteristic cannot be met with the original setting. When it is necessary to change the setting of any internal control, always check for possible interaction that may require adjustment of other controls.

Specific interactions are called out within certain adjustment steps to indicate that the adjustments must be repeated until no further improvement is noted.

PREPARATION FOR ADJUSTMENT

It is necessary to remove the instrument cabinet to perform the Adjustment Procedure. See the "Cabinet" removal instructions located in the "Maintenance" section of this manual.

Before performing this procedure, ensure that the internal Line Voltage Selection jumper is set for the ac-power-source voltage being used. This procedure is written to accommodate either nominal ac-power-source range used (115 Vac or 230 Vac). If a choice of source voltage is available, then power supply regulation may be checked on both ranges for testing purposes.

All test equipment items required to accomplish a complete Adjustment Procedure are described in Table 4-1 at the beginning of Section 4, "Performance Check Procedure." The specific items of equipment needed to perform each subsection in this procedure are listed at the beginning of the subsection. The item number shown in parentheses with each piece of equipment refers to the equipment item number presented in Table 4-1.

Connect the test equipment to an appropriate ac-power-input source and connect the 336 to a variable autotransformer through an isolation transformer (items 9 and 10 in Table 4-1) that is set for the nominal ac-power-source voltage available. (Items 9 and 10 in Table 4-1 are for a nominal 115 V source voltage. If a 230 V source voltage is used, appropriate substitutions must be made.) Apply power and allow a 20-minute warmup period before commencing any adjustments.

Display

The most accurate display adjustments are made with a stable, well-focused, low-intensity display. Unless otherwise noted in a procedure step, adjust the INTENSITY, FOCUS, and TRIGGER LEVEL controls as needed to view the display.

INDEX TO ADJUSTMENT PROCEDURE

Triggering

Horizontal

External Z-Axis, Calibrator, CHART OUT, and Option 01

POWER SUPPLY AND DISPLAY

Equipment Required (see Table 4-1)

Time-Mark Generator (Item 3)
Function Generator (Item 4)
Digital Multimeter (Item 5)
Variable Autotransformer (Item 9)
Isolation Transformer (Item 10)
50 Ω BNC Coaxial Cable (Item 11)
50 Ω BNC Termination (Item 13)
Alignment Tool (Item 17)

See **ADJUSTMENT LOCATIONS** *at the rear of this manual for location of adjustments and test points.*

NOTE

Prior to applying power to the 336, verify that the Nominal Voltage Selector is set to the correct power source voltage. Connect the 336 to an appropriate power source via an autotransformer and an isolation transformer. Apply power to the instrument and test equipment. Make the initial 336 control settings as soon as the Power-on diagnostics routine has completed, and allow a 20-minute warmup period before commencing the adjustments and checks for maximum accuracy.

INITIAL CONTROL SETTINGS

Control settings not listed do not affect the initial procedure and will be set when necessary.

Set:

INTENSITY	Minimum
FOCUS	Midrange

NOTE

Performing the adjustment of Step 1 will normally require a complete adjustment of the instrument. If that is not intended, do not make the adjustment unless the +5 V falls outside of its specification during the regulation check of Step 2.

1. Adjust +5 V Digital Power Supply (A13R167)

a. Connect the digital voltmeter − (minus) lead to A4TP110 and connect the + (plus) lead to A4TP100.

b. ADJUST—+5 V_D Adj A15R167 for a digital voltmeter reading of +5.00 V.

NOTE

The checks in Step 2 require the availability of both 115 V and 230 V nominal source voltage supplies to complete fully. If only one source voltage is available, check the power supply regulation at that voltage only.

2. Check Power Supply Regulation

a. Vary ac input voltage from 90 V to 132 V.

b. CHECK—Digital Voltmeter reading remains at 5 V ±3% (4.85 V to 5.15 V) as the source voltage is varied between the limits in part a.

c. Turn off the instrument power and unplug the power cord.

WARNING

The power supply filter capacitors retain a charge for a short period of time after the power is turned off. Use care not to come in contact with exposed connections when moving the Nominal Voltage Selector.

d. Remove the top cover from the power supply module to gain access to the Nominal Voltage Selector. Move the selector plug (A13P50) to the 230 V nominal voltage position.

e. Set the ac source voltage for 230 V. Reconnect the power cord to the instrument and turn the 336 on.

f. Vary ac input voltage from 180 V to 250 V.

g. CHECK—Digital Voltmeter reading remains at 5 V ±3% (4.85 V to 5.15 V) as the source voltage is varied between the limits in part f.

h. Turn off the instrument and unplug the power cord. Return the Nominal Voltage Selector and the ac input source voltage to 115 V (or leave them both set for 230 V operation if that is the local nominal ac source voltage) and replace the power supply top cover. Apply power to the instrument.

3. Adjust CRT Grid Bias (A15R40)

a. Set:

A SEC/DIV	Clockwise to X-Y Mode
INTENSITY	Visible display
FOCUS	Best focused display

b. Connect the Digital Voltmeter + (plus) lead to the collector of Q660 (located on Horizontal Output board A12); minus lead remains on chassis ground. The collector lead of Q660 is the center lead of the transistor and is not marked.

c. Use the Channel 1 and Channel 2 Vertical POSITION controls to center the dot.

d. Set the INTENSITY control for a +25 V reading on the Digital Voltmeter.

e. ADJUST—CRT Grid Bias A15R40 for a visible dot, then back off on the adjustment until the dot just disappears.

f. Disconnect the Digital Voltmeter leads from the 336.

4. Adjust STORE Display Intensity (A1R920)

a. Set:

A and B SEC/DIV	1 ms
VERT MODE	CH 2
AC-GND-DC (both)	GND
VAR SWP/HOLDOFF	CAL/NORM (in detent)
Horizontal Display Mode	A (knob in)
TRIGGER	
SOURCE	CH 2
COUPLING	AC
MODE	AUTO
A SLOPE	+ (plus)
DISPLAY MODE	
STORE	ON (LED illuminated)
NON STORE	OFF
VIEW	OFF
Vertical POSITION	Midrange
Horizontal POSITION	Midrange
FOCUS	Best focused display
Main MENU Selections	
STORE MODE	NORMAL
READOUT	ON
TIMEOUT	NORMAL

b. ADJUST—STORAGE INTENSITY A1R920 for best viewing intensity of STORE trace display.

NOTE

Storage trace intensity is reduced when many of the menus displays are called up (for ease in viewing the choices). Depending on the STORAGE INTENSITY adjustment, the trace will be either just visible or completely blanked at those times.

5. Adjust Readout Intensity (A1R924)

a. Set:

Main MENU Selection	
SETTINGS	On

b. ADJUST—Readout Intensity (A1R924) for the best viewing intensity of crt readout.

6. Adjust TRACE ROTATION (A1R926)

a. Set:

DISPLAY MODE	
STORE	OFF
NON STORE	ON (LED illuminated)
VIEW	OFF
INTENSITY	Visible trace

b. Use the CH 2 POSITION control to position the auto baseline trace to the center horizontal graticule line.

c. ADJUST—TRACE ROTATION (A1R926) to align the baseline trace with the center horizontal graticule line.

7. Adjust Astigmatism (A15R150)

a. Set

DISPLAY MODE	
STORE	OFF
NON STORE	OFF
VIEW	OFF

b. Press in the MENU ON/OFF and LAST push buttons at the same time. Hold in both buttons momentarily and release together.

c. Press the TRIGGER RESET button to initialize the diagnostics, then press MENU button 3 to obtain a full screen display of all characters.

d. ADJUST—Astig potentiometer A15R150 in conjunction with front-panel FOCUS control for the best-defined display over the entire crt viewing area.

e. Press the MENU ON/OFF and the LAST push button in together and release to return the instrument to normal operation.

8. Adjust Geometry (A15R160)

NOTE

This adjustment has considerable effect on horizontal deflection of the crt and must be completed prior to attempting to adjust the horizontal timing.

a. Set:

DISPLAY	
NON STORE	ON (LED illuminated)
STORE	OFF
VIEW	OFF
CH 1 AC-GND-DC	DC
CH 2 VOLTS/DIV	10 mV
SEC/DIV	0.2 ms

b. Apply 0.2 ms time markers from the time-mark generator to the CH 1 OR X input connector via a 50 Ω coaxial cable and a 50 Ω termination.

c. Set the CH 1 Vertical POSITION control fully ccw and use the Horizontal POSITION control to align the time markers with the vertical graticule lines.

d. ADJUST—Geometry potentiometer A15R160 for 0.1 division or less horizontal bowing of the time markers at the right-most and left-most vertical graticule lines.

e. Disconnect the test equipment from the 336.

9. Check Z-Axis Compensation

a. Set:

VERT MODE	CH 2
X10 MAG	ON (button lighted)
A SEC/DIV	0.1 μs (10 ns with X10 MAG on)
CH 2 VOLTS/DIV	0.1V
CH 2 POSITION	Midrange
CH 2 AC-GND-DC	DC

b. Connect a 1 MHz positive-going fast-rise signal from the calibration generator to the CH 2 OR Y input via a 50 Ω BNC coaxial cable and a 50 Ω termination, and set the generator output amplitude for a 4-division step display.

c. Set the A TRIGGER LEVEL control to the center of the plus (+) SLOPE region and rotate the INTENSITY control to fully cw.

d. Use the Horizontal POSITION control to position the start of the sweep within the graticule viewing area.

e. CHECK—That the low-level portion of the display prior to the rising edge of the fast-rise signal is at least 2 horizontal divisions.

f. Turn off the X10 MAG and return the INTENSITY control to the proper brightness for normal viewing.

g. Disconnect the test equipment from the 336.

VERTICAL

Equipment Required (see Table 4-1)

Leveled Sine-Wave Generator (Item 1)
Calibration Generator (Item 2)
Function Generator (Item 4)
Isolation Transformer (Item 10)
50 Ω BNC Cable (2 required) (Item 11)
50 Ω Precision BNC Cable (Item 12)
50 Ω Termination (Item 13)
50 Ω 10X Attenuator (Item 14)
Adapter BNC male-to-miniature probe tip (Item 16)
Alignment Tool (Item 17)
10X Oscilloscope Probe (Item 18)
Dual-input Coupler (Item 20)

See **ADJUSTMENT LOCATIONS** *at the rear of this manual for location of test points and adjustments.*

NOTE

If starting the adjustment procedure at this point, prior to applying power to the 336, verify that the Nominal Voltage Selector is set to the correct power source voltage. Connect the 336 to an appropriate power source via an isolation transformer. Apply power to the instrument and test equipment. Make the initial 336 control settings as soon as the Power-on diagnostics routine has completed, and allow a 20-minute warmup period before commencing the adjustments and checks for maximum accuracy.

INITIAL CONTROL SETTINGS

Control settings not listed do not affect the initial procedure and will be set when needed.

Set:

INTENSITY	Visible display
FOCUS	Best defined display
VERT MODE	DUAL TRACE
VOLTS/DIV (both)	5 mV
VOLTS/DIV VAR (both)	CAL (in detent)
AC-GND-DC (both)	GND
CH 2 INVERT	Noninverted (no down arrow displayed)
Vertical POSITION (both)	Midrange
DISPLAY MODE	
ON STORE	ON (LED illuminated)
STORE	OFF
VIEW	OFF
Horizontal Display	A (SEC/DIV knob in)
Horizontal POSITION	Midrange
SEC/DIV	0.5 ms
VAR SWP/HOLDOFF	CAL/NORM (in detent)
TRIGGER	
MODE	AUTO
SOURCE	CH 2
COUPLING	AC
A LEVEL	For a stable display (with signal applied)
A SLOPE	+ (plus)
MAIN MENU Selections	
READOUT	ON
TIMEOUT	SLOW
HORIZ VAR	SEC/DIV
ACQ WINDOW	POST TRIG

1. Check Channel 1 and Channel 2 Probe Coding

a. Connect the standard accessory 10X probe to the CH 1 OR X input connector.

b. CHECK—CH 1 VOLTS/DIV readout changes to 50 mV.

c. Move the 10X probe to the CH 2 input connector.

d. CHECK—CH 2 VOLTS/DIV readout changes to 50 mV.

e. Disconnect the probe.

2. Check Channel 1 and Channel 2 Input Gate Current

a. Use the CH 1 and CH 2 POSITION control to align the traces with the center horizontal graticule line.

b. CHECK—Channel 1 trace shift is 0.1 division or less when switching the CH 1 Input Coupling switch between GND and AC.

c. CHECK—Channel 2 trace shift is 0.1 division or less when switching the CH 2 Input Coupling switch between GND and AC.

3. Check Input Coupling (AC-GND-DC) Switches and AC Coupling Lower Bandpass

a. Set:

AC-GND-DC (Vertical Input Coupling) (both)	DC
VERT MODE	CH 1

b. Connect a 20 mV, standard-amplitude square-wave signal from the calibration generator to the CH 1 input connector via a 50 Ω BNC cable (4-division display).

c. Position the bottom of the display to the center horizontal graticule line and set the Channel Input Coupling switch to GND (CH 1 or CH 2 as appropriate).

d. CHECK—Trace is at the center horizontal graticule line with no vertical deflection.

e. Set the Channel Input Coupling switch to AC.

f. CHECK—Display is centered about the center horizontal graticule line.

g. Set the VERT MODE and TRIGGER SOURCE to CH 2 and move the test signal to the CH 2 input connector.

h. Repeat parts c through f for the CH 2 Input Coupling switch.

i. Disconnect the test equipment from the instrument.

j. Set:

VERT MODE	DUAL TRACE
VOLTS/DIV (both)	0.5 V
SEC/DIV	0.5 s ROLL
CH 1 AC-GND-DC	AC
CH 2 AC-GND-DC	DC

k. Connect one of the accessory 10X probes to the CH 2 input connector and remove the grasping probe tip.

l. Connect the output of the function generator to the probe tip via a 50 Ω termination and a BNC male-to-miniature-probe-tip adapter.

m. Set the generator output for a 1 Hz sine wave and adjust the output amplitude control for a 5-division display amplitude.

n. Switch the CH 2 AC-GND-DC switch to AC.

o. CHECK—Display amplitude is 3.5 divisions or more.

p. Move the probe from the CH 2 input to the CH 1 input.

q. CHECK—Display amplitude is 3.5 divisions or more.

r. Disconnect the test equipment from the 336.

4. Adjust CH 2 Invert Balance (A1R418)

a. Set:

VERT MODE	CH 2
CH 2 VOLTS/DIV	5 mV
CH 2 AC-GND	DC GND

b. ADJUST—Invert Bal A1R418 for minimum trace shift when switching between noninverted and inverted (down-arrow symbol displayed) CH 2 displays.

5. Adjust Channel 1 Variable Balance (A1R118)

a. Set:

VERT MODE	CH 1
CH 1 VOLTS/DIV	5 mV
CH 1 AC-GND-DC	GND

b. Use the CH 1 Vertical POSITION control to position the trace to the center horizontal graticule line.

c. ADJUST—CH 1 Var Bal A1R118 for minimum trace shift as the CH 1 VOLTS/DIV VAR control is rotated between fully clockwise (cw) and fully counterclockwise (ccw).

d. Return the CH 1 VAR control to the CAL position (fully cw).

6. Adjust Channel 1 and Channel 2 Step Attenuator Balance (A1R151 and A1R451)

a. Set:

CH 1 VOLTS/DIV	20 mV
CH 2 INVERT	Noninverted (no down arrow symbol displayed)

b. ADJUST—CH 1 Step Atten Bal A1R151 for minimum trace shift as the CH 1 VOLTS/DIV switch is rotated between 20 mV and 5 mV.

c. Set:

VERT MODE	CH 2
CH 2 VOLTS/DIV	20 mV

d. ADJUST—CH 2 Step Atten Bal A1R451 for minimum trace shift as the CH 2 VOLTS/DIV switch is rotated between 20 mV and 5 mV.

7. Check Channel 2 Variable Balance

a. Set:

CH 2 VOLTS/DIV	5 mV

b. CHECK—Trace shift is 2 divisions or less when rotating the CH 2 VAR control between fully clockwise and fully counterclockwise.

c. Return the CH 2 VAR control to the CAL position (fully cw).

8. Adjust Channel 1 and Channel 2 Position Centering (A1R164 and A1R464)

a. Set:

VERT MODE	DUAL TRACE
CH 1 VOLTS/DIV	5 mV
SEC/DIV	10 μs

b. Position the white index dot on the CH 1 and CH 2 Vertical POSITION controls to the top (midrange rotation).

c. ADJUST—CH 1 Position Center A1R164 to align the CH 1 trace with the center horizontal graticule line.

d. ADJUST—CH 2 Position Center A1R464 to align the CH 2 trace with the center horizontal graticule line.

9. Check Channel 1 and Channel 2 POSITION Range

a. Set:

AC-GND-DC (both)	AC
CH 1 VOLTS/DIV	0.1 V
CH 2 VOLTS/DIV	50 mV
TRIGGER SOURCE	EXT

b. Connect a 50 kHz sine-wave signal from the function generator to the CH 1 OR X input connector via a 50 Ω BNC cable and a 50 Ω BNC termination. Connect the function generator Trig Out signal to the 336 EXT TRIG IN connector via a 50 Ω BNC cable and a 50 Ω BNC termination.

c. Set the sine-wave generator output for a 6-division display and adjust the A TRIG LEVEL control for a stable display.

d. Set the CH 1 VOLTS/DIV switch to 50 mV (signal amplitude of 12 divisions).

e. CHECK—Top of displayed waveform will position down to (or below) the center horizontal graticule line, and

bottom of display will position up to (or above) the center horizontal graticule line using the channel POSITION control.

f. Move the test signal from the CH 1 input to the CH 2 input. (Verify that the display amplitude is still 6 divisions. Adjust the the generator output amplitude, if necessary.)

g. CHECK—Repeat part e using the CH 2 POSITION control.

h. Disconnect the test equipment from the 336.

10. Adjust/Check Channel 1 and Channel 2 Vertical Gain (A11R74 and A1R108)

a. Set:

VERT MODE	CH 2
CH 2 VOLTS/DIV	5 mV
AC-GND-DC (both)	DC
A SEC/DIV	0.5 ms
TRIGGER	
SOURCE	CH 2

b. Connect a 20 mV, standard-amplitude square-wave signal from the calibration generator to the CH 2 input connector via a 50 Ω BNC cable.

c. Vertically center the display.

d. ADJUST—Vert Output Gain A11R74 for a 4-division CH 2 display.

e. Move the test signal to the CH 1 input connector and set the VERT MODE and TRIGGER SOURCE to CH 1.

f. Set the CH 1 VOLTS/DIV to 5 mV and vertically center the display.

g. ADJUST—CH 1 Gain A11R108 for a 4-division CH 1 display.

h. CHECK—Change the CH 1 VOLTS/DIV switch and calibration generator settings as shown in Table 5-1 and check that the deflection accuracy is within 3% for all VOLTS/DIV switch settings listed.

i. Set the VERT MODE and TRIGGER SOURCE to CH 2, and set the calibration generator output for 50 mV.

j. Move the test signal from the CH 1 input to the CH 2 input and vertically center the display.

k. CHECK—Repeat part h for all the CH 2 VOLTS/DIV switch settings.

l. Return the calibration generator output to 20 mV.

Table 5-1
Vertical Deflection Accuracy

VOLTS/DIV Setting	Calibration Generator Amplitude	Divisions Of Deflection
10 mV	50 mV	4.85 to 5.15
20 mV	0.1 V	4.85 to 5.15
50 mV	0.2 V	3.88 to 4.12
0.1 V	0.5 V	4.85 to 5.15
0.2 V	1 V	4.85 to 5.15
0.5 V	2 V	3.88 to 4.12
1 V	5 V	4.85 to 5.15
2 V	10 V	4.85 to 5.15
5 V	20 V	3.88 to 4.12
10 V	50 V	4.85 to 5.12

11 Adjust/Check Storage Gain (A11R102 and A5R47)

a. Set:

CH 2 VOLTS/DIV	5 mV
DISPLAY	
NON STORE	Off
STORE	On (LED illuminated)
VIEW	Off
Main MENU Selection	
CURSORS	ON
TRIGGER	
A LEVEL	Adjust for a stable, triggered display

b. Use the DLY TIME/CURSOR push buttons and MENU 1 button (CURSOR SEL) to position one cursor dot on the top of the standard-amplitude square wave and the other on the bottom of the waveform.

c. ADJUST—Storage Gain A5R47 for a ΔV readout of 20.0 mV ±0.4 mV. (Changes in the readout should be centered around 20 mV).

d. ADJUST—Storage Wfm Gain A11R102 for a STORE display amplitude of 4 divisions.

e. CHECK—Change the VOLTS/DIV setting and calibration generator standard-amplitude output to each of the settings given in Table 5-2 and check the storage gain accuracy and cursor ΔV readout accuracy for each VOLTS/DIV setting given.

f. Press MENU button 2 to turn off the CURSORS Mode.

g. Set the calibration generator output to 0.5 V.

12 Adjust STORE and READOUT Display Vertical Position (A11R126 and A6R704)

a. Press in the MENU ON/OFF and MENU LAST buttons together and release at the same time (336 enters the diagnostics mode).

b. Press the TRIGGER RESET button, then press the MENU ON/OFF button to start the Waveform RAM Check.

c. Use the Horizontal POSITION control to move the right end of the display to the center vertical graticule line.

d. ADJUST—Storage Position A11R126 to position the center data value level to the center horizontal graticule line.

e. Press the Trigger MODE RESET button to exit the Waveform RAM check, then press MENU button 3 to display all characters.

f. ADJUST—RO Y Position A6R704 to vertically position the readout display totally within the graticule area with equal spacing at the top and bottom of the readout.

g. Press the MENU ON/OFF and the MENU LAST buttons in together and release to exit the diagnostics mode.

13 Adjust Storage DC Level (A5R42)

a. Set:

AC-GND-DC (both)	GND
DISPLAY MODE	
NON STORE	On (LED illuminated)
STORE	On (LED illuminated)
VIEW	Off

b. Use the CH 2 Vertical POSITION control to position the traces near the center of the graticule area.

c. ADJUST—Storage DC Level A5R42 to overlay the STORE trace on the NON STORE trace.

Table 5-2
Storage Deflection Accuracy

VOLTS/DIV Setting	Generator Setting	Waveform Deflection Limits	Voltage Readout Limits
10 mV	50 mV	4.85 to 5.15	48.1 mV to 51.9 mV
20 mV	0.1 V	4.85 to 5.15	96.2 mV to 103.8 mV
50 mV	0.2 V	3.88 to 4.12	192 mV to 208 mV
0.1 V	0.5 V	4.85 to 5.15	481 mV to 519 mV
0.2 V	1 V	4.85 to 5.15	962 mV to 1.038 V
0.5 V	2 V	3.88 to 4.12	1.92 V to 2.08 V
1 V	5 V	4.85 to 5.15	4.81 V to 5.19 V
2 V	10 V	4.85 to 5.15	9.62 V to 10.38 V
5 V	20 V	3.88 to 4.12	19.2 V to 20.8 V
10 V	50 V	4.85 to 5.15	48.1 V to 51.9 V

14 Adjust TRIG VIEW Gain and Position (A2R320 and A2R330)

a. Set:

VERT MODE	TRIG VIEW (STORE Mode turns off automatically)
TRIGGER	
MODE	NORM
SOURCE	EXT

b. Move the standard-amplitude test signal from the CH 2 input to the EXT TRIG IN connector.

c. Verify that the generator output is set for a 0.5 V standard-amplitude signal.

d. Use the A TRIGGER LEVEL control to vertically center the TRIG VIEW display on the + (plus) SLOPE.

e. ADJUST—Trig View Gain A2R320 for a 5-division ±5% display amplitude (4.75 to 5.25 divisions).

f. ADJUST Trig View Position A2R330 to align the start of the TRIG VIEW trace with the center horizontal graticule line.

g. Set the TRIG SOURCE to EXT/10 and set the calibration generator output to 5 V. Use the A TRIG LEVEL control to vertically center the display on the + (plus) SLOPE.

h. CHECK—TRIG VIEW display amplitude is 5 divisions ±5% (4.75 to 5.25 divisions).

i. Disconnect the test equipment from the 336.

15. Adjust Frequency Compensation (A11C64, A11R86, A11C86, A11R87, A11C87, A11R151, A11C151, A1R402, A1C402, A1R102, A1C102, A1C195, A1C816, and A5R50)

a. Set:

VERT MODE	CH 2
VOLTS/DIV	5 mV
X10 MAG	ON
SEC/DIV	0.1 μs (with X10 MAG on)
TRIGGER	
MODE	AUTO
SOURCE	CH 2

b. Connect the calibration generator fast-rise positive-going signal to the CH 2 input connector via a 50 Ω Precision coaxial BNC cable, a 10X attenuator, and a 50 Ω termination.

c. Set the generator output amplitude for a 4-division signal display at 1 MHz.

d. Set the A TRIGGER LEVEL for a stable display of the leading edge of the signal on − (minus) SLOPE.

e. Use the Horizontal POSITION control to position the rising edge of the signal to near the center of the graticule area, and set the DISPLAY MODE to STORE.

f. ADJUST—Storage HF Compensation A5R50, CH 2 Compensation A1R402 and A1C402, and Vertical Compensation A1C816 for the best flat-top display with aberrations of 10% peak-to-peak (0.4 division) or less.

g. Set:

DISPLAY MODE	NON STORE
X10 MAG	ON
A SEC/DIV	0.1 μs (with X10 MAG on)
TRIGGER	
SLOPE	+ (plus)

h. Set the Trigger LEVEL control to display the entire leading edge of the fast rise + signal. Use the Horizontal POSITION control to position the rising edge near the center vertical graticule line.

i. ADJUST—Vertical Output Compensation A11C64, A11R86, A11C86, A11R87, A11C87, A11R151, and A11C151 for the best flat-top display with aberrations of 5% peak-to-peak (0.2 division) or less.

NOTE

Vertical Comp A1C816 may require compromise adjustment to obtain the correct HF response for the NON-STORE waveform.

j. CHECK—That the aberrations at 10 mV, 20 mV, and 50 mV per divisions are within 5 % (0.2 division) or less and that they are within 7% (0.14 division on a 2-division signal) or less at 0.5 V per division. Change the fast-rise signal output amplitude and remove the 10X attenuator as necessary to maintain a 4-division display amplitude (2 divisions maximum at a VOLTS/DIV setting of 0.5 V.)

NOTE

If the aberrations exceed the specification at any VOLTS/DIV setting checked in part j, it may be necessary to select values for A1R313 and A1R318. This procedure is done when the factory calibration is performed, so it should not be required in a normal adjustment procedure. However, should selection be considered necessary, the selectable values are given in "Selectable Components," located in the Maintenance section of this manual. Tektronix part numbers are given in the "Replaceable Electrical Parts" section of this manual. If new component values are selected, repeat this Step from part a.

k. Return the VOLTS/DIV setting to 5 mV, insert the 10X attenuator back into the test setup, and adjust the generator output amplitude to reobtain a 4-divsion display amplitude.

l. Use the CH 2 Vertical POSITION control to position the top of the display to the bottom graticule line.

m. CHECK—For a flat-top display with aberrations of 7% peak-to-peak (0.28 division) or less.

n. Use the CH 2 Vertical POSITION control to position the top of the display to the top graticule line.

o. Repeat the check of part m.

p. If the position effect aberrations exceed 7%, continue with part q. If not, skip to part v.

q. ADJUST—Vert Ampl Bal A11R70 to obtain 7% or less aberration on the CH 2 display.

r. Repeat parts l through o to recheck the position effect aberrations.

s. Disconnect the fast-rise + test signal from the CH 2 input, then connect a 20 mV standard-amplitude signal from the calibration generator to the CH 2 input via a 50 Ω coaxial cable.

t. Set:

A SEC/DIV	0.2 ms
TRIGGER	
LEVEL	For a stable display
Horizontal POSITION	Midrange

u. ADJUST—Vert Output Gain A11R74 for a 4-division vertical spacing between the displayed traces. Do not disconnect the standard-amplitude signal coaxial cable from the CH 2 input.

v. Connect the fast-rise + test signal coaxial cable with 50 Ω termination and 10X attenuator the CH 1 input.

w. Set:

A SEC/DIV	0.1 μs
VERT MODE	CH 1
TRIGGER	
SOURCE	CH 1
LEVEL	Stable display of entire leading edge

x. ADJUST—CH 1 Compensation A1R102, A1C103, and A1C195 for the best flat-top display with aberrations of 5% peak-to-peak (0.2 division) or less.

y. Repeat parts j and k for CH 1.

z. Use the CH 1 Vertical POSITION control to position the top of the display to the bottom graticule line.

aa. CHECK—For a flat-top display with aberrations of 7% peak-to-peak (0.28 division) or less.

ab. Use the CH 1 Vertical POSITION control to position the top of the display to the top graticule line.

ac. Repeat the check of part aa.

ad. If the position effect aberrations exceed the given tolerance, continue with part ae. If not, skip to part ah.

ae. ADJUST—Vert Ampl Bal A11R70 to obtain 7% or less aberrations on the front corner of the CH 1 display.

af. Repeat parts z through ac to recheck the position effect aberrations on the CH 1 signal.

ag. Set the VERT MODE to CH 2 and repeat parts t and u to set the correct vertical output gain.

ah. Disconnect the test equipment from the 336.

16. Adjust Trig View Compensation (A1C744)

a. Connect the calibration generator fast-rise + signal to the EXT TRIG IN connector via a 50 Ω coaxial cable and a 50 Ω termination.

b. Set:

VERT MODE	TRIG VIEW
AC-GND-DC (both)	GND
TRIGGER	
SOURCE	EXT
MODE	NORM
COUPLING	DC

c. Set the calibration generator output amplitude for a 4-division vertical display at 1 MHz, and use the A TRIG LEVEL control to display the entire rising edge of the TRIG VIEW display.

d. ADJUST—Trig View Compensation A1C744 for the best flat-top display with aberrations of 10% peak-to-peak (0.4 division) or less.

e. Disconnect the test equipment from the 336.

17. Adjust Channel 1 and Channel 2 Input Compensation

a. Set:

VERT MODE	CH 1
CH 1 VOLTS/DIV	5 mV (50 mV with 10X probe)
AC-GND-DC (both)	DC
A SEC/DIV	2 ms
TRIGGER	
MODE	AUTO
SOURCE	CH 1
A LEVEL	Stable display
SLOPE	+ (plus)
COUPLING	AC

b. Connect the calibration generator high-amplitude output signal to the CH 1 input connector via a 50 Ω 10X attenuator, a BNC male-to-miniature probe-tip adapter, and the standard accessory 10X probe.

c. Set the calibration generator for a 5-division vertical amplitude display at 1 kHz; then, set the A SEC/DIV setting to 0.2 ms.

d. ADJUST—Probe low-frequency compensation for the best flat-top display.

e. Remove the 10X attenuator from the test setup.

f. Set:

CH 1 VOLTS/DIV	0.5 V (with 10X probe)
A SEC/DIV	2 ms

g. Set the calibration generator for a 5-division display amplitude; then, set the A SEC/DIV back to 0.2 ms.

h. ADJUST—CH 1 50 mV Comp A1C20 and A1C22 for the best flat-top display with aberrations of 2% peak-to-peak (0.1 division) or less.

i. Set:

CH 1 VOLTS/DIV	5 V (with 10X probe)
A SEC/DIV	2 ms

j. Repeat part g.

k. ADJUST—CH 1 0.5 V Comp A1C10 and A1C12 for the best flat-top display with aberrations of 2% peak-to-peak (0.1 division) or less.

l. Set:

CH 2 VOLTS/DIV	5 mV (50 mV with 10X probe)
A SEC/DIV	2 ms
TRIGGER	
SOURCE	CH 2

m. Reinsert the 10X attenuator between the calibration generator output and the BNC male-to-miniature probe tip adapter and move the probe from the CH 1 input connector to the CH 2 input connector.

n. Repeat part g.

o. ADJUST—CH 2 Input capacitor A1C302 for the best flat-top display. Do not readjust the probe low-frequency compensation. Capacitor A1C302 is adjustable to match the Channel 2 input capacitance with the Channel 1 input capacitance.

NOTE

If a correct match between the Channel 2 input capacitor and the Channel 1 input capacitor cannot be obtained, it may be necessary to select the value of CH 1 input capacitor C2. As this process is done in factory calibration, it should not be required in a normal adjustment procedure. However, if a component change is necessary, the selectable values are given in the Maintenance section of this manual under "Selectable Components." Part numbers are given in the "Replaceable Electrical Parts" section of this manual.

p. Remove the 10X attenuator from the test setup.

q. Set:

CH 2 VOLTS/DIV	0.5 V (with 10X probe)
A SEC/DIV	2 ms

r. repeat part g.

s. ADJUST—CH 2 50 mV Comp A1C320 and A1C322 for best flat-top display with aberrations of 2% peak-to-peak (0.1 division) or less.

t. Set:

CH 2 VOLTS/DIV	5 V (with 10X probe)
A SEC/DIV	2 ms

u. repeat part g.

v. ADJUST—CH 2 0.5 V Comp A1C310 and A1C312 for best flat-top display with aberrations fo 2% peak-to-peak (0.1 division) or less.

w. Disconnect the test equipment from the 336.

18. Adjust EXT and EXT/10 Trigger Compensation (A1C912, A1C914, A1C916, A2C103, and A2C104)

a. Set:

VERT MODE	TRIG VIEW
A SEC/DIV	2 ms
TRIGGER	
SOURCE	EXT
COUPLING	DC
MODE	NORM
LEVEL	Vertically center the TRIG VIEW display

b. Connect the calibration generator high-amplitude test signal to the EXT TRIG IN connector via a 50 Ω coaxial cable and a 10X attenuator.

c. Set the calibration generator output amplitude for a 5-division signal and move the A SEC/DIV setting back to 0.2 ms.

d. ADJUST—EXT Trig Comp A1C914 and A1C916 for the best flat-top display with aberrations and flatness of 10% peak-to peak (0.5 division) or less.

e. Disconnect the coaxial cable from the EXT TRIG IN connector and connect the 10X accessory probe to the EXT TRIG IN connector.

f. Connect the probe tip to the calibration generator via a BNC male-to-miniature probe tip adapter.

g. ADJUST—Ext Trig Input capacitor A1C912 for the best flat-top display.

h. Disconnect the test equipment from the EXT TRIG IN connector and remove the probe.

i. Connect the calibration generator high-amplitude test signal to the EXT TRIG IN connector via a 50 Ω coaxial cable.

j. Set the Trigger SOURCE to EXT/10.

k. ADJUST—EXT/10 Trig Comp A2C102 and A2C104 for the best flat-top display with aberrations of 10% peak-to-peak (0.5 division) or less.

l. Disconnect the test equipment from the 336.

19. Check Bandwidth

a. Set:

VERT MODE	CH 2
VOLTS/DIV (both)	5 mV
A SEC/DIV	10 μs
TRIGGER	
SOURCE	CH 2
COUPLING	AC
LEVEL	For a stable display on the + SLOPE

b. Connect the leveled sine-wave generator output to the CH 2 input via a 50 Ω coaxial cable and a 50 Ω termination.

c. Set the generator frequency for 50 kHz and set the output amplitude for a 6-division vertical display.

d. Increase the sine-wave generator output frequency to 50 MHz.

e. CHECK—NON STORE display amplitude is 4.2 divisions peak-to-peak or more.

NOTE

If the bandwidth for either Channel falls below specification, the input compensation adjustments should be checked to determine if they have been correctly set. A fast-rise signal from the calibration generator should display a rise time of approximately 7 ns or less in order for the bandwidth to meet specification. It may be necessary to compromise the input adjustments to obtain the proper rise time. The aberration specifications should not be exceeded in any case.

f. Set the Display Mode to STORE and set the A SEC/DIV setting to 0.1 μs.

g. CHECK—STORE display amplitude is 4.2 divisions peak-to-peak or more.

h. Set the Display Mode to NON STORE and set the A SEC/DIV setting to 10 μs.

i. Repeat parts c through h for each VOLTS/DIV setting up to 1 V.

NOTE

The sine-wave generator output is limited to five volts peak-to-peak. Therefore, at the 1 V setting, set the reference signal amplitude to 5 divisions and check for a display amplitude of at least 3.5 divisions at 50 MHz.

j. Set:

VERT MODE	CH 1
TRIGGER	
SOURCE	CH 1

k. Repeat parts c through i for Channel 1.

l. Set:

VERT MODE	TRIG VIEW
A SEC/DIV	10 μs
TRIGGER	
SOURCE	EXT
MODE	NORM

m. Set the sine-wave generator frequency to 50 kHz and move the test signal from the CH 1 connector to the EXT TRIG IN connector.

n. Adjust the A TRIG LEVEL control for a stable display near the center of the graticule area.

o. Set the generator output amplitude for a 5-division vertical display. Adjust the A TRIG LEVEL control as necessary to center the display.

p. Increase the generator output frequency to 35 MHz.

q. CHECK—TRIG VIEW display amplitude is 3.5 divisions peak-to-peak or more.

r. Set the TRIG SOURCE to EXT/10 and reestablish a 5-division, 50 kHz reference signal display.

s. Repeat parts p and q.

t. Disconnect the coaxial cable from the EXT TRIG IN connector.

u. Set:

VERT MODE	ADD
VOLTS/DIV (both)	5 mV
TRIGGER	
SOURCE	CH 1
MODE	AUTO

v. Connect the leveled sine-wave generator output to the CH 1 and CH 2 input connectors via a 50 Ω coaxial cable, a 50 Ω termination, and dual-input coupler.

w. Set the generator output frequency to 50 kHz and adjust the output amplitude to obtain a 6-division ADD display.

x. Increase the generator output frequency to 30 MHz.

y. CHECK—ADD display amplitude is 4.2 divisions peak-to-peak or more.

20. Check Common-Mode Rejection Ratio

a. Set:

VERT MODE	DUAL TRACE
VOLTS/DIV (both)	10 mV
A SEC/DIV	0.1 μs
CH 2 INV	Inverted (down arrow displayed)

b. Set the generator output frequency to 10 MHz and set the output amplitude for a 5-division vertical display of the CH 1 and CH 1 signals. Use the Vertical POSITION controls to center the two traces vertically.

c. Set:

VERT MODE	ADD
VOLTS/DIV (both)	5 mV

d. CHECK—Trace deflection is 1 division or less.

e. Disconnect the test equipment from the 336.

21. Check 5 kHz Dropout

a. Set:

VERT MODE	CH 1
CH 1 VOLTS/DIV	1 V
DISPLAY MODE	STORE
A SEC/DIV	0.1 ms

b. Connect the function generator output to the CH 1 input via a 50 Ω coaxial cable and a 50 Ω termination.

c. Set the function generator for a sine-wave output at 5 kHz.

d. Set the generator output amplitude for a 5-division vertical display. Use the CH 1 Vertical POSITION control to center the display.

e. CHECK—For any noticeable upward or downward spikes from the CH 1 trace.

22. Check Storage Acquisition Window

a. Set the function generator for a positive-going pulse at 100 Hz. Set the generator output to obtain a 5-division display (if necessary).

b. Use the MENU controls to set the Storage Acquisition Window to PRE TRIG. (The STORE trace is dimmed while the Menu is displayed.)

c. Use the Horizontal POSITION control to align the start of the trace with the first vertical graticule line.

d. CHECK—Rising edge of the pulse is near the 9th vertical graticule line.

e. Recall the Acquisition Window Menu by pressing the MENU LAST button and set the Acquisition Window to MID TRIG.

f. CHECK—Rising edge of the pulse is near the center vertical graticule line.

g. Set the Acquisition Window to POST TRIG.

h. CHECK—Rising edge of the pulse is near the 2nd vertical graticule line.

23. Adjust/Check ENVELOPE Storage Mode

NOTE

Instruments with serial numbers below B300201 do not include the Envelope Offset adjustment. For those serial number instruments, skip parts b, c, d, and e of this step.

a. Set:

VERT MODE	CH 1
CH 1 AC-GND-DC	GND
DISPLAY MODE	
STORE	ON (button illuminated)
NON STORE	OFF
VIEW	OFF
MAIN MENU Selections	
STORE MODE	ENV
A SEC/DIV	2 ms
TRIGGER	
SOURCE	CH 2 (untriggered display)

b. With the ENVELOPE Menu displayed, press MENU button 2 to decrement the number of acquisitions to 1 TIMES.

c. Use the CH 1 Vertical POSITION control to center the trace.

d. ADJUST—Envelope Offset A5R56 for minimum trace width.

e. CHECK—Envelope trace width is less than 0.2 divisions.

f. Recall the ENVELOPE menu and press MENU button 1 to increment the number of acquisitions to continuous (infinity symbol displayed).

g. Set the CH 1 AC-GND-DC switch to AC.

h. CHECK—Display fills to a solid bright band, 5 divisions in amplitude.

i. Press MENU button 3 (RESET).

j. CHECK—Acquired envelope is cleared and a new acquisition starts.

k. Disconnect the coaxial cable from the function generator and connect the leveled sine-wave generator output to the CH 1 input connector.

l. Set:

CH 1 VOLTS/DIV	5 mV
CH 1 AC-GND-DC	DC
TRIGGER	
SOURCE	CH 1

m. Recall the ENVELOPE Menu and press MENU button 2 to decrement the number of acquisitions to 1 TIMES.

n. Set the sine-wave generator output for a 50 kHz reference signal, 6 divisions in amplitude.

o. Increase the generator frequency to 10 MHz.

p. CHECK—ENVELOPE display is 4.2 divisions peak-to-peak or more.

q. Disconnect the test equipment from the 336.

24. Check AVERAGE Storage Mode

a. Set:

MAIN MENU Selections	
STORE MODE	AVERAGE
A SEC/DIV	0.1 μs

b. With the AVERAGE Menu displayed, press MENU button 2 to decrement the number of averages to 8 TIMES (if not already at that setting).

c. CHECK—Number at lower right counts down to 1, then switches to AVG at the end of the count.

d. Recall the AVERAGE Menu and press MENU button 1 to increment the number of acquisitions to be averaged.

e. CHECK—That the number of times increments to 16, 32, 64, 128, then 256; one increment for each press of the MENU 1 button.

f. Press MENU button 2 to decrement the number back to 8 TIMES.

g. Set the STORE MODE back to NORMAL.

25. Check PROCESS Operation

a. Connect a 5 mV standard-amplitude square-wave signal from the output of the calibration generator to the CH 1 and CH 2 input connectors via a 50 Ω coaxial cable and a dual-input coupler.

b. Set:

VERT MODE	DUAL TRACE
VOLTS/DIV (both)	5 mV
AC-GND-DC (both)	DC
SEC/DIV	1 ms
STORAGE	PROCESS

c. Adjust the CH 1 and CH 2 Vertical POSITION controls to place the CH 1 and CH 2 displays at convenient locations within the graticule area.

d. Switch Channel 1 and Channel 2 AC-GND-DC switches to GND to acquire a ground reference for calculations. (Do not reposition the Vertical POSITION controls after acquiring the ground reference. If repositioning occurs, reacquire the ground reference.)

e. Set both AC-GND-DC switches back to DC.

f. Select WFM processing by pressing MENU button 1, then press MENU button 1 again to select CH 1 + CH 2.

g. CHECK—Peak-to-peak amplitude of the added signals is 2 divisions within 6% (1.88 to 2.12 divisions p-p).

h. Press MENU button 2 to select CH 1 − CH 2.

i. CHECK—Display peak-to-peak amplitude is zero divisions within 6% (0.12 division p-p) disregarding transition spikes.

j. Press MENU button 3 to select CH 1 x CH 2.

k. CHECK—Display peak-to-peak amplitude is 1 division within 7% (0.93 to 1.07 division).

l. Press the MENU LAST button to discontinue WFM processing and disconnect the test equipment from the instrument.

m. Connect the output of a leveled sine-wave generator to the CH 1 input connector via a 50 Ω precision coaxial cable and a 50 Ω termination.

n. Set:

VERT MODE	CH 1
SEC/DIV	5 μs

o. Set the generator frequency for 250 kHz and adjust the output amplitude for a display of 6 divisions.

p. With the PROCESS Menu displayed, press MENU button 2 to select PARAMETERS then press MENU button 1 to select RMS.

q. Set CH 1 AC-GND-DC switch to GND to acquire a ground reference (readouts go to zero), then set it back to DC.

NOTE

Do not vertically reposition the channel display after switching the input coupling back to DC. If this should occur, reacquire a ground reference before checking the RMS readout of the signal display.

r. CHECK—RMS readout is 10.6 mV ±0.6 mV (10 mV to 11.2 mV).

s. Press MENU button 2 to select P-P.

t. CHECK—P-P readout is 30 mV ±1 mV (29 mV to 31 mV).

u. Press MENU button 3 to select MEAN.

v. CHECK—MEAN readout is 0.0 mV ±0.6 mV (−0.6 mV to 0.6 mV).

w. Disconnect the coaxial cable from the leveled sine-wave generator.

26. Check CHOP and DUAL TRACE VERT MODE

a. Connect the function generator output to the CH 1 input via a 50 Ω coaxial cable and a 50 Ω termination.

b. Set the function generator for a sine-wave output at a frequency of 10 Hz.

c. Set:

VERT MODE	DUAL TRACE
VOLTS/DIV (both)	1 V
A SEC/DIV	10 ms
TRIGGER	
MODE	NORM
LEVEL	For a stable display
DISPLAY MODE	NON STORE

d. Set the generator output amplitude for about a 5-division display and use the Vertical POSITION controls to position both traces within the graticule area.

e. CHECK—Both traces are displayed simultaneously (chopped).

f. Set the A SEC/DIV setting to 0.5 ms.

g. CHECK—Traces are displayed alternately.

h. Set the VERT MODE to CHOP.

i. CHECK—Both traces are displayed simultaneously.

j. Disconnect the test equipment from the 336.

TRIGGERS

Equipment Required (see Table 4-1)

Leveled Sine-Wave Generator (Item 1)
Function Generator (Item 4)
50 Ω BNC Coaxial Cable (Item 11)
50 Ω BNC Termination (Item 13)
10X Attenuator (Item 14)
2X Attenuator (Item 15)
Alignment Tool (Item 17)
TV Signal Generator (Item 19)
Dual-input Coupler (Item 20)

See ***ADJUSTMENT LOCATIONS*** *at the rear of this manual for location of adjustments and test points.*

NOTE

If starting the adjustment procedure at this point, prior to applying power to the 336, verify that the Nominal Voltage Selector is set to the correct power source voltage. Connect the 336 to an appropriate power source via an isolation transformer. Apply power to the test equipment and 336. Make the initial 336 control settings as soon as the Power-on diagnostics routine has completed, and allow a 20-minute warmup period before commencing the adjustments and checks for maximum accuracy.

INITIAL CONTROL SETTINGS

Control settings not listed do not affect the initial procedure and will be set when necessary.

Set:	
INTENSITY	Visible display
FOCUS	Best defined display
VERT MODE	CH 1
CH 1 VOLTS/DIV	0.5 V
VOLTS/DIV VAR (both)	CAL (in detent)
AC-GND-DC (both)	DC
CH 2 INVERT	Noninverted (no down arrow displayed with CH 2 VERT MODE)
Vertical POSITION (both)	Midrange
DISPLAY MODE	
NON STORE	ON (LED illuminated)
STORE	OFF
VIEW	OFF
Horizontal Display	A (knob in)
Horizontal POSITION	Midrange
SEC/DIV	20 μs
X10 MAG	OFF (indicator unlighted)
VAR SWP/HOLDOFF	CAL/NORM (in detent)
TRIGGER	
MODE	AUTO
SOURCE	CH 1
COUPLING	AC
A LEVEL	For a stable display (with signal applied)
A SLOPE	+ (plus)
B MODE	Triggerable after delay
B SLOPE	+ (plus)
B LEVEL	Center of the + SLOPE
Main MENU Selections	
READOUT	ON
TIME OUT	SLOW
CURSORS	OFF
HORIZ VAR	HOLDOFF
TRACE SEP	2.0 DIV

1. Adjust A and B Trigger LEVEL Centering (A2R258 and A2R251)

NOTES

Instruments with serial numbers below B300126 do not include the B Trig LEVEL Centering adjustment. For those serial number instruments, skip parts g and h of this step.

a. Connect the function generator output to the CH 1 and CH 2 input connectors via a 50 Ω coaxial cable, a 50 Ω termination, and a dual-input coupler.

b. Set the function generator for a sine-wave output at a frequency of 50 kHz.

c. Set the function generator output amplitude to obtain a 3-division vertical display.

d. Set the CH 1 VOLTS/DIV to 5 V.

e. Set the A TRIG LEVEL control to the center of the + SLOPE range.

f. ADJUST—A Level Ctrg A2R258 to obtain a stable display point.

g. Set the Horizontal Display Mode to ALT (SEC/DIV knob out).

h. ADJUST—B Level Ctrg A2R251 to obtain a stable display point.

2. Adjust A and B Trigger Sensitivity (A2R480 and A2R482)

a. Set:

CH 1 VOLTS/DIV	10 V

b. ADJUST—A Trig Sens A2R480 to obtain a stable A trigger point.

c. Set the B Trigger LEVEL control to the center of the + (plus) SLOPE.

d. ADJUST—B Trig Sens A2R482 for a stable B trigger point, then back off enough to just produce an unstable B trigger point.

e. ADJUST—A Trig Sens A2R480 to just produce an unstable A trigger point.

f. Set the Trigger MODE to NORM.

g. CHECK—The A Sweep is not triggered at any point as the A LEVEL control is rotated through its full range.

h. Set the Trigger MODE to AUTO.

i. CHECK—The B Sweep is not triggered at any point as the B LEVEL control is rotated through its full range (not in RUNS AFTER DELAY).

j. Set the Horizontal Display to A (push SEC/DIV knob in).

3. Check A and B Internal Trigger Sensitivity

a. Set:

VERT MODE	DUAL TRACE
A SEC/DIV	10 ms
VOLTS/DIV (both)	0.5 V
TRIGGER COUPLING	AC

b. Set the generator output for a sine-wave output of 30 Hz and set the output amplitude for a 3-division display amplitude.

c. Set both VOLTS/DIV settings to 5 V to obtain a signal amplitude of 0.3 division on both channels.

d. CHECK—A and B Trigger Sensitivity.

1. Set the Trigger MODE to NORM.
2. Verify that a stable A Sweep display can be obtained using the A TRIG LEVEL control on both + and − SLOPE.
3. Set the Trigger SOURCE to CH 2 and repeat subpart 2.
4. Set the Horizontal Display Mode to ALT (pull SEC/DIV knob).
5. Verify that a stable B Sweep display (also an intensified zone appears on the A trace) can be obtained using the B TRIG LEVEL control on both + and − SLOPE. (Adjust the A TRIG LEVEL control as necessary to maintain a stable A Sweep display.)
6. Set the Trigger SOURCE to CH 1 and repeat subpart 5.
7. Set:

Horizontal Display Mode	A (push SEC/DIV knob in)

8. For 50 kHz, 10 MHz, and 50 MHz triggering, set the TRIGGER COUPLING to DC and repeat subparts 2 through 7.

e. Set the function generator for an output frequency of 10 Hz and set the Trigger COUPLING to DC.

f. CHECK—Repeat part d, subparts 2 through 5.

g. Set:

A SEC/DIV	10 μs
VOLTS/DIV (both)	0.5 V
Horizontal Display	
MODE	A (push SEC/DIV knob in)
TRIGGER	
MODE	AUTO
COUPLING	AC
SOURCE	CH 1

h. Disconnect the coaxial cable from the function generator and connect it to the leveled sine-wave generator output.

i. Set the sine-wave generator frequency to 50 kHz and adjust the output amplitude for signal displays 3 divisions in amplitude.

j. Set both VOLTS/DIV settings to 5 V.

k. CHECK—Repeat part d.

l. Increase the generator frequency to 10 MHz, set the A SEC/DIV setting to 0.1 μs, and switch Trigger COUPLING to AC.

m. CHECK—Repeat part d, subparts 2 through 8.

n. Set:

VOLTS/DIV (both)	0.5 V
TRIGGER	
COUPLING	AC
MODE	AUTO

o. Increase the generator frequency to 50 MHz and set the output amplitude for signal displays 3 divisions in amplitude.

p. Set VOLTS/DIV settings to 1 V.

q. CHECK—Repeat part d.

4. Check HF REJ and LF REJ COUPLING

a. Set:

TRIGGER	
COUPLING	HF REJ
MODE	NORM

b. CHECK—A stable A Sweep display cannot be obtained at any A TRIG LEVEL setting on either + or − SLOPE.

c. Set:

VOLTS/DIV (both)	0.5 V
TRIGGER	
COUPLING	LF REJ

d. Set the leveled sine-wave generator output for 3-division display amplitudes.

e. Set the VOLTS/DIV settings to 1 V.

f. CHECK—A stable A Sweep display can be obtained using the A TRIG LEVEL control on both + and − SLOPE.

g. Set the Trigger SOURCE to CH 2 and repeat part f.

h. Set the VOLTS/DIV settings to 0.5 V.

i. Set the sine-wave generator output for a 5-division display at 10 MHz.

j. Set the VOLTS/DIV settings to 5 V.

k. CHECK—Repeat parts f and g.

l. Set the sine-wave generator to 50 kHz.

m. Set the A SEC/DIV setting to 10 μs.

n. CHECK—Repeat parts f and g.

o. Set the A Trigger COUPLING to HF REJ.

p. CHECK—Repeat part f and g.

q. Set:

VOLTS/DIV (both)	0.5 V
A SEC/DIV	20 ms

r. Disconnect the coaxial cable from the leveled sine-wave generator output and connect it to the function generator output.

s. Set the function generator for sine-wave output and adjust the amplitude control for 5-division displays.

t. Set the VOLTS/DIV settings to 5 V.

u. CHECK—Repeat parts f and g.

v. Set the Trigger COUPLING to LF REJ.

w. CHECK—Repeat part b.

x. Disconnect the test equipment from the 336.

5. Check EXT and EXT/10 Trigger Sensitivity

a. Set:

VERT MODE	CH 2
CH 2 VOLTS/DIV	10 mV
TRIGGER	
COUPLING	AC
SOURCE	EXT

b. Connect the function generator output to the CH 2 and EXT TRIG IN connectors via a 50 Ω coaxial cable, a 10X attenuator, a 2X attenuator, a 50 Ω termination, and a dual-input coupler.

c. Set the function generator for a 7-division display amplitude (70 mV peak-to-peak).

d. CHECK—A stable A Sweep display can be obtained using the A TRIG LEVEL control on both + and − SLOPE with both AC and DC Trigger COUPLING.

e. Set:

CH 2 VOLTS/DIV	20 mV
TRIGGER	
COUPLING	HF REJ

f. Remove the 2X attenuator from the test setup.

g. CHECK—A stable A Sweep Display can be obtained using the A TRIG LEVEL control on both + and − SLOPE.

h. Set the Trigger COUPLING to LF REJ

i. CHECK—A stable A Sweep Display cannot be obtained using the A TRIG LEVEL control on either + or − SLOPE.

j. Set:

TRIGGER	
SOURCE	EXT/10
COUPLING	HF REJ
CH 2 VOLTS/DIV	0.2 V

k. Remove the 10X attenuator from the test setup.

l. CHECK—Repeat part g.

m. Add the 2X attenuator back to the test setup between the coaxial cable and the 50 Ω termination.

n. CHECK—Repeat part d.

o. Move the coaxial cable from the function generator output connector to the leveled sine-wave generator output connector.

p. Set:

CH 2 VOLTS/DIV	0.1 V
A SEC/DIV	10 μs.

q. Set the sine-wave generator for a 7-division signal amplitude at 50 kHz.

r. CHECK—Repeat part d.

s. Set:

VOLTS/DIV	0.2 V
TRIGGER	
COUPLING	HF REJ

t. Remove the 2X attenuator from the test setup.

u. CHECK-Repeat part g.

v. Set:

TRIGGER	
SOURCE	EXT
CH 2 VOLTS/DIV	20 mV

w. Add the 10X attenuator to the test setup.

x. CHECK—A stable A Sweep display can be obtained using the A TRIG LEVEL control in both + and − SLOPE with both HF REJ and LF REJ COUPLING.

y. Set:

TRIGGER	
COUPLING	HF REJ
A SEC/DIV	0.1 μs

z. Increase the sine-wave generator to 10 MHz.

aa. CHECK—Repeat part i.

ab. Set the Trigger COUPLING to LF REJ.

ac. CHECK—Repeat part g.

ad. Insert the 2X attenuator back into the test setup.

ae. CHECK—Repeat part d.

af Set:

CH 2 VOLTS/DIV	0.1 V
TRIGGER	
SOURCE	EXT/10

ag. Remove the 10X attenuator from the test setup.

ah. CHECK—Repeat part d.

ai Set:

TRIGGER	
COUPLING	LF REJ
CH 2 VOLTS/DIV	0.2 V

aj. Remove the 2X attenuator from the test setup.

ak. CHECK—Repeat part g.

al. Increase the sine-wave generator frequency to 50 MHz.

am. Set:

TRIGGER	
SOURCE	EXT
CH 2 VOLTS/DIV	0.1 V

an. Set the sine-wave generator output for a 7-division display amplitude.

ao. CHECK—Repeat part g.

ap. Insert the 2X attenuator back the test setup.

aq. CHECK—Repeat part d.

ar. Disconnect the test equipment from the 336.

6. Check LINE Trigger

a. Set:

VERT MODE	CH 1
CH 1 VOLTS/DIV	5 mV (50 mV with 10X probe)
A SEC/DIV	5 ms
TRIGGER	
SOURCE	LINE
COUPLING	AC
MODE	AUTO

b. Connect a 10X probe to the CH 1 input connector.

c. Place the 10X probe tip next to the ac-power cord.

d. Adjust the spacing and/or orientation of the probe tip with respect to the ac-power cord to obtain about a 4- to 5-division display amplitude. (A short length of wire wrapped around the power cord may be used as a pickup loop, if necessary. Connect the probe tip only to one end of the wire.)

e. CHECK—A stable line frequency display can be obtained by using the A TRIG LEVEL control in both + and − SLOPE.

f. Disconnect the 10X probe from the 336.

7. Check Trigger MODE

a. Set:

CH 1 VOLTS/DIV	0.5 V
A SEC/DIV	0.5 ms

b. Connect the output of the function generator to the CH 1 input connector via a 50 Ω coaxial cable and a 50 Ω termination.

c. Set the function generator for a sine-wave output at 1 kHz and set the generator amplitude control for a 4-division display amplitude.

d. CHECK—Display remains stably triggered as the A TRIG LEVEL control is rotated through its range on both + and − SLOPE. (At the transition point between + and − SLOPE, the display may become unstable.)

e. Set:

TRIGGER	
MODE	NORM

f. Adjust the A TRIG LEVEL control for a stable display.

g. Set the CH 1 AC-GND-DC switch to GND.

h. CHECK—The trace is not visible on the crt.

i. Set:

TRIGGER	
MODE	SINGLE

j. CHECK—RESET button is lighted.

k. Set the CH 1 AC-GND-DC switch to DC.

l. CHECK—A single sweep occurs, and the RESET button is unlighted. Verify that a single sweep occurs with each press of the RESET button. (Adjust INTENSITY control to increase the display intensity, if necessary.)

m. Disconnect the test equipment from the 336.

8. Check External Trigger LEVEL Range

a. Set:

CH 1 VOLTS/DIV	0.5 V
TRIGGER	
SOURCE	EXT
MODE	AUTO
COUPLING	DC

b. Connect the function generator output to the CH 1 and EXT TRIG IN connectors via a 50 Ω coaxial cable, a 50 Ω termination, and a dual-input coupler.

c. Set the function generator output amplitude for a 3-division display. Use the CH 1 Vertical POSITION control to center the display vertically.

d. Set the Trigger MODE to NORM.

e. CHECK—Display remains triggered as the TRIG LEVEL control is rotated to change the trigger point by ±1 V (start of sweep up 1 division and down 1 division from the center horizontal graticule line).

f. Repeat part e for the − SLOPE side of the TRIG LEVEL control.

g. Set:

Horizontal Display Mode	ALT (pull SEC/DIV knob to out position)
TRACE SEP	2.0 div
A TRIGGER	
LEVEL	For a stable A Sweep
SLOPE	+ (plus)

h. CHECK—Repeat parts e and f for the B(DLY'D) TRIG LEVEL control.

i. Remove the 50 Ω termination from the test setup.

j. Set:

CH 1 VOLTS/DIV	5 V
Horizontal Display Mode	A (SEC/DIV knob in)
TRIGGER	
SOURCE	EXT/10

k. Rotate the amplitude control on the function generator to full amplitude (10 V p-p open circuit). Pull the DC Offset knob of the function generator to the out position and rotate it fully counterclockwise (ccw).

l. Use the CH 1 Vertical POSITION control to align the positive peaks of the sine wave with the center horizontal graticule line.

m. CHECK—Display remains triggered as the TRIG LEVEL control is rotated to change the trigger point from −10 V to 0 V (start of trace changes from 2 divisions below center graticule to center graticule).

n. Rotate the DC Offset knob on the function generator to fully clockwise (cw).

o. CHECK—Display remains triggered as the TRIG LEVEL control is rotated to change the trigger point from 0 V to 10 V (start of trace change from center graticule to 2 divisions above center graticule).

p. CHECK—Repeat part o for the − SLOPE.

q. Rotate the DC Offset knob to fully ccw.

r. CHECK—Repeat part m for the − SLOPE.

s. Set:

Horizontal Display Mode	ALT (SEC/DIV knob to the out position)
A TRIGGER	
LEVEL	For a stable A Sweep
SLOPE	+ (plus)

t. CHECK—Repeats parts m through r for the B (DLY'D) TRIG LEVEL control.

u. Disconnect the test equipment from the 336.

9. Check TV Trigger Sensitivity

a. Set:

VERT MODE	CH 1
CH 1 VOLTS/DIV	0.2 V
SEC/DIV	20 μs
TRIGGER	
A MODE	NORM
SOURCE	CH 1
COUPLING	TV SYNC
B MODE	Triggerable After Delay

b. Connect a source of TV sync-negative composite video to the CH 1 and EXT TRIG IN connectors via a 50 Ω coaxial cable and a dual-input coupler. (Use a 50 Ω termination depending on the generator output impedance.)

c. Adjust the generator output amplitude and use attenuators as necessary to obtain a 1.5-division display amplitude of the horizontal sync pulses.

d. CHECK—That stable TV line triggering can be obtained by adjusting the A TRIG LEVEL control (disregard field pulses moving through the display).

e. Switch the SEC/DIV setting to 5 ms.

f. CHECK—That stable TV field triggering can be obtained by adjusting the A TRIG LEVEL control.

g. Remove attenuators and adjust the generator output amplitude to obtain a 7.5-division display amplitude of the horizontal sync pulses.

h. Set the CH 1 VOLTS/DIV setting to 0.1 V to obtain a 15-division signal amplitude.

i. CHECK—TV field display remains stably triggered.

j. Set the Trigger SOURCE to EXT.

k. CHECK—TV field display remains stably triggered.

l. Set CH 1 VOLTS/DIV setting to 0.2 V.

m. Insert attenuators and adjust the generator output amplitude as necessary for a 2-division display amplitude.

n. Set:

SEC/DIV	0.2 ms
TRIGGER	
A SLOPE	− (minus)
A LEVEL	For a stable display

o. CHECK—Display switches to line sync when the SEC/DIV control is set to 0.1 ms. (Disregard the field pulses running through the display; the VAR HOLDOFF control may be adjusted to reduce or eliminate the vertical sync field pulses from the display).

p. Set:

A SEC/DIV	0.2 ms
Horizontal Display Mode	ALT (pull SEC/DIV knob out)
B SEC/DIV	20 μs

q. CHECK—A stable B Sweep line pulse display can be obtained by adjusting the B TRIG LEVEL control and that the A Sweep display remains stably triggered on the field pulse.

r. Disconnect the test equipment from the 336.

10. Check Trigger Jitter

a. Set:

CH 1 VOLTS/DIV	0.1 V
A SEC/DIV	0.1 ms
Horizontal Display Mode	A (SEC/DIV knob in)
DISPLAY MODE	STORE
TRIGGER	
MODE	NORM
COUPLING	AC
SOURCE	CH 1
SLOPE	+ (plus)
LEVEL	For a triggered display with signal applied

b. Connect the fast-rise + output of the calibration generator to the CH 1 input connector via a 50 Ω coaxial cable and a 50 Ω termination.

c. Set the calibration generator frequency for a 1 kHz signal and adjust the output amplitude control to obtain about a 5-division display amplitude.

d. Use the Horizontal POSITION control to move the rising edge of the waveform to the center vertical graticule line.

e. Press in the X10 MAG button and use the Horizontal POSITION control to align the rising edge of the magnified display with the center vertical graticule line.

f. CHECK—Jitter of the rising edge of the waveform is approximately ±0.1 division horizontally.

g. Set:

DISPLAY MODE	NON STORE
A SEC/DIV	10 ns (with X10 MAG on)

h. Disconnect the coaxial cable from the calibration generator and connect it to the output of the leveled sine-wave generator.

i. Set the sine-wave generator for an output frequency of 50 MHz and adjust the amplitude controls for about a 5-division display amplitude.

j. Use the Horizontal POSITION control to align the rising edge of one of the sine-wave cycles with the center vertical graticule line.

k. CHECK—Jitter on the rising edge of the waveform is ±0.1 division or less.

l. Disconnect the test equipment from the 336.

HORIZONTAL

Equipment Required (see Table 4-1)

- Time Mark Generator (Item 3)
- Test Oscilloscope (Item 6)
- 50 Ω BNC Coaxial Cable (Item 11)
- 50 Ω Precision BNC Coaxial Cable (Item 12)
- 50 Ω BNC Termination (Item 13)
- Alignment Tool (Item 17)

See **ADJUSTMENT LOCATIONS** *at the rear of this manual for location of adjustments and test points.*

NOTE

If starting the adjustment procedure at this point, prior to applying power to the 336, verify that the Nominal Voltage Selector is set to the correct power source voltage. Connect the 336 to an appropriate power source via an isolation transformer and apply power to the test equipment and 336. Make the initial 336 control settings as soon as the Power-on diagnostics routine has completed, and allow a 20-minute warmup period before commencing the adjustments and checks for maximum accuracy.

INITIAL CONTROL SETTINGS

Control settings not listed do not affect the initial procedure and will be set when necessary.

Set:	
INTENSITY	Visible display
FOCUS	Best defined display
VERT MODE	CH 1
CH 1 VOLTS/DIV	0.5 V
VOLTS/DIV VAR (both)	CAL (in detent)
CH 2 INVERT	Noninverted (no down arrow displayed with CH 2 VERT MODE)
AC-GND-DC (both)	DC
Vertical POSITION (both)	Midrange
DISPLAY MODE	
NON STORE	ON (LED lighted)
STORE	OFF
VIEW	OFF
Horizontal Display	A (SEC/DIV knob in)
Horizontal POSITION	Midrange
SEC/DIV	1 ms
X10 MAG	OFF
VAR SWP/HOLDOFF	CAL/NORM (in detent)
TRIGGER	
MODE	AUTO
SOURCE	CH 1
COUPLING	AC
A LEVEL	For a stable display (with signal applied)
A SLOPE	+ (plus)
B LEVEL	RUNS AFTER DELAY
Main MENU Selections	
READOUT	ON
TIME OUT	SLOW
STORE MODE	NORMAL
CURSORS	OFF
HORIZ VAR	SEC/DIV
TRACE SEP	2.0 DIV

1. Adjust X10 MAG Registration (A12R200)

a. Connect the output of the time-mark generator to the CH 1 input connector via a 50 Ω BNC coaxial cable and a 50 Ω termination.

b. Set the generator for 5 ms time markers.

c. Use the Horizontal POSITION control to align the middle time marker with the center vertical graticule line.

d. Set X10 MAG on.

e. Repeat part c.

f. Set X10 MAG off.

g. ADJUST—Mag Registration A12R200 to position the middle time marker to the center horizontal graticule line.

h. Repeat parts d through g until no horizontal shift of the time marker is observed between X10 MAG on and off.

2. Adjust READOUT Horizontal Gain and Position (A4R284 and A4R280)

a. Press MENU ON/OFF and MENU LAST buttons at the same time and release together to enter the diagnostics mode.

b. Press Trigger Mode RESET button, then press the MENU 2 button to display a full screen of plus symbols (+).

c. If the display extends horizontally beyond the graticule edges, set Readout Gain A4R284 fully counterclockwise (minimium gain); otherwise, skip to part d.

d. ADJUST—Readout Horizontal Position A4R280 to center the display within the graticule area.

e. ADJUST—Readout Gain A4R284 for a full-screen display (left and right end of the display on the first and last vertical graticule line respectively).

f. Press MENU ON/OFF and MENU LAST buttons at the same time and release together to exit the diagnostics mode.

g. Set the READOUT OFF (press MENU ON/OFF, MENU 4, MENU 1, MENU 2).

h. CHECK—VOLTS/DIV and SEC/DIV Readouts turn off.

i. Set the READOUT ON (press MENU LAST, if menu display has timed out, then MENU 1).

3. Adjust A Sweep, B Sweep, and STORE Mode Display Timing

a. Set the time-mark generator for 1 ms time markers.

b. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd veritical graticule line.

c. ADJUST—A 1 ms Timing A3R424 for exactly 1 time marker per division over the center 8 divisions.

d. Set:

A SEC/DIV	2 ms
B SEC/DIV	1 ms
Horizontal Display Mode	B (push SEC/DIV knob in after setting sweep speeds)
B TRIGGER	
MODE	Triggerable After Delay
LEVEL	For a stable B Sweep display
DLY TIME	Minimum delay (press left DLY TIME button until delay time readout stops changing)

e. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

f. ADJUST—B 1 ms Timing A3R524 for exactly 1 time marker per division over the center 8 divisions.

g. Set:

Horizontal Display Mode	ALT (SEC/DIV knob out)
A SEC/DIV	0.2 μs
B SEC/DIV	0.1 μs

h. Set the time mark generator for 0.1 μs time markers.

i. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

j. ADJUST—B 100 ns Timing A3C554 for exactly 1 time marker per division over the center 8 divisions.

k. Set:

Horizontal Display Mode	A (SEC/DIV knob back to 0.2 μs)
A SEC/DIV	0.1 μs

l. ADJUST—A 100 ns Timing A3C454 for exactly 1 time marker per division over the center 8 divisions.

m. Set:

A SEC/DIV	1 ms
DISPLAY MODE	STORE

n. Set the time-mark generator for 1 ms time markers.

o. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd graticule line.

p. ADJUST—Storage Sweep Length A6R54 for exactly 1 time marker per division over the center 8 divisions.

q. Set A SEC/DIV to 1 μs.

r. Set the generator for 1 μs time markers.

s. ADJUST—Equivalent Mode Horizontal Gain A5R732 for exactly 1 time marker per division over the center 8 divisions.

t. Disconnect test equipment from the 336.

4. Adjust Storage X Gain (A6R370)

a. Connect the standard-amplitude output of the calibration generator to the CH 1 OR X input via a 50 Ω Precision coaxial cable.

b. Set the calibration generator output for a 2 V standard-amplitude signal.

c. Set:

SEC/DIV	1 ms
VERT MODE	DUAL TRACE
Horizontal POSITION	Midrange

d. Set the Storage Display to X-Y (press MENU ON/OFF, MENU 1, MENU 3, MENU 2).

e. Use the CH 1 Vertical POSITION control to align the end of the trace with a convenient vertical graticule line as a measurement reference point.

f. ADJUST—Storage X Gain A6R370 for a 4-division horizontal display.

g. Set the Storage Display back to TIME (press MENU LAST, MENU 1).

5. Adjust NON STORE X-Axis Gain and Position (A4R220 and A1R217)

a. Set:

CH 1 VOLTS/DIV	5 mV
DISPLAY MODE	NON STORE
SEC/DIV	X-Y (SEC/DIV knob ccw to X-Y)

b. Set the calibration generator for a 20 mV standard-amplitude signal.

c. ADJUST—X-Y Gain A4R220 for a 4-division horizontal display. (Use the CH 1 Vertical POSITION control to align the display horizontally with the graticule lines for making the measurement.)

d. Set the CH 1 AC-GND-DC switch to GND.

e. Set the CH 1 Vertical POSITION control to midrange (white index dot at the top of the knob).

f. ADJUST—X-Y Pos A1R217 to align the dot with the center vertical graticule line.

g. Disconnect the test equipment from the 336.

6. Adjust X10 MAG Gain and Linearity (A4R266 and A4R298)

a. Set:

VERT MODE	CH 1
CH 1 VOLTS/DIV	0.5 V
CH 1 AC-GND-DC	DC
DISPLAY MODE	NON STORE
A SEC/DIV	1 ms (with X10 MAG off)
X10 MAG	ON

b. Connect the output of the time-mark generator to the CH 1 input via a 50 Ω coaxial cable and a 50 Ω termination.

c. Set the generator output for 0.1 ms time markers.

d. Use the Horizontal POSITION control to align one of the time markers with the center vertical graticule line.

e. ADJUST—X10 Gain A4R266 for exactly 1 time marker per division over the center 8 divisions.

f. Set SEC/DIV to 10 ns.

g. Set the generator output for 20 ns time markers.

h. ADJUST—Linear Center A4R298 for the best linearity over the center 8 divisions (1 time marker per 2 divisions).

7. Check VAR SEC/DIV Range

a. Set:

X10 MAG	Off
SEC/DIV	0.1 ms (with X10 MAG off)

b. Set the generator for 0.1 ms time markers (1 time marker per division).

c. CHECK—Number of time markers per divisions increases to at least 5 markers per 2 divisions as the VAR SWP/HOLDOFF control is rotated counterclockwise.

d. Return the VAR SWP/HOLDOFF control to the detent position (fully clockwise).

8. Adjust Delay Time Start and Stop (A4R122 and A4R128)

a. Set:

Horizontal Display Mode	ALT (SEC/DIV knob out)
B SEC/DIV	1 μs
B TRIGGER MODE	RUNS AFTER DELAY (in detent fully counter-clockwise)

b. Set the generator for 50 μs time markers.

c. Use the Horizontal POSITION control to align the start of the A Sweep trace with the first vertical graticule line.

d. Press the right DLY TIME/CURSOR button and hold it until the Delay Time position readout stops changing (dot at the right side of the trace).

e. ADJUST—Delay Stop A4R128 to position the delay time dot on the 21st time marker on the A Sweep, and continue the adjustment to align the rising edge of the time marker on the B Sweep with the start of the B Sweep trace.

f. Press the left DLY TIME/CURSOR button and hold it until the Delay Time position readout stops changing (dot at the left side of the trace).

g. ADJUST—Delay Start A4R122 to position the delay time dot on the 2nd time marker in from the left edge, and continue the adjustment to align the rising edge of the time marker on the B Sweep with the start of the B Sweep trace.

h. Repeat parts d through g until no further improvement is noted in the Delay Time Position adjustment.

9. Check Delay Time Jitter

a. Set:

A SEC/DIV	1 ms
B SEC/DIV	1 μs
Delay Time Position	Minimum delay (press left DLY TIME/CURSOR position button until delay readout stops changing)

b. Set the generator for 1 ms time markers.

c. Use the Horizontal POSITION control to align the time markers displayed on the A Sweep with the vertical graticule lines.

d. Use the DLY TIME/CURSOR position buttons to position the delay time intensified dot on the A Sweep to the 2nd time marker.

e. Push in the A SEC/DIV knob to obtain a display of the B Sweep only (adjust INTENSITY as necessary for viewing).

f. Use the DLY TIME/CURSOR position bottons to align the rising edge of the time marker with the center vertical graticule line, then press in both DLY TIME/CURSOR button to zero the delay time readout.

g. CHECK—Delay time jitter is 1 division or less horizontal movement of the rising edge of the time marker.

h. Pull the SEC/DIV knob out for ALT Horizontal Display.

i. Set the Delay Time to 8.0 ms, then press the SEC/DIV knob back in for a B Sweep display only.

NOTE

At the amount of magnification displayed by the B Sweep display, the difference between delay-time positioning resolution and delay-time readout resolution becomes a factor in determining the exact position of the time marker rising edge.

j. Set the Delay Time Position as necessary to view the rising edge of the time marker near the graticule center.

k. CHECK—Repeat part g.

10. Check VAR HOLDOFF Range

a. Set:

Horizontal Display Mode	A (SEC/DIV knob in)
A SEC/DIV	10 μs

b. Set the HORIZ VAR to HOLDOFF (press MENU ON/OFF, MENU 3, MENU 1, MENU 1). The front-panel VAR SWP/HOLDOFF control will now vary the holdoff time.

c. Turn the READOUT display off (press MENU ON/OFF, MENU 4, MENU 1, MENU 2).

d. Set the time-mark generator for 0.2 μs time markers.

e. Set the Test Oscilloscope controls:

Volts/Div	0.5 V
Sec/Div	50 μs
Vert Mode	Ch 1
Ch 1 Ac-Gnd-Dc	Ac
Trigger	
Coupling	Ac
Mode	Auto
Slope	− (minus)
Level	For a stable display
Horizontal Display Mode	A Sweep only

f. Connect the 10X probe tip from the test oscilloscope to A3TP480 (A Sweep) and connect the probe ground lead to chassis ground of the 336.

g. Use the Var Sec/Div control on the test oscilloscope to obtain a 1-division horizontal display of the A Sweep holdoff time (the flat portion at the bottom of the waveform).

h. CHECK—Holdoff time increases to 10 divisions or more as the VAR SWP/HOLDOFF control on the 336 is rotated fully counterclockwise.

i. Set the VAR HOLDOFF back to NORM (fully clockwise) and turn the READOUT back on (press MENU LAST, MENU 1).

11. Check Horizontal POSITION Range

a. Set The CH 1 AC-GND-DC switch to GND.

b. CHECK—Left and right ends of the trace can be positioned horizontally past the center vertical graticule line as the Horizontal POSITION control is rotated fully clockwise and fully counterclockwise respectively.

12. Check A and B NON STORE Timing Accuracy

a. Set:

A TRIGGER	
MODE	NORM
LEVEL	For a stable display
SLOPE	+
SEC/DIV	0.1 μs
CH 1 AC-GND-DC	DC

b. Set the time-mark generator for 0.1 μs time markers.

c. Use the CH 1 Vertical POSITION control to place the tips of the time markers at the center horizontal graticule line (for ease in determining timing from the graticule markings).

d. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line. (Maintain alignment of the 2nd time marker with the 2nd vertical graticule line when checking the timing accuracy at all sweep speeds.)

e. CHECK—Timing accuracy at the 10th graticule line is within 2% (0.2 division) and linearity between any two divisions of the center eight divisions is within 4% (0.08 division)

f. Change the SEC/DIV setting and the time-mark generator setting, one step at a time, to maintain 1 time marker per division and repeat parts d and e for each sweep speed (up to 0.2 s for the A Sweep and 50 ms for the B Sweep).

g. Set:

CH 1 VOLTS/DIV	0.5 V
SEC/DIV	0.1 μs
Horizontal Display Mode	ALT (SEC/DIV knob out)
Delay Time Position	Minimum delay (press left DLY TIME/CURSOR button until delay time readout stops changing)

h. Set the time-mark generator for 0.1 μs time markers.

i. Use the CH 1 Vertical POSITION control to align the tops of the time markers display on the B Sweep with the center horizontal graticule line (for ease in checking timing).

j. CHECK—Repeat parts d, e, and f to check the B Sweep timing accuracy and 2-division linearity.

k. Set:

Horizontal Display Mode	A (SEC/DIV knob in)
A SEC/DIV	0.1 μs (with X10 MAG off)
CH 1 VOLTS/DIV	0.5 V

l. Set the time-mark generator for 20 ns time markers and press in the X10 MAG button on the front panel of the 336 (1 time marker per 2 divisions).

m. Use the Horizontal POSITION control to align a displayed time marker with the 2nd vertical graticule line. (The first and last 50 ns of the 10 ns and 20 ns per division sweeps are excluded from the timing accuracy and 2-division linearity checks.)

n. CHECK—Magnified timing accuracy at the 10th vertical graticule line is within 3% (within 0.3 division) and linearity between any 2 divisions over the center 8 divisions is within 5% (within 0.1 division).

o. Change the SEC/DIV setting and the time-mark generator setting, one step at a time, to maintain 1 time marker per division for the remaining sweep speeds, and repeat parts m and n for each sweep speed (up to 20 ms for the A Sweep and 5 ms for the B Sweep).

p. Set the time-mark generator for 20 ns time markers.

q. Set:

SEC/DIV	10 ns (with X10 MAG on)
Horizontal Display Mode	ALT (pull SEC/DIV knob out)
A TRIGGER LEVEL	For a stable display

r. CHECK—Repeat parts m, n, and o for the B Magnified timing accuracy and 2-division linearity checks.

13. Check Storage Timing Accuracy

a. Set:

X10 MAG	Off (button unlighted)

A SEC/DIV	0.2 s (with X10 MAG off)
CH 1 AC-GND-DC	GND
Horizontal Display Mode	A (push SEC/DIV knob in)
TRIGGER MODE	AUTO
DISPLAY MODE	STORE

b. Turn on the CURSORS (press MENU ON/OFF, MENU 1, MENU 4).

c. Use the Horizontal POSITION control to align the start of the trace with the 1st vertical graticule line.

d. Use the DLY TIME/CURSOR buttons to align one cursor dot exactly with 2nd vertical graticule line.

e. Press MENU button 1 to activate the second cursor and position it to the left for a time difference readout of 1.600 s.

f. CHECK—Graticule indication of cursor difference at the 10th graticule line is accurate within 2% (0.2 division).

g. Change the SEC/DIV setting, one step at a time, and repeat part f for each sweep speed. Use the Horizontal POSITION control as necessary to keep the 1st cursor dot aligned with the 2nd vertical graticule line.

h. Set the time-mark generator for 0.1 μs time markers and set the CH 1 AC-GND-DC switch to DC.

i. Turn the CURSORS mode off (press MENU button 2).

j. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line.

k. CHECK—Equivalent-time sampling accuracy is within 2% (0.2 division) at the 10th vertical graticule line.

l. Change the SEC/DIV setting and time-mark generator setting, one step at a time, to maintain 1 time marker per division, and repeat parts j and k for A Sweep speed settings down to 50 μs per division (the end of the equivalent-time sampling region).

14. Check Delay Time Differential Accuracy

a. Set:

CH 1 VOLTS/DIV	1 V
SEC/DIV (both)	0.1 μs
DISPLAY MODE	NON STORE
Horizontal Display Mode	ALT (SEC/DIV knob out)
DLY TIME	Minimum (press left DLY TIME/CURSOR position button until readout stops changing)
TRACE SEP	2.0 DIV

b. Set the time-mark generator for 0.1 μs time markers and use the CH 1 vertical POSITION control to position the tips of the time markers displayed by the B Sweep near the center horizontal graticule line.

c. Use the Horizontal POSITION control to align the 2nd time marker on the B Sweep with a reference vertical graticule line. (The 1st time marker may not be completely visible on the B Sweep trace; therefore, at the faster A Sweep speeds the 2nd vertical graticule line makes a convenient reference line.)

d. Press both DLY TIME/CURSOR position buttons at the same time and release to zero the delay time readout. Use the Horizontal POSITION control to realign the time marker with the reference graticule line as necessary.

e. Press the right DLY TIME/CURSOR button to position the 10th time marker to the reference vertical graticule line (8-division spacing between the 2nd and 10th time markers). The correct delay for an 8-divisions spacing is given in column 3 of Table 5-3.

f. CHECK—Delay time readout is within the limits given in Table 5-3, column 4 (Delay Readout Limits).

g. Using the remaining time-mark generator and B SEC/DIV switch settings given in Table 5-3, check the 8-division delay time accuracy for each A SEC/DIV switch setting given in column 1 of the table.

NOTE

When switching the A SEC/DIV switch setting to the next slower sweep speed, use the following procedure.

1. Rotate the SEC/DIV knob ccw to obtain the next slower A SEC/DIV setting to be checked.

2. Rotate the SEC/DIV knob cw to obtain the next B SEC/DIV setting to be used.

NOTE

Some setup time for each check may be saved by alternately checking the delay from the 2nd time marker to the 10th; then, at the next slower A SEC/DIV switch setting to be checked, from the 10th time marker back to the 2nd time marker. Zero the delay-time readout and align the starting time marker with the reference graticule to start at either end of the delay.

NOTE

As indicated in Table 5-3, at the slowest A Sweep speeds the A Trigger MODE should be switched to NORM to prevent the AUTO trigger from being generated before a signal triggering event occurs. Adjust the A TRIG LEVEL control as necessary to obtain a stable display on the + SLOPE.

NOTE

At the slower A SEC/DIV settings, the A Sweep trace may be removed from the display to eliminate the flicker due to sweep switching while making the actual timing accuracy check. After setting the correct A and B SEC/DIV settings, simply press in the SEC/DIV knob to obtain the B Delayed Sweep only. After making the check, pull the SEC/DIV knob out to set the new sweep speed settings for the next check.

h. Disconnect the test equipment from the 336.

15 Check TRACE SEP Operation

a. Set:

A SEC/DIV	1 ms
B SEC/DIV	0.1 ms
TRIGGER MODE	AUTO

b. Use the CH 1 Vertical POSITION control to align the B Sweep trace with the center horizontal graticule line.

Table 5-3
Differential Timing Accuracy

Time-Mark Generator and A Sec/Div Settings	B Sec/Div Setting Delay	Eight Division Limits	Delay Readout
0.1 μs	0.1 μs	800 ns	787 ns to 813 ns
0.2 μs	0.1 μs	1.600 μs	1.574 μs to 1.626 μs
0.5 μs	0.1 μs	4.000 μs	3.935 μs to 4.065 μs
1 μs	0.1 μs	8.00 μs	7.87 μs to 8.13 μs
2 μs	0.2 μs	16.00 μs	15.74 μs to 16.26 μs
5 μs	0.5 μs	40.00 μs	39.35 μs to 40.65 μs
10 μs	1 μs	80.0 μs	78.7 μs to 81.3 μs
20 μs	2 μs	160.0 μs	157.4 μs to 162.6 μs
50 μs	5 μs	400.0 μs	393.5 μs to 406.5 μs
0.1 ms	10 μs	800 μs	787 μs to 813 μs
0.2 ms	20 μs	1.600 ms	1.574 ms to 1.626 ms
0.5 ms	50 μs	4.000 ms	3.935 ms to 4.065 ms
1 ms	0.1 ms	8.00 ms	7.87 ms to 8.13 ms
2 ms	0.2 ms	16.00 ms	15.74 ms to 16.26 ms
5 ms	0.5 ms	40.00 ms	39.35 ms to 40.65 ms
10 ms	1 ms	80.0 ms	78.7 ms to 81.3 ms
20 ms	2 ms	160.0 ms	157.4 ms to 162.6 ms
50 ms [a]	5 ms	400.0 ms	393.5 ms to 406.5 ms
0.1 s [a]	10 ms	800 ms	787 ms to 813 ms
0.2 s [a]	20 ms	1.600 s	1.574 s to 1.626 s

[a]**Set A Trigger MODE to NORM.**

c. Press MENU ON/OFF, MENU 3, then MENU 2 to obtain the TRACE SEP Menu display.

d. Press MENU button 2 to decrement the trace separation between the A Sweep and the B Delayed Sweep.

e. CHECK—Each decrement decreases the trace separation by approximately 0.5 division, and at 0.0 DIV separation, the traces are overlayed.

NOTE

The TRACE SEP Menu display times out. To recall it if it times out before you have completed the check, simply press the MENU LAST button.

EXTERNAL Z-AXIS, CALIBRATOR, CHART OUT, AND OPTION 01

Equipment Required (see Table 4-1)

- Calibration Generator (Item 2)
- Digital Multimeter (Item 5)
- Test Oscilloscope with Probes (Item 6)
- GPIB Controller for Option 01 (Item 7)
- X-Y Plotter (Item 8)
- Isolation Transformer (Item 10)
- 50 Ω Precision BNC Coaxial Cable (Item 12)
- Dual-input Coupler (Item 20)
- Shorting Plug (Item 21)

See **ADJUSTMENT LOCATIONS** *at the rear of this manual for location of adjustments and test points.*

NOTE

If starting the adjustment procedure at this point, prior to application of power to the instrument, verify that the Nominal Voltage Selector is set for the correct ac source voltage. Connect the 336 to an appropriate power source via an isolation transformer. Apply power to the instrument and test equipment. Make the initial control settings upon completion of the Power-on diagnostics routine, and allow a 20-minute warmup period before commencing the adjustments and checks for maximum accuracy.

INITIAL CONTROL SETTINGS

Control settings not listed do not affect the initial procedure and will be set when needed.

Set:

INTENSITY	Visible display
FOCUS	Best defined display
VERT MODE	CH 1
CH 1 VOLTS/DIV	1 V
AC-GND-DC (both)	AC
Vertical POSITION	Midrange
DISPLAY MODE	
NON STORE	On (LED illuminated)
STORE	Off
VIEW	Off
Horizontal Position	Midrange
Horizontal Display Mode	A (SEC/DIV knob in)
SEC/DIV	0.5 ms
VAR SWP/HOLDOFF	CAL/NORM (in detent)
TRIGGER	
MODE	AUTO
SOURCE	CH 1
COUPLING	AC
A SLOPE	+ (plus)
A LEVEL	For a stable display with signal applied
Main MENU Selections	
READOUT	ON
TIMEOUT	SLOW
STORE MODE	NORMAL

1. Check External Z-Axis Input (NON STORE Mode only)

a. Connect the output of the calibration generator to the CH 1 and EXT Z-AXIS IN input connectors via a 50 Ω BNC coaxial cable and a dual-input coupler.

b. Set the calibration generator for a 5 V standard-amplitude signal output.

c. CHECK—Top half of signal is blanked, and blanking starts at approximately 3 V (3 divisions from the negative peak).

d. Disconnect the test equipment from the 336.

2. Adjust/Check Calibrator Output (A1R992)

a. Install a shorting plug across A1P982.

b. Set the DMM to measure on the 2 V DC range.

c. Connect the LO lead (minus) of the DMM to chassis ground on the 336 and connect the HI lead (plus) to the CAL OUT connector.

d. ADJUST—Cal Volts Adjust (A1R992) for a DMM reading of .300 V.

e. Remove the shorting plug from A1P982.

f. Set the test oscilloscope for a Volts/Div of 0.1 V (with 10X probe attached) and a Sec/Div of 1 ms. (The 336 may be used as the test oscilloscope.)

g. Connect the probe ground lead to chassis ground on the 336 and connect the probe tip to the CAL OUT connector.

h. CHECK—Calibrator frequency is approximately 1 kHz.

i. Disconnect the test equipment from the 336.

3. Check CHART OUT Operation

a. Set:

CH 1 VOLTS/DIV	1 V
SEC/DIV	0.5 ms
DISPLAY MODE	
NON STORE	Off
STORE	On
VIEW	Off

b. Connect the output of the function generator to the CH 1 input connector via a 50 Ω cable and a 50 Ω termination.

c. Set the function generator for a 1 kHz sine-wave signal and adjust the output amplitude for a 5-division display.

d. Press the ENTER button to store the displayed waveform.

e. Set the DISPLAY MODE to VIEW.

f. Connect the appropriate cables of the X-Y Plotter to the X, Y, and SIG GND connectors on the 336 right side panel.

g. Select the CHART Menu (use the Menu diagram in the front-cover to determine the selection path).

h. Press MENU button 3 to obtain the X-Y Plotter calibration voltage at the X and Y output connectors and apply power to the X-Y Plotter.

i. Adjust the X-Y Plotter sensitivity to calibrate the plot to the 336 crt graticule. Successive presses of the CAL button (MENU 3) switch the calibration voltages between full upper right and full lower left corner deflection of the 336 crt graticule. (Refer to the X-Y Plotter Operator's Manual for its operation.)

j. When the X-Y Plotter is calibrated, lift the plotting pen and install a new graph paper (if desired).

k. With the plot pen still up, press MENU button 1 (FAST START) to commence the plot. When the pen reaches the starting point, lower it to draw the waveform. At the end of the plot, lift the pen. (Approximately 7 seconds is allowed for all pen lifting and pen lowering movements.)

l. CHECK—The waveform plotted corresponds to the waveform displayed by the 336.

m. Disconnect the X-Y Plotter and test equipment from the 336.

4. Check GPIB (Option 01)

a. Turn off the 336.

b. Connect the GPIB cable from the controller to the 336 GPIB connector.

c. Connect the function generator output to the CH 1 and CH 2 input connectors via a 50 Ω coaxial cable, a 50 Ω termination, and a dual-input coupler.

d. Apply power to the 336 and set the front-panel controls as follows:

VERT MODE	DUAL TRACE
VOLTS/DIV (both)	2 V
DISPLAY MODE	STORE
Main MENU Selections	
DATA OUT	GPIB

e. Adjust the function generator output to obtain 2-division display amplitudes on the CH 1 and CH 2 trace. Use the Vertical POSITION control to place the display at convenient locations within the graticule area.

f. Use the INCR-DECR buttons (MENU 1 and MENU 2) to set the GPIB My Talk Address (mta) and note the address chosen for later use. (Do not set the address to TALK ONLY.)

g. Start the GPIB test program running in the controller (see "Options," Section 7 for sample program listings).

h. Enter the Talk Address of the 336.

i. CHECK—Power on SRQ (decimal 65) was issued.

j. Request a waveform plot by pressing MENU button 3.

k. CHECK—Transmit request SRQ (decimal 195) is issued and waveforms plotted correspond to the waveforms displayed on the 336.

l. Turn off the 336 and disconnect the GPIB cable.

5. Check Extended Memory and Battery Backup

a. Apply power to the 336.

b. Set:

VERT MODE	DUAL TRACE
VOLTS/DIV (both)	2 V
SEC/DIV	0.5 ms
CURSORS	On

c. Use the following procedure to store waveforms in all the VIEW memory stack locations:

1. Press the ENTER push button to store the display in the current memory stack location.
2. Press VIEW to obtain the VIEW menu display.
3. Press MENU button 1 (INCR) to increase the stack location number by 1.
4. Select STORE Display Mode again and press ENTER to store the display in the new stack location.
5. Continue subparts 2 through 4 until all VIEW memory stack locations are filled.

d. Leave VIEW Display Mode selected and turn off the 336.

e. Wait several minutes and reapply power to the 336.

f. CHECK—Front-panel controls are set as in part b and VIEW Display Mode is on.

g. Press the VIEW button twice to obtain the VIEW Menu and use the INCR button (MENU 1) to scroll through the entire memory stack.

h. CHECK—That the waveforms stored in VIEW memory in part c have been retained.

i. Turn off the 336.

j. Press A8S130 to clear the memory.

k. Reapply power to the 336.

l. CHECK—Front panel settings are as follows:

VERT MODE	CH 1
VOLTS/DIV	50 mV
DISPLAY MODE	NON STORE
SEC/DIV	2 ms
TRIGGER	
MODE	AUTO
SOURCE	CH 1
COUPLING	AC

m. Disconnect the test equipment from the 336.

MAINTENANCE

INTRODUCTION

This section of the manual contains information for conducting preventive maintenance, troubleshooting, and corrective maintenance on the 336 Oscilloscope. Circuit board removal procedures are included in the corrective maintenance part of this section.

STATIC-SENSITIVE COMPONENTS

The following precautions are applicable when performing any maintenance involving internal access to the instrument.

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. Table 6-1 lists the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

When performing maintenance, observe the following precautions to avoid component damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers or on a metal rail. Label any package that contains static-sensitive components or assemblies.

3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these components. Servicing static-sensitive components or assemblies should be performed only at a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by their bodies, never by their leads.

Table 6-1
RELATIVE SUSCEPTIBILITY TO STATIC DISCHARGE DAMAGE

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[a] **Voltage equivalent for levels: (Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.)**

1 = 100 to 500 V 4 = 500 V 7 = 400 to 1000 V (est.)
2 = 200 to 500 V 5 = 400 to 600 V 8 = 900 V
3 = 250 V 6 = 600 to 800 V 9 = 1200 V

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only approved antistatic, vacuum-type desoldering tools for component removal.

PREVENTIVE MAINTENANCE

INTRODUCTION

Preventive maintenance consists of cleaning, visual inspection, and checking instrument performance. When accomplished regularly, it may prevent instrument malfunction and enhance instrument reliability. The severity of the environment in which the instrument is used determines the required frequency of maintenance.

An appropriate time to accomplish preventive maintenance is just before instrument adjustment.

GENERAL CARE

The cabinet minimizes accumulation of dust inside the instrument and should normally be in place when operating the 336. The front cover supplied with the instrument provides both dust and damage protection for the front panel and crt, and it should be on whenever the instrument is stored or is being transported.

INSPECTION AND CLEANING

The 336 should be visually inspected and cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket, preventing efficient heat dissipation. It also provides an electrical conduction path that could result in instrument failure, especially under high-humidity conditions.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use a nonresidue-type cleaner, preferably isopropyl alcohol or a solution of 1% mild detergent with 99% water. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

Exterior

INSPECTION. Inspect the external portions of the instrument for damage, wear, and missing parts; use Table 6-2 as a guide. Instruments that appear to have been dropped or otherwise abused should be checked thoroughly to verify correct operation and performance. Deficiencies found that could cause personal injury or could lead to further damage to the instrument should be repaired immediately.

CAUTION

To prevent getting moisture inside the instrument during external cleaning, use only enough liquid to dampen the cloth or applicator.

CLEANING. Loose dust on the outside of the instrument can be removed with a soft cloth or small soft-bristle brush. The brush is particularly useful for dislodging dirt on and around the controls and connectors. Dirt that remains can be removed with a soft cloth dampened in a mild detergent-and-water solution. Do not use abrasive cleaners.

Two plastic light filters, one blue and one clear, are provided with the oscilloscope. Clean the light filters and the crt face with a soft lint-free cloth dampened with either isopropyl alcohol or a mild detergent-and-water solution.

Interior

To gain access to internal portions of the instrument for inspection and cleaning, refer to the "Removal and Replacement Instructions" in the "Corrective Maintenance" part of this section.

INSPECTION. Inspect the internal portions of the 336 for damage and wear, using Table 6-3 as a guide. Deficiencies found should be repaired immediately. The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; therefore, it is important that the cause of overheating be corrected to prevent recurrence of the damage.

If any electrical component is replaced, conduct a Performance Check for the affected circuit and for other closely related circuits (see Section 4). If repair or replacement work is done on any of the power supplies, conduct a complete Performance Check and, if so indicated, an instrument readjustment (see Sections 4 and 5).

CAUTION

To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the instrument.

Table 6-2
External Inspection Check List

Item	Inspect For	Repair Action
Cabinet, Front Panel, and Cover	Cracks, scratches, deformations, damaged hardware or gaskets.	Touch up paint scratches and replace defective components.
Front-panel Controls	Missing, damaged, or loose knobs, buttons, and controls.	Repair or replace missing or defective items.
Connectors	Broken shells, cracked insulation, and deformed contacts. Dirt in connectors.	Replace defective parts. Clean or wash out dirt.
Carrying Handle	Correct operation.	Replace defective parts.
Accessories	Missing items or parts of items, bent pins, broken or frayed cables, and damaged connectors.	Replace damaged or missing items, frayed cables, and defective parts.

Table 6-3
Internal Inspection Checklist

Item	Inspect For	Repair Action
Circuit Boards	Loose, broken, or corroded solder connections. Burned circuit boards. Burned, broken, or cracked circuit-run plating.	Clean solder corrosion with an eraser and flush with isopropyl alcohol. Resolder defective connections. Determine cause of burned items and repair. Repair defective circuit runs.
Resistors	Burned, cracked, broken, blistered.	Replace defective resistors. Check for cause of burned component and repair as necessary.
Solder Connections	Cold solder or rosin joints.	Resolder joint and clean with isopropyl alcohol.
Capacitors	Damaged or leaking cases. Corroded solder on leads or terminals.	Replace defective capacitors. Clean solder connections and flush with isopropyl alcohol.
Semiconductors	Loosely inserted in sockets. Distorted pins.	Firmly seat loose semiconductors. Remove devices having distorted pins. Carefully straighten pins (as required to fit the socket), using long-nose pliers, and reinsert firmly. Ensure that straightening action does not crack pins, causing them to break off.
Wiring and Cables	Loose plugs or connectors. Burned, broken, or frayed wiring.	Firmly seat connectors. Repair or replace defective wires or cables.
Chassis	Dents, deformations, and damaged hardware.	Straighten, repair, or replace defective hardware.

CLEANING. To clean the interior, blow off dust with dry, low-pressure air (approximately 9 psi). Remove any remaining dust with a soft brush or a cloth dampened with a solution of mild detergent and water. A cotton-tipped applicator is useful for cleaning in narrow spaces and on circuit boards. If these methods do not remove all the dust or dirt, the instrument may be spray washed using a solution of 5% mild detergent and 95% water as follows:

CAUTION

An exception to the following procedure is the Front-Panel module. Clean it only with isopropyl alcohol as described in step 4.

1. Gain access to the parts to be cleaned by removing easily accessible shields and panels.

2. Spray wash dirty parts with the detergent-and-water solution; then use clean water to thoroughly rinse them.

3. Dry all parts with low-pressure air.

NOTE

Most of the switches used in the 336 are sealed and the contacts are inaccessible. If cleaning is deemed necessary, use only isopropyl alcohol.

4. Clean switches with isopropyl alcohol and wait 60 seconds for the majority of the alcohol to evaporate. Then complete drying with low-pressure air.

5. Dry all components and assemblies in an oven or drying compartment using low-temperature (125° F to 150° F) circulating air.

LUBRICATION

There is no periodic lubrication required for this instrument.

SEMICONDUCTOR CHECKS

Periodic checks of the transistors and other semiconductors in the oscilloscope are not recommended. The best check of semiconductor performance is actual operation in the instrument.

PERIODIC READJUSTMENT

To ensure accurate measurements, check the performance of this instrument every 2000 hours of operation, or if used infrequently, once each year. In addition, replacement of components may necessitate readjustment of the affected circuits.

Complete Performance Check and Adjustment instructions are given in Sections 4 and 5. The Performance Check Procedure can also be helpful in localizing certain troubles in the instrument.

TROUBLESHOOTING

INTRODUCTION

Preventive maintenance performed on a regular basis should reveal most potential problems before an instrument malfunctions. However, should troubleshooting be required, the following information is provided to facilitate location of a fault. In addition, the material presented in the "Theory of Operation" and "Diagrams" sections of this manual may be helpful while troubleshooting.

TROUBLESHOOTING AIDS

Diagnostic Firmware

The operating firmware in this instrument contains diagnostic routines that aid in locating malfunctions. When instrument power is applied, power-up tests are performed to verify proper operation of the instrument's microprocessor, RAM and ROM. If a failure is detected, this information is passed on to the operator in the form of a crt readout error message. The failure information directs the operator to the failing block of memory. If the failure is such that the processor can still execute the diagnostic routines, the user can call up specific tests to further check the failing circuitry. The specific diagnostic routines are explained later in this section.

Schematic Diagrams

Complete schematic diagrams are located on tabbed foldout pages in the "Diagrams" section. Portions of circuitry mounted on each circuit board are enclosed by heavy black lines. The assembly number and name of the circuit are shown near either the top or the bottom edge of the diagram.

Functional blocks on schematic diagrams are outlined with a wide grey line. Components within the outlined area perform the function designated by the block label. The "Theory of Operation" uses these functional block names when describing circuit operation as an aid in cross-referencing between the theory and the schematic diagrams.

Component numbers and electrical values of components in this instrument are shown on the schematic diagrams. Refer to the first page of the "Diagrams" section for the reference designators and symbols used to identify components. Important voltages and waveform reference numbers (enclosed in hexagonal-shaped boxes) are also shown on each diagram. Waveform illustrations are located adjacent to their respective schematic diagram.

Circuit Board Illustrations

Circuit board illustrations showing the physical location of each component are provided for use in conjunction with each schematic diagram. Each board illustration is found in the "Diagrams" section on the back of a foldout page, preceding the first schematic diagram(s) to which it relates.

The locations of waveform test points are marked on the circuit board illustrations with hexagonal outlined numbers corresponding to the waveform numbers on both the schematic diagram and the waveform illustrations.

Circuit Board Locations

The placement in the instrument of each circuit board is shown in a board locator illustration. This illustration is located on the foldout page along with the circuit board illustration.

Power Distribution

Power Distribution circuitry is included on the schematics in the "Diagrams" section to aid in troubleshooting power-supply problems.

Circuit Board Interconnection Diagram

A circuit board interconnection diagram is provided in the "Diagrams" section. Interconnecting plugs are shown and the appropriate schematic diagrams are indicated to provide the pin connections and signal names for the larger circuit board connectors.

Grid Coordinate System

Each schematic diagram and circuit board illustration has a grid border along its left and top edges. A table located adjacent to each diagram lists the grid coordinates of each component shown on that diagram. To aid in physically locating components on the circuit board, this table also lists the grid coordinates of each component on the circuit board illustration.

Near each circuit board illustration is an alphanumeric listing of all components mounted on that board. The second column in each listing identifies the schematic diagram on which each component can be found. These component-locator tables are especially useful when more than one schematic diagram is associated with a particular circuit board.

Troubleshooting Charts

The troubleshooting charts contained in the "Diagrams" section are to be used as an aid in locating malfunctioning circuitry. To use the charts, begin with the Troubleshooting Index flowchart. This chart will help identify problem areas and will direct you to other appropriate charts for further troubleshooting.

Some malfunctions, especially those involving multiple simultaneous failures, may require more elaborate troubleshooting approaches with references to circuit descriptions in the "Theory of Operation" section of this manual.

Component Color Coding

Information regarding color codes and markings of resistors and capacitors is located on the color-coding illustration (Figure 9-1) at the beginning of the "Diagrams" section.

RESISTOR COLOR CODE. Resistors used in this instrument are carbon-film, composition, or precision metal-film types. They are usually color coded with the EIA color code; however, some metal-film type resistors may have the value printed on the body. The color code is interpreted starting with the stripe nearest to one end of the resistor. Composition resistors have four stripes; these represent two significant digits, a multiplier, and a tolerance value. Metal-film resistors have five stripes representing three significant digits, a multiplier, and a tolerance value.

CAPACITOR MARKINGS. Capacitance values of common disc capacitors and small electrolytics are marked on the side of the capacitor body. White ceramic capacitors are color coded in picofarads, using a modified EIA code.

Dipped tantalum capacitors are color coded in microfarads. The color dot indicates both the positive lead and the voltage rating. Since these capacitors are easily destroyed by reversed or excessive voltage, be careful to observe the polarity and voltage rating when replacing them.

DIODE COLOR CODE. The cathode end of each glass-encased diode is indicated by either a stripe, a series of stripes or a dot. For most diodes marked with a series of stripes, the color combination of the stripes identifies three digits of the Tektronix Part Number, using the resistor color-code system. The cathode and anode ends of a metal-encased diode may be identified by the diode symbol marked on its body.

Semiconductor Lead Configurations

Figure 9-2 in the "Diagrams" section shows the lead configurations for semiconductor devices used in the instrument. These lead configurations and case styles are typical of those used at completion of the instrument design. Vendor changes and performance improvement changes may result in changes of case styles or lead configurations. If the device in question does not appear to match the configuration shown in Figure 9-2, examine the associated circuitry or consult a manufacturer's data sheet.

Multipin Connectors

Multipin connector orientation is indexed by two triangles; one on the holder and one on the circuit board. Slot numbers are usually molded into the holder. When a connection is made to circuit board pins, ensure that the index on the holder is aligned with the index on the circuit board (see Figure 6-1).

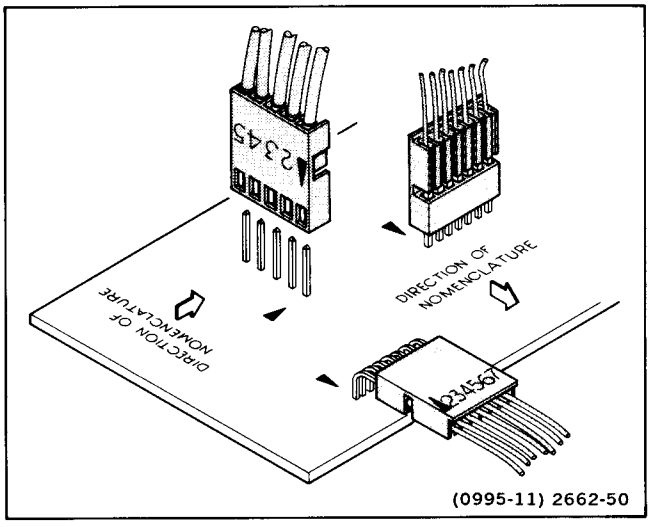


Fig. 6-1. Multipin connector orientation.

TROUBLESHOOTING EQUIPMENT

The equipment listed in Table 4-1 of this manual, or equivalent equipment, may be useful when troubleshooting this instrument.

TROUBLESHOOTING TECHNIQUES

The following procedure is arranged in an order that enables checking simple trouble possibilities before requiring more extensive troubleshooting. The first two steps use diagnostic aids inherent in the instrument's operating firmware and will locate many circuit faults. The next four

procedures are check steps that ensure proper control settings, connections, operation, and adjustment. If the trouble is not located by these checks, the remaining steps will aid in locating the defective component. When the defective component is located, replace it using the appropriate replacement procedure given under "Corrective Maintenance" in this section.

CAUTION

Before using any test equipment to make measurements on static-sensitive, current-sensitive, or voltage-sensitive components or assemblies, ensure that any voltage or current supplied by the test equipment does not exceed the limits of the component to be tested.

1. Power-up Tests

The 336 performs automatic verification of the instrument's Microprocessor, ROM, and RAM (the operating kernel).

If the kernel test fails, the memory (RAM or ROM) is identified by a message on the crt (if the instrument is able to produce a display). If a failure occurs, refer to the "Diagnostic Routines" discussion later in this section for definitions of error messages.

Once a problem area has been identified, the associated troubleshooting procedure should be performed to further isolate the problem. The troubleshooting procedures are located on tabbed-foldout pages in the "Diagrams" section at the rear of this manual.

2. Diagnostic Test Routines

The instrument firmware contains seven diagnostic routines that may be selected by the user from the front panel to further clarify the nature of a suspected failure. The desired test is selected using the MENU buttons after entering the Diagnostics Mode. Entry into the Diagnostic Mode and its uses are explained in the "Diagnostic Routines" discussion later in this section.

3. Check Control Settings

Incorrect control settings can give a false indication of instrument malfunction. If there is any question about the correct function or operation of any control, refer to either the "Operating Information" in Section 2 of this manual or to the 336 Operators Manual.

4. Check Associated Equipment

Before proceeding, ensure that any equipment used with the 336 is operating correctly. Verify that input signals are properly connected and that the interconnecting cables are not defective. Check that the ac-power-source voltage to all equipment is correct.

5. Visual Check

Perform a visual inspection. This check may reveal broken connections or wires, damaged components, semiconductors not firmly mounted, damaged circuit boards, or other clues to the cause of an instrument malfunction.

6. Check Instrument Performance and Adjustment

Check the performance of either those circuits where trouble appears to exist or the entire instrument. The apparent trouble may be the result of misadjustment. Complete performance check and adjustment instructions are given in Sections 4 and 5 of this manual.

7. Isolate Trouble to a Circuit

To isolate problems to a particular area, use any symptoms noticed to help locate the trouble. Refer to the troubleshooting charts in the "Diagrams" section as an aid in locating a faulty circuit

When trouble symptoms appear in more that one circuit, first check the power supplies; then check the affected circuits by taking voltage and waveform readings. Check first for the correct output voltage of each individual supply. These voltages are measured between the power supply test points and ground (see schematic diagram 19, and associated circuit board illustrations in the "Diagrams" section).

The Low Voltage Power Supply levels are interdependent. All the low voltage supplies use the +2.5 V reference for their reference levels. If more that one of the low voltage supplies appears defective, check the +2.5 V REF and the +5 V Digital supplies first.

A defective component elsewhere in the instrument can create the appearance of a power-supply problem and may also affect the operation of other circuits. Use the power supply troubleshooting charts to aid in locating the problem.

8. Check Circuit Board Interconnections

After the trouble has been isolated to a particular circuit, again check for loose or broken connections, improperly seated semiconductors, and heat-damaged components.

9. Check Voltages and Waveforms

Often the defective component can be located by checking circuit voltages or waveforms. Typical voltages are listed on the schematic diagrams. Waveforms indicated on the schematic diagrams by hexagonal-outlined numbers are shown adjacent to the diagrams. Waveform test points are shown on the circuit board illustrations.

NOTES

Voltages and waveforms indicated on the schematic diagrams are not absolute and may vary slightly between instruments. To establish operating conditions similar to those used to obtain these readings, see the voltage and waveform setup conditions preceding the waveform illustrations.

Note the recommended test equipment, front-panel control settings, voltage and waveform conditions, and cable-connection instructions. Any special control settings required to obtain a given waveform are noted under the waveform illustration. Changes to the control settings from the initial setup, other than those noted, are not required.

10. Check Individual Components

The following procedures describe methods of checking individual components. Two-lead components that are soldered in place are most accurately checked by first disconnecting one end from the circuit board. This isolates the measurement from the effects of the surrounding circuitry. See Figure 9-1 for component value identification and Figure 9-2 for semiconductor lead configurations.

WARNING

To avoid electric shock, always disconnect the instrument from the ac power source before removing or replacing components.

CAUTION

When checking semiconductors, observe the static-sensitivity precautions located at the beginning of this section.

TRANSISTORS. A good check of a transistor is actual performance under operating conditions. A transistor can most effectively be checked by substituting a known-good component. However, be sure that circuit conditions are not such that a replacement transistor might also be damaged. If substitute transistors are not available, use a dynamic-type transistor checker for testing. Static-type transistor checkers are not recommended, since they do not check operation under simulated operating conditions.

When troubleshooting transistors in the circuit with a voltmeter, measure both the emitter-to-base and emitter-to-collector voltages to determine whether they are consistent with normal circuit voltages. Voltages across a transistor may vary with the type of device and its circuit function.

Some of these voltages are predictable. The emitter-to-base voltage for a conducting silicon transistor will normally range from 0.6 V to 0.8 V. The emitter-to-collector voltage for a saturated transistor is about 0.2 V. Because these values are small, the best way to check them is by connecting a sensitive voltmeter across the junction rather that comparing two voltages taken with respect to ground. If the former method is used, both leads of the voltmeter must be isolated from ground.

If voltage values measured are less that those just given, either the device is shorted or no current is flowing in the external circuit. If values exceed the emitter-to-base values given, either the junction is reverse biased or the device is defective. Voltages exceeding those given for typical emitter-to-collector values could indicate either a nonsaturated device operating normally or a defective (open-circuited) transistor. If the device is conducting, voltage will be developed across the resistors in series with it; if open, no voltage will be developed across the resistors unless current is being supplied by a parallel path.

CAUTION

When checking emitter-to-base junctions, do not use an ohmmeter range that has a high internal current. High current may damage the transistor. Reverse biasing the emitter-to-base junction with a high current may degrade the current-transfer ratio (Beta) of the transistor.

A transistor emitter-to-base junction also can be checked for an open or shorted condition by measuring the resistance between terminals with an ohmmeter set to a range having a low internal source current, such as the R X 1 kΩ range. The junction resistance should be very high in one direction and much lower when the meter leads are reversed.

When troubleshooting a field-effect transistor (FET), the voltage across its elements can be checked in the same manner as previously described for other transistors. How-

ever, remember that in the normal depletion mode of operation, the gate-to-source junction is reverse biased; in the enhanced mode, the junction is forward biased.

INTEGRATED CIRCUITS. An integrated circuit (IC) can be checked with a voltmeter, test oscilloscope, or by direct substitution. A good understanding of circuit operation is essential when troubleshooting a circuit having IC components. Use care when checking voltages and waveforms around the IC so that adjacent leads are not shorted together. An IC test clip provides a convenient means of clipping a test probe to an IC.

CAUTION

When checking a diode, do not use an ohmmeter scale that has a high internal current. High current may damage a diode. Checks on diodes can be performed in much the same manner as those on transistor emitter-to-base junctions. Do not check tunnel diodes or back diodes with an ohmmeter; use a dynamic tester, such as the TEKTRONIX 576 Curve Tracer.

DIODES. A diode can be checked for either an open or a shorted condition by measuring the resistance between terminals with an ohmmeter set to a range having a low internal source current, such as the R X 1 kΩ range. The diode resistance should be very high in one direction and much lower when the meter leads are reversed.

Silicon diodes should have 0.6 to 0.8 V across their junctions when conducting. Higher readings indicate that they are either reverse biased or defective, depending on polarity.

RESISTORS. Check resistors with an ohmmeter. Refer to the "Replaceable Electrical Parts" list for the tolerances of resistors used in this instrument. A resistor normally does not require replacement unless its measured value varies widely from its specified value and tolerance.

INDUCTORS. Check for open inductors by checking continuity with an ohmmeter. Shorted or partially shorted inductors can usually be found by checking the waveform response when high-frequency signals are passed through the circuit.

CAPACITORS. A leaky or shorted capacitor can best be detected by checking resistance with an ohmmeter set to one of the highest ranges. Do not exceed the voltage rating of the capacitor. The resistance reading should be high after the capacitor is charged to the output voltage of the ohmmeter. An open capacitor can be detected with a capacitance meter or by checking whether the capacitor passes ac signals.

11. Repair and Adjust the Circuit

If any defective parts are located, follow the replacement procedures given under "Corrective Maintenance" in this section. After any electrical component has been replaced, the performance of that circuit and any other closely related circuit should be checked. Since the power supplies affect all circuits, performance of the entire instrument should be checked if work has been done on the power supplies or if the power transformer has been replaced. Readjustment of the affected circuitry may be necessary . Refer to the "Performance Check" and "Adjustment Procedure", sections 4 and 5 of this manual.

DIAGNOSTIC ROUTINES

The diagnostic routines contained in the 336 operating firmware consist of the power-up tests that are automatically performed when power is first applied and seven user-initiated test routines.

Power-on Tests

At power on, the instrument runs the internal diagnostic routines. While the tests are in progress, all displays are turned off, and the front-panel LED indicators are all lighted. In about five seconds or less, the tests are completed, and the instrument commences normal operation, unless a Checksum error is detected. Error messages are displayed on the crt to indicate the location of a detected Checksum error. The possible error messages are:

CPU A7 U200 BAD,

CPU A7 U220 BAD,

CPU A7 U300 BAD,

and when Option 01 is installed:

OPTION A8 U300 BAD,

OPTION A8 U310 BAD.

Error messages indicate that some or all of the oscilloscope functions may not work in a normal manner. The exact nature and amount of malfunctioning depends on the circuitry involved.

User-Initiated Diagnostics

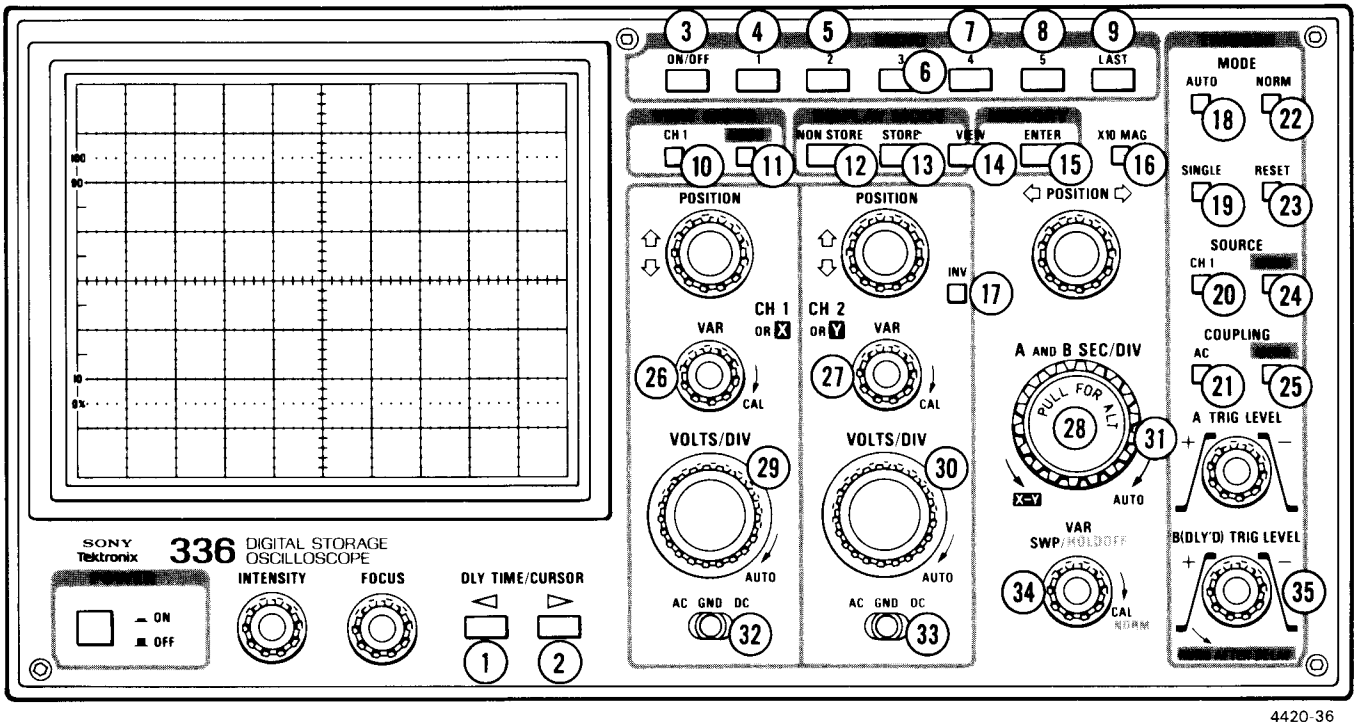
Entry into the Diagnostics Mode is accomplished by pressing both the MENU ON/OFF and the MENU LAST buttons in simultaneously. When the routine is in effect, all the normal crt displays are turned off. There is a choice of seven MENU selectable diagnostic tests available, after pressing the Trigger Mode RESET button to obtain the selection mode. Exiting from a selected test routine is done by again pressing the Trigger Mode RESET button. Exiting from the Diagnostic function completely is done by again pressing the MENU ON/OFF and the MENU LAST buttons in together.

NOTE

Turn VIEW Display Mode off prior to entering the Diagnostic Mode. A firmware problem in Version 4.4 does not allow normal exiting if VIEW is on when entering diagnostics. To exit diagnostics in this case, press the MENU ON/OFF and LAST button in together and release quickly. Turning the power off, then back on again will also reset the 336 to the normal operating condition.

Test Routines

NUMBER KEY STUCK TEST. This test is entered by pressing in the MENU LAST button. The test displays a number that corresponds to one of the front-panel push buttons, rotary switches, toggle switches, or detent switches as they are pressed or changed, as appropriate. Use of this test will check that all the switches and switch positions are being read by the instrument's microprocessor when they are actuated and if any switch is stuck. Table 6-4 list the switches and their associated numbers. The secondary numbers given define the setting of the multiposition switches. Figure 6-2 illustrates the number associated with each front-panel switch or control that is read.



4420-36

Fig. 6-2. Controls and associated numbers for the NUMBER KEY STUCK diagnostic test.

Table 6-4
Number Key Stuck Test

Control Name	Display		Secondary Number Definition
<	1		
>	2		
MENU			
ON/OFF	3		
1	4		
2	5		
3	6		
4	7		
5	8		
LAST	9		
VERT MODE			
CH 1	10		
MENU	11		
DISPLAY MODE			
NON STORE	12		
STORE	13		
VIEW	14		
ENTER	15		
X10 MAG	16		
INV (Invert)	17		
TRIGGER			
AUTO	18		
SINGLE	19		
SOURCE CH 1	20		
COUPLING AC	21		
NORM	22		
RESET	23[a]		
SOURCE MENU	24		
COUPLING MENU	25		
CH 1 VAR	26	1	UNCAL
	26	0	CAL
CH 2 VAR	27	1	UNCAL
	27	0	CAL
HORIZ DISPLAY	28	1	A ALT B
	28	0	A OR B
CH 1 VOLTS/DIV	29	15 ~ 0	16 INCREMENTS
CH 2 VOLTS/DIV	30	15 ~ 0	16 INCREMENTS
A AND B SEC/DIV	31	15 ~ 0	16 INCREMENTS
CH 1 AC-GND-DC	32	1	DC
		2	AC
		3	GND

Table 6-4 (cont)

Control Name	Display		Secondary Number Definition
CH 2 AC-GND-DC	33	1	DC
		2	AC
		3	GND
VAR SWP/HOLDOFF	34	1	VARIABLE
	34	0	CAL/NORM
B TRIGGER	35	1	RUNS AFTER DELAY
	35	0	TRIGGERABLE

[a] Number 23 for the RESET button will never be displayed, as pressing the button exits the test.

CHARACTER DISPLAY RAM CHECK. Pressing the MENU 2 button causes a display of 256 + (plus) characters on the crt. This test verifies the Character RAM and Character Generator and may be used to check the Geometry and TRACE ROTATION adjustments.

DISPLAY ALL CHARACTERS. A display of all 63 possible characters is generated when the MENU 3 button is pressed. This test also verifies the Character RAM and Character Generator and is useful for checking the Astigmatism adjustment.

CHIP SELECT CHECK. When the MENU 4 button is pressed, the microprocessor begins a read and write routine to addresses 0000(H) through FFFF(H) to verify the address decoding and chip select strobes. The only front-panel visual indication that the test is in progress is that any readout displays on the crt will blink slightly. A test oscilloscope may be used to check the operation of the address decoding and microprocessor address lines while the test is in progress.

GPIB (GENERAL PURPOSE INTERFACE BUS) OPTION CHECK. This test is used as a check on the GPIB portion of Option 01. It is started by pressing MENU button 1. When started, the GPIB interface places repeated data from 0 to 255 on the bus data lines. The 336 GPIB interface does not assert a service request (SRQ) and does not execute interface clear (IFC) or device clear (DCL) interface commands with the GPIB test. The handshake in this mode does not conform to the IEEE-488 Interface Standard, and the data is not expected to be received by all types of listeners or controllers. The data output lines can be checked using a test oscilloscope to verify that they are functioning. When the Trigger Mode RESET button is pressed to exit this check, the 336 stops placing data on the output lines without sending a message terminator. See Figure 7-3 in Section 7 for the electrical and physical arrangement of the GPIB output connector.

WAVEFORM RAM CHECK. This test generates a display of four 128-point ramps, with data-point values ranging from 64 to 191. At the end of the ramp waveform, five steps will appear. These steps have data-point values of 78, 103, 128, 153, and 178 respectively. This test, initiated by pressing the MENU ON/OFF button, is used to verify the waveform RAM and associated circuitry. The steps and waveform amplitude are used to check the gain and alignment of the stored display against the crt graticule. If X10 MAG is pressed on prior to entering the diagnostic routines, the test waveform will be horizontally magnified for a more detailed examination of the waveform with respect to missing or wrong data.

CORRECTIVE MAINTENANCE

INTRODUCTION

Corrective maintenance consists of component replacement and instrument repair. This part of the manual describes special techniques and procedures required to replace components in this instrument. If it is necessary to ship your instrument to a Tektronix Service Center for repair or service, refer to the "Repackaging for Shipment" information in Section 2 of this manual.

MAINTENANCE PRECAUTIONS

To reduce the possibility of personal injury or instrument damage, observe the following precautions.

1. Disconnect the instrument from the ac-power source before removing or installing components.

2. Verify that the line-rectifier filter capacitors are discharged prior to performing any servicing.

3. Use care not to interconnect instrument grounds which may be at different potentials (cross grounding).

4. When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, many of the standard electronic components can usually be obtained from a local commercial source. Before purchasing or ordering a part from a source other than Tektronix, Inc., please check the "Replaceable Electrical Parts" list for the proper value, rating, tolerance, and description.

NOTE

Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

Special Parts

In addition to the standard electronic components, some special parts are used in the 336. These components either are manufactured or selected by SONY/TEKTRONIX, Inc. to meet specific performance requirements, or they are manufactured for SONY/TEKTRONIX, Inc. in accordance with our specifications. The various manufacturers can be identified by referring to the "Cross Index-Manufacturer's Code number to Manufacturer" at the beginning of the "Replaceable Electrical Parts" list. Order all special parts directly from your local Tektronix Field Office or representative.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., be sure to include all of the following information:

1. Instrument type (include modification or option numbers).

2. Instrument serial number.

3. A description of the part (if electrical, include its full circuit component number)

4. Tektronix part number.

Selectable Components

Several components in the 336 are selectable to obtain optimum circuit operation. Value selection of these components is done during the initial factory adjustment procedure. Further selection is not usually necessary for subsequent adjustments unless a component has been changed that affects circuitry for which a selected component has been specifically chosen.

At this time, the components listed in Table 6-5 have been designated as selectable. See the Replaceable Electrical Parts List for part numbers. Also, check the Change Pages at the rear of this manual for additional changes that may occur between manual reprints.

Table 6-5
Selectable Components

Component	Values	Purpose
A1C2	Nominal 0.39 pf Select 0.68 pf Select 1.00 pf	Match CH 1 input C.
A1R13 A1R18	Nominal 15 Ω Select 10 Ω	Obtain correct CH 1 transient response.
A1R313 A1R318	Nominal 15 Ω Select 10 Ω	Obtain correct CH 2 transient response.
A12C130 A12C230	Nominal 0.39 pf Select 0.20 pf Select 0.56 pf	Obtain correct magnified sweep linearity.

MAINTENANCE AIDS

The maintenance aids listed in Table 6-6 include items required for performing most of the maintenance procedures in this instrument. Equivalent products may be substituted for the examples given, provided their characteristics are similar.

Table 6-6
Maintenance Aids

Description	Specification	Usage	Example
1. Soldering Iron	15 to 25 W.	General soldering and unsoldering.	Antex Precision Model C.
2. Flat-bit Screwdriver	4-inch shaft, 3/16-inch bit.	Assembly and disassembly.	
3. Phillips Screwdriver	Tip sizes: #1, #2, magnetic tip	Assembly and disassembly.	
4. Nutdrivers	3/16 inch, 5/16 inch.	Assembly and disassembly.	Xcelite #6 and #10.
5. Open-end Wrenches	3/8 inch, 5/16 inch, 9/16 inch.	Assembly and disassembly.	
6. Allen Wrenches	0.050 inch, 1/16 inch.	Assembly and disassembly.	
7. Long-nose Pliers		Component removal and replacement.	Diamalloy Model LN55-3.
8. Diagonal Cutters		Component removal and replacement.	Diamalloy Model M554-3.
9. Vacuum Solder Extractor	No static charge retention.	Unsoldering static sensitive devices and components on multilayer boards.	Pace Model PC-10.
10. Spray Cleaner	No-Noise ®	Switch and pot cleaning.	Tektronix Part Number 006-0442-02.
11. Pin-replacement Kit		Replace circuit board connector pins.	Tektronix Part Kit Number 040-0542-00.
12. IC-removal Tool		Removing DIP IC packages.	Augat T114-1.
13. Isopropyl Alcohol	Reagent grade.	Cleaning attenuator and front-panel assemblies.	2-Isopropanol.
14. Power Supply Load Module	Provide proper loading of the power supply.	Troubleshooting power supply problems.	Tektronix Part Number 670-8133-00.
15. Service Maintenance Kit	336 circuit board extenders and extender cables.	Troubleshooting circuit boards.	Tektronix Part Number 067-1161-00.

INTERCONNECTIONS

Interconnections in this instrument are made with pins soldered onto the circuit boards. Several types of mating connectors are used for the interconnecting pins. The following information provides the replacement procedures for the various type connectors.

End-Lead Pin Connectors

Pin connectors used to connect the wires to the interconnect pins are factory assembled. They consist of machine-inserted pin connectors mounted in plastic holders. If the connectors are faulty, the entire wire assembly should be replaced.

Multipin Connectors

When pin connectors are grouped together and mounted in a plastic holder, they are removed, reinstalled, or replaced as a unit. If any individual wire or connector in the assembly is faulty, the entire cable assembly should be replaced. To provide correct orientation of a multipin connector, an index arrow is stamped on the circuit board, and either a matching arrow is molded into or the numeral 1 is marked on the plastic housing as a matching index. Be sure these index marks are aligned with each other when the multipin connector is reinstalled.

TRANSISTORS AND INTEGRATED CIRCUITS

Transistors and integrated circuits should not be replaced unless they are actually defective. If removed from their sockets or unsoldered from the circuit board during routine maintenance, return them to their original board locations. Unnecessary replacement or transposing of semiconductor devices may affect the adjustment of the instrument. When a semiconductor is replaced, check the performance of any circuit that may be affected.

Any replacement component should be of the original type or a direct replacement. Bend transistor leads to fit their circuit board holes, and cut the leads to the same length as the original component. See Figure 9-2 in the "Diagrams" section for lead-configuration illustrations.

The chassis-mounted power supply transistor is insulated from the chassis by a heat-transferring mounting block. Reinstall the mounting block and bushings when replacing these transistors. Use a thin layer of heat-transferring compound between the insulating block and chassis when reinstalling the block.

NOTE

After replacing a power transistor, check that the collector is not shorted to the chassis before applying power to the instrument.

To remove socketed dual-in-line packaged (DIP) integrated circuits, pull slowly and evenly on both ends of the device. Avoid disengaging one end of the integrated circuit from the socket before the other, since this may damage the pins.

To remove a soldered DIP IC when it is going to be replaced, clip all the leads of the device and remove the leads from the circuit board one at a time. If the device must be removed intact for possible reinstallation, do not heat adjacent conductors consecutively. Apply heat to pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

SOLDERING TECHNIQUES

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used to remove or replace parts. General soldering techniques, which apply to maintenance of any precision electronic equipment, should be used when working on this instrument.

WARNING

To avoid an electric-shock hazard, observe the following precautions before attempting any soldering: turn the instrument off, disconnect it from the ac power source, and wait at least three minutes for the line-rectifier filter capacitors to discharge.

Use rosin-core wire solder containing 63% tin and 37% lead. Contact your local Tektronix Field Office or representative to obtain the names of approved solder types.

When soldering on circuits boards or small insulated wires, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron may cause etched circuit conductors to separate from the board base material and melt the insulation on small wires. Always keep the soldering-iron tip properly tinned to ensure best heat transfer from the iron tip to the solder joint. Apply only enough solder to make a firm joint. After soldering, clean the area around the solder connection with an approved flux-removing solvent (such as isopropyl alcohol) and allow it to air dry.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum-type desoldering equipment should attempt repair of any circuit board in this instrument. Many integrated circuits are static sensitive and may be damaged by solder extractors that generate static charges. Perform work involving static-sensitive devices only at a static-free work station while wearing a grounded antistatic wrist strap. Use only an antistatic vacuum-type solder extractor approved by a Tektronix Service Center.

CAUTION

Attempts to unsolder, remove, and resolder leads from the component side of a circuit board may cause damage to the reverse side of the circuit board. The following techniques should be used to replace a component on a circuit board:

1. Touch the vacuum desoldering tool to the lead at the solder connection. Never place the iron directly on the board; doing so may damage the board.

NOTE

Some components are difficult to remove from the circuit board due to a bend placed in the component leads during machine insertion. To make removal of machine-inserted components easier, straighten the component leads on the reverse side of the circuit board.

2. When removing a multipin component, especially an IC, do not heat adjacent pins consecutively. Apply heat to the pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

CAUTION

Excessive heat can cause the etched circuit conductors to separate from the circuit board. Never allow the solder extractor tip to remain at one place on the board for more than three seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for desoldering multipin components) must not be used. Damage caused by poor soldering techniques can void the instrument warranty.

3. Bend the leads of the replacement component to fit the holes in the circuit board. If the component is replaced while the board is installed in the instrument, cut the leads so they protrude only a small amount through the reverse side of the circuit board. Excess lead length may cause shorting to other conductive parts.

4. Insert the leads into the holes of the board so that the replacement component is positioned the same as the original component. Most components should be firmly seated against the circuit board.

5. Touch the soldering iron to the connection and apply enough solder to make a firm solder joint. Do not move the component while the solder hardens.

6. Cut off any excess lead protruding through the circuit board (if not clipped to the correct length in step 3).

7. Clean the area around the solder connection with an approved flux-removing solvent. Be careful not to remove any of the printed information from the circuit board.

REMOVAL AND REPLACEMENT INSTRUCTIONS

WARNING

To avoid electric shock, disconnect the instrument from the ac power source before removing or replacing any component or assembly.

The exploded view drawings in the "Replaceable Mechanical Parts" list (Section 10) may be helpful during the removal and reinstallation of individual components or subassemblies. Circuit board and component locations are shown in "Diagrams," Section 9 of this manual.

Read these instructions completely before attempting any corrective maintenance.

Cabinet

Removal of the instrument cabinet is accomplished as follows:

1. Unplug the power cord from the ac power source.

2. Unplug the power cord from the rear-panel connector.

3. Install the plastic front-panel cover, place the handle against the top of the cabinet, and set the instrument face down on a flat surface.

4. Remove the two phillips-head retaining screws in the bottom of the cabinet.

5. Loosen the two phillips-head screws holding the rear panel in place and remove the rear panel. Carefully slide the cabinet off of the instrument.

WARNING

The line-rectifier filter capacitors may retain a charge for a short period of time after the instrument is turned off. Normally, the time required to remove the cabinet will allow these capacitors to discharge to a safe level; however, if operating the instrument with the cover off for servicing, allow one to two minutes after turning the power off before beginning any cleaning or servicing.

To reinstall the cabinet, perform the reverse of the preceding instructions. When sliding the cabinet back on, take care not to pinch any of the internal cabling between the cabinet and the chassis.

Power Supply Module

Removal of the Power Supply Module is accomplished as follows:

1. Remove the cabinet as described in that procedure.

2. Remove the three screws holding the top cover of the supply module to the module chassis and remove the cover. Note the orientation of the internal cabling with respect to the shield attached to the top cover plate for reinstallation.

3. Disconnect multipin connectors P50 and P56 from the rear of the Main Board. Note connector orientation for reinstallation.

4. Remove multipin connector P100 from the rear of the Horizontal Amplifier Board, noting orientation for reinstallation.

5. Using needle-nose pliers, disconnect multipin connector P174 from right-front corner of the DC/DC Converter Board (bottom of supply module, attached to the HV Multiplier module) noting connector orientation for reinstallation.

6. Remove the four screws, two on either side of the supply module, holding the module to the main chassis. Do not remove the screw holding the power supply switching transistor to the chassis.

7. Partially separate the supply module from the chassis and disconnect the crt socket by prying evenly on both sides of the socket.

8. Place the instrument on its left side (to make access to the multipin connectors on the bottom easier) and work the connectors (disconnected in step 3 above) through the plastic chassis slot while sliding the supply module away from the chassis.

To reinstall the Power Supply Module, perform the reverse of the preceding instructions.

Dismantling the Power Supply Module

HIGH VOLTAGE REGULATOR BOARD (A15) REMOVAL. To remove the High Voltage Regulator Board, perform the following steps:

1. Disconnect multipin connectors P10 and P1, noting orientation for reinstallation.

2. Remove the three mounting screws holding the board to the chassis of the module.

3. Pull the board up and away from the module, being careful not to bend the circuit board connecting pins as they are disengaged.

DC/DC CONVERTER BOARD (A13) REMOVAL. To remove the DC/DC Converter Board, perform the following steps:

1. Remove the three screws holding the bottom cover to the supply module chassis and remove the cover.

2. Disconnect multipin connector P30, near the power switch, noting orientation for reinstallation.

3. Remove the four corner screws holding the board to the chassis.

4. Remove the board, being careful not to bend the board connector pins as they disengage.

PRIMARY BOARD (A14) REMOVAL. To remove the Primary board, perform the following steps:

1. Disconnect multipin connectors P100 and P186, noting orientation for reinstallation.

2. Remove the two screws holding the fan to the chassis and remove the fan.

3. Remove the screw holding the power transistor mounting block/heat sink to the chassis.

4. Remove the three screws holding the board to the chassis and remove the board.

To reinstall the power supply boards, perform the reverse of the preceding instructions. Use a small amount of heat-transferring compound between the power transistor heat sink and the module chassis when that component is reinstalled.

Horizontal Amplifier (A12) Removal

To remove the Horizontal Amplifier board, perform the following steps:

1. Remove the instrument cabinet as described in that procedure.

2. Disconnect multipin connector P100 from the rear of the circuit board.

3. Disconnect multipin connectors P270 and P420 from the A4 Control Board, noting orientation for reinstallation.

4. Disconnect the horizontal deflection leads from the top of the crt.

5. Remove the two mounting screws holding the board to the chassis.

6. Slide the board sideways to disengage the pins of the circuit board connector and remove the board.

To reinstall the Horizontal Amplifier board, perform the reverse of the preceding instructions.

Vertical Amplifier (A11) Removal

To remove the Vertical Amplifier board, perform the following steps:

1. Remove instrument cabinet as described in that procedure.

2. Remove the Horizontal Amplifier as described in that procedure.

3. Disconnect the vertical deflection leads from the side of the crt.

4. Unsolder the two delay-line leads and the outer shielding conductor from the board.

5. Remove the two board-mounting screws and the two screws holding the transistor heat sinks (near hole in board) to the chassis.

6. Slide the board up to disengage the pins of the circuit board connector and remove the board.

To reinstall the Vertical Amplifier board, perform the reverse of the preceding instructions.

Trigger (A2), Sweep (A3), Control (A4), Acquisition (A5), Display (A6), CPU (A7), and Option (A8) Board Removal

NOTE

These boards are located in a plug-in circuit board compartment and are all removed in a similar manner.

To remove a board from the circuit board compartment, perform the following steps:

1. Remove the instrument cabinet as described in that procedure.

2. Remove the screw holding the circuit board retainer (bracket across the top of the circuit boards) and remove the retainer.

3. If the circuit board being removed is connected to the ribbon bus, disconnect all the large ribbon cable connectors from the top of the circuit boards (press tabs on each side of connectors outward to disconnect) and remove the cable.

4. Remove any other cabling attached to the top of the board, noting orientation for reinstallation.

NOTE

The Option board (A8) has three screws holding the board to the chassis which have to be removed before that board may be unplugged from the circuit board compartment.

5. Disengage the circuit board from the Main board connector pins by using the prying holes at the top corners of the board; then, slide the board out of the circuit board compartment.

To reinstall a plug-in circuit board, perform the reverse of the preceding instructions. Make sure the circuit board is properly aligned in the front and rear edge retaining slots before pressing the board down to engage the connector pins from the Main board.

Front Panel Removal

To remove the front panel (as an assembly), do the following:

1. Remove the instrument cabinet as described in that procedure.

2. Using a 0.050-inch hex-head tool, remove the four hex-head screws holding the front panel to the chassis.

3. Disconnect ribbon-cable connector P700 from the top of the CPU board (A7).

4. Disconnect multipin connectors P400, P480, and P500 from the Key Interface Board (A9), noting orientation for reinstallation.

5. Remove the two screws holding the grounding straps to the instrument chassis (near either front corner).

6. Slide the Front Panel assembly out of the chassis, routing the cabling through the chassis slots.

FRONT PANEL DISASSEMBLY (A9 AND A10). To remove the two front-panel circuit boards, perform the following steps:

1. Using a 0.050-inch hex-head tool, loosen the hex-head setscrew holding the SEC/DIV knob to the control shaft and remove the knob.

2. Using firm outward pressure, pull the remaining knobs from their control shafts. It may be necessary to pry the knobs off using a small flat-bladed screwdriver.

3. Remove the five screws holding the rear board of the assembly to its mounting posts.

4. Pull the board up and away from the panel, hinging it away from the smaller inner board.

5. Unscrew the two hex screws holding the smaller board to the front panel and remove the interconnected board assemblies.

6. If one of the boards must be replaced, unsolder the interconnecting cable using soldering techniques described elsewhere in this section. Do not consecutively heat adjacent conductors, as excessive heat may damage the board.

To reinstall the front-panel boards, perform the reverse of the preceding instructions.

Main Board (A1) Removal

1. Remove the instrument cabinet as described in that procedure.

2. Remove all the plug-in circuit boards from the circuit board compartment as described in that procedure.

3. Disconnect multipin connectors P50 and P56 from the rear of the Main board, noting orientation for reinstallation.

4. Disconnect multipin connectors P400, P480, and P500 from the front panel, noting orientation for reinstallation.

5. Disconnect trace rotation multipin connector (P926) from the rear of the Main board.

6. Unsolder the two delay-line leads and the delay-line grounding shield from the rear of the Main board, noting orientation for reinstallation.

7. Unsolder the wire to the CAL OUT terminal.

8. Unsolder the wires to the CHART OUT connectors.

9. Unsolder the resistors from the EXT TRIG IN and EXT Z-AXIS IN connectors.

10. Remove the eight screws holding the board to the chassis, including the one at the edge of the attenuator shield.

11. Tilt the edge of the board up (opposite side from the attenuators) and slide the board sideways out of the chassis.

To reinstall the Main board, perform the reverse of the preceding instructions.

CRT Removal

WARNING

Use care when handling a crt. Breakage of the crt may cause high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses (preferably a full-face shield) should be worn. Avoid striking the crt on any object which may cause it to crack or implode.

To remove the crt, perform the following steps:

1. Remove the instrument cabinet as described in that procedure.

2. Disconnect the horizontal- and vertical-deflection leads from the neck of the crt.

3. Unplug the crt socket from the rear of the crt by prying evenly on both sides of the socket.

WARNING

The crt may retain a high-voltage charge after the instrument is turned off. To avoid electrical shock, discharge the anode lead to chassis ground as soon as the insulating cover is slid back to expose the solder connection to the HV Multiplier.

4. Using needle-nose pliers having well-insulated handles, gently pry the plastic insulator on the anode lead forward to expose the solder connection to the HV Multiplier module.

5. Discharge the crt anode lead to chassis ground, using either the insulated pliers or a screwdriver or similar tool having an insulated handle. Repeat the grounding several times to ensure a complete discharge.

6. Unsolder the anode lead of the crt and disconnect it from the HV Multiplier.

7. Slide the plastic insulator off of the anode lead and retain it for reinstallation.

8. Loosen the Front Panel and slide it forward to expose the crt bezel.

9. Remove the two screws holding the crt bezel in place and remove the bezel and blue crt filter.

10. Slide the crt out of the chassis by pressing forward on the rear of the crt neck until the front of the crt may be grasped; then, continue removal by pulling from the front. Take care not to strike the crt neck on the chassis as it is being removed.

NOTE

Once the crt is removed, it should be stored in such a manner as to protect it from impact. If stored face down, it should be placed on a soft, nonabrasive surface to prevent the face plate from being scratched.

Installing a new crt is done by reversing the removal procedure steps. Feed the anode lead through the hole in the crt shield when sliding the crt back into the chassis. Slip the plastic insulator onto the anode lead before resoldering the lead to the HV Module.

OPTIONS

INTRODUCTION

This section contains a general description of the available options for the 336 Digital Storage Oscilloscope. Unique and more detailed operating information pertaining to the GPIB (General Purpose Interface Bus) portion of Option 01 follows the general option descriptions. Additional information about instrument options and option availability can be obtained either by consulting the current Tektronix Product Catalog or by contacting your local Tektronix Field Office or representative.

POWER CORD OPTIONS

Instruments are shipped with the detachable power-cord configuration ordered by the customer. Descriptive information about the international power-cord options is provided in Section 2, "Operating Information." The following list identifies the Tektronix part number for the available power cords.

Option A1 (Universal Euro)	161-0104-06
Option A2 (UK)	161-0104-07
Option A3 (Australian)	161-0104-05
Option A4 (North American)	161-0104-08
Option A5 (Switzerland)	161-0167-00

OPTION 01

This option combines an extended memory and battery backup with the General Purpose Interface Bus (GPIB) communication capability. Additional memory supplied with the option, provides storage space for up to eight frames (16 traces) of digitized waveforms (added to the standard instrument's one frame of memory space). These stored waveforms are maintained in memory by the battery backup system so that they may be recalled for display and analysis after the instrument has been off for an extended period of time.

Operating instructions for the extended memory portion of Option 01 are included wherever appropriate throughout this Service manual.

When equipped with this option, the 336 also has the capability to transmit a waveform message over an IEEE-488 General Purpose Interface Bus (GPIB). During a transmission, either the last STORE Mode waveform acquired or a displayed VIEW waveform (if VIEW Mode is enabled) will be sent to either a bus controller or a listener instrument on the bus. If no waveform data is available to be transmitted when the GPIB is requested to do so, the 336 will send only the ID portion of the normal transmission. The waveform message format will conform to the Tektronix Interface Standard (GPIB Codes, Formats, Conventions, and Features Standard).

Basic operating information pertaining to the use and control of the GPIB portion of Option 01 is included in Section 2, "Operating Information," of this manual. More detailed information concerning the use of a GPIB and the 336 in a system is contained in the following text.

Servicing information for both the GPIB and the extended memory portions of Option 01, including schematics, troubleshooting charts, and performance check procedures are incorporated in the appropriate sections of this service manual.

GPIB OPERATING INFORMATION

The GPIB is a digital interface that allows efficient communication between the components of an instrumentation system. It is used for transmitting and receiving data between self-contained instruments or devices and acts as an interface system that is independent of the actual function of those instruments or devices.

A Typical System on the GPIB

Figure 7-1 illustrates a typical system using the GPIB and shows the names and functions established for the 16 active signal lines. While only four instruments are shown, more may be supported by a GPIB system. Some instruments may have addressable subsections such as programmable plug-in units housed in a mainframe. In this type of configuration, the mainframe may be addressed with a primary address code, and the plug-in units would then be addressed with a secondary address code.

Instrument spacing and loading on a bus have constraints that must be observed to maintain the electrical characteristics of the bus. The operating instructions supplied with a GPIB bus controller must be observed when connecting instrumentation into a system configuration.

Controllers, Talkers, and Listeners

A talker is an instrument that can send data over the bus. The 336 is an example of a talker instrument that has transmitting capabilities only. Listener instruments can accept data from the bus. A programmable device, having front-panel functions that may be controlled via commands issued over the bus, is an example of a listener. However, a listener may only have a single capability, such as recording data from the bus, with no programmable functions available. Instruments may have both talker and listener capabilities combined as with instruments that are the most GPIB system oriented. The intended use of a device on a bus dictates its design requirements.

A GPIB controller is an instrument that, as its name implies, controls the communication activities on the bus. The controller determines which of the other instruments on a bus will talk and which will listen during any given time interval. The controller also has the ability to assign itself as either a talker or a listener, whenever the programmed routine requires. In addition to designating current talker and listeners for a particular communication sequence, the controller has the task of sending special controlling codes and commands (called interface messages) to remotely control any or all of the devices on the bus having programmable capabilities.

GPIB Signal Line Definitions

Figure 7-1 shows the 16 signal lines of the GPIB functionally divided into three component busses: an eight-line data transfer bus, a three-line transfer control (handshake) bus, and a five-line management bus.

THE DATA BUS. Eight bidirectional signal lines, DI01 through DI08, make up the data bus. Information, in the form of data bytes, is transferred over the data bus. A handshake sequence between an enabled talker and the enabled listeners transfers one data byte (eight parallel bits) at a time. Data bytes in either interface or device-dependent messages are sent in byte-serial, bit-parallel fashion over the data bus.

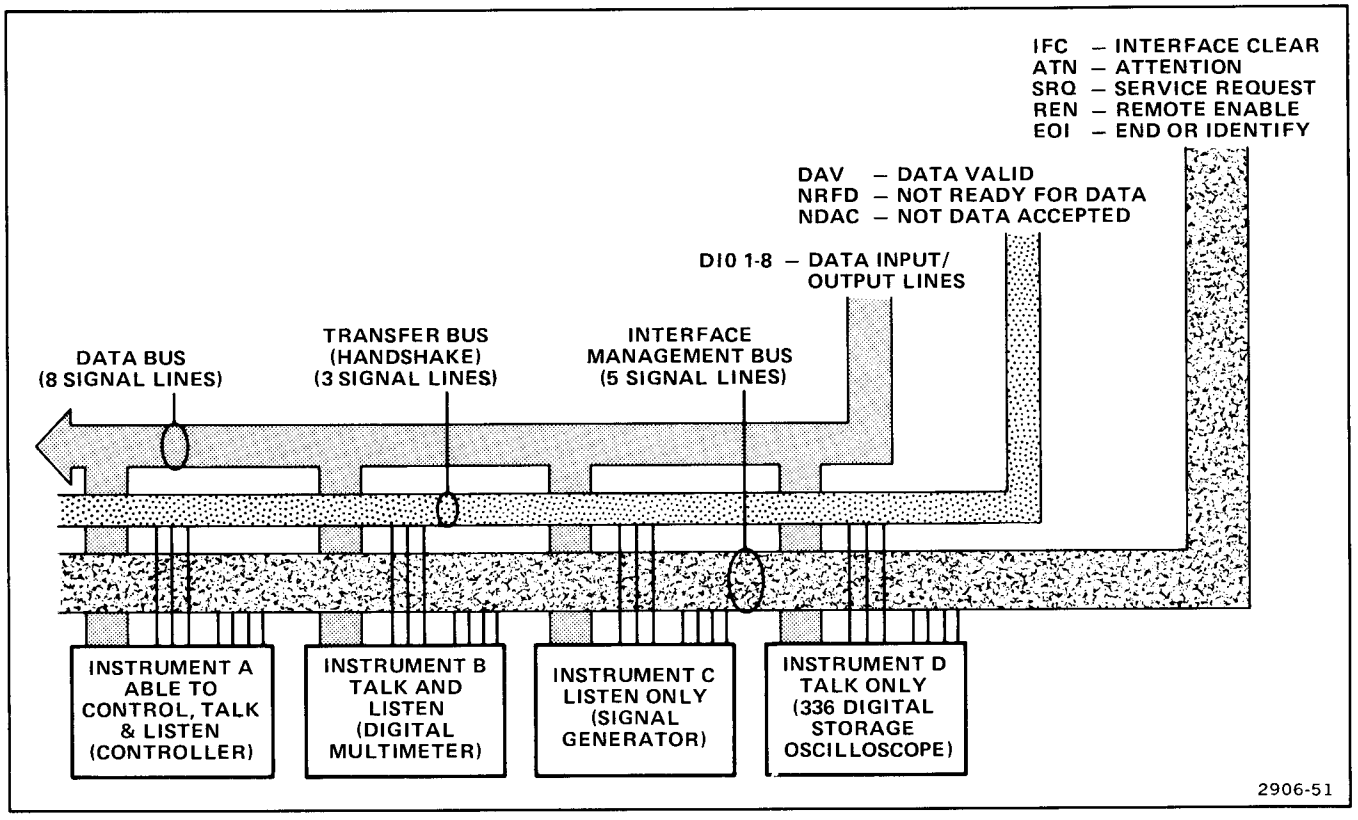


Figure 7-1. A typical system using the General Purpose Interface Bus.

Since the GPIB handshake sequence is an asynchronous operation, the data transfer rate at any one time is only as fast as the slowest instrument involved in the data-byte transfer. A talker cannot place data bytes on the bus faster than any one listener can accept them.

THE TRANSFER BUS (HANDSHAKE). Each time a data byte is sent over the data bus, an enabled talker and all enabled listeners execute a handshake sequence via the transfer bus. A typical handshake routine showing the activity on the transfer-bus signal lines is illustrated in Figure 7-2. The attention (ATN) line is also shown to illustrate the controller's role in the process.

NOTE

On the GPIB signal lines, the TRUE (asserted) level is the low amplitude, and the FALSE (unasserted) level is the high amplitude.

NOT READY FOR DATA (NRFD)—An asserted (TRUE) NRFD message indicates that one or more assigned listeners are not ready to receive the next data byte from the talker. When all of the assigned listeners for a particular data-byte transfer have released their NRFD, the NRFD message become FALSE. This RFD (Ready for Data) message tells the talker it may place the next data byte on the data bus.

DATA VALID (DAV)—The DAV message is asserted TRUE by the talker after the talker places a data byte on the data bus. The talker is inhibited from asserting DAV as long as any listener asserts the NRFD message.

NOT DATA ACCEPTED (NDAC)—Each assigned listener holds the NDAC message asserted TRUE until that listener accepts the data byte currently on the data bus. When all assigned listeners accept the current data byte, the NDAC message becomes FALSE. This DAC (Data Accepted) message tells the talker that all assigned listeners have accepted the current data byte, and that byte may be removed from the bus.

When both NDAC and NRFD are FALSE at the same time, an invalid state exists on the bus. This occurs when no listeners are assigned on the bus.

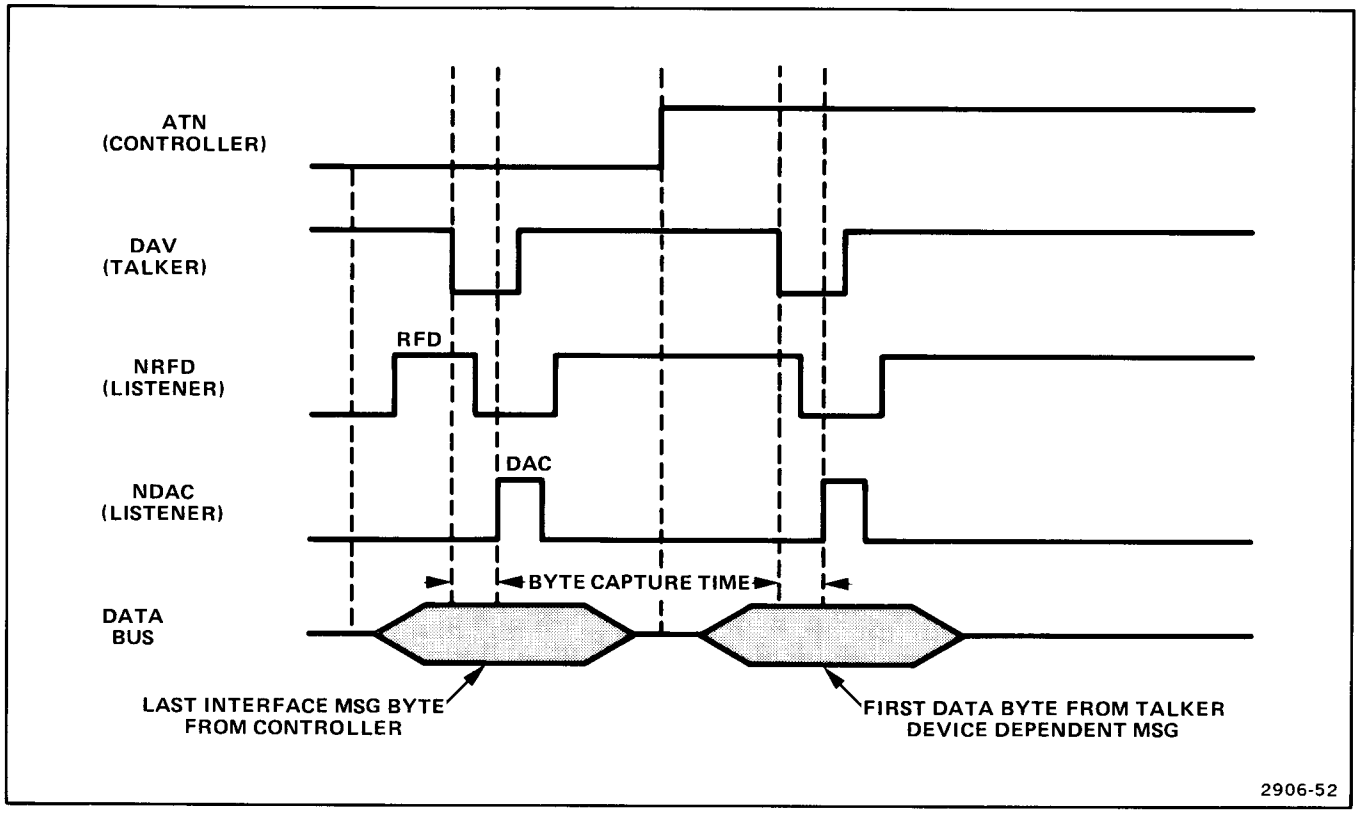


Figure 7-2. A typical handshake timing sequence (idealized).

THE MANAGEMENT BUS. The management bus contains five signal lines that control the operation of the GPIB. The lines are named as follows: Interface Clear (IFC), Attention (ATN), Service Request (SRQ), Remote Enable (REN), and End or Identify (EOI).

INTERFACE CLEAR—The bus controller asserts the IFC message TRUE to place all interface circuitry in a predetermined quiescent state (this may or may not be the power-on state). Only the bus controller can generate this signal. While IFC is TRUE, no other message will be recognized.

ATTENTION—A controller asserts the ATN message TRUE when instruments connected to the bus are being enabled as either talkers or listeners and when there is other interface-control traffic. As long as the ATN message is TRUE, only instrument address codes and control messages can be transferred over the data bus. With the ATN message FALSE, only those instruments enabled as a talker and listener(s) can transfer data. Only a controller can generate the ATN message.

SERVICE REQUEST—Any instrument connected to the bus can request the controller's attention by sending a service request (SRQ). The controller may respond by executing a serial poll to determine which instrument is requesting service. An instrument requesting service identifies itself by asserting data input/output line number seven (DIO7) TRUE when it sends the status byte. The status byte conveys to the controller what action is requested. Instruments not requesting service will send a "no status" byte as they are polled by the controller.

REMOTE ENABLE—The bus controller sends the REN message TRUE whenever the interface system is operating under remote program control. Used with other control messages, the REN message causes an instrument on the bus to select between two alternate sources of programming data. A remote-local interface function indicates to an instrument that it will receive information input from either the front-panel controls (LOCAL) or from the interface (REMOTE). Since the 336 does not have a remote capability, it transmits data as determined by the setting of its front-panel controls.

END OR IDENTIFY—A talker can use the EOI message to indicate the end of a data-transfer sequence. The talker sends the EOI message TRUE as the last byte of data is transmitted. In this sense, EOI is essentially a ninth data line and must observe the same setup times as the data bus lines.

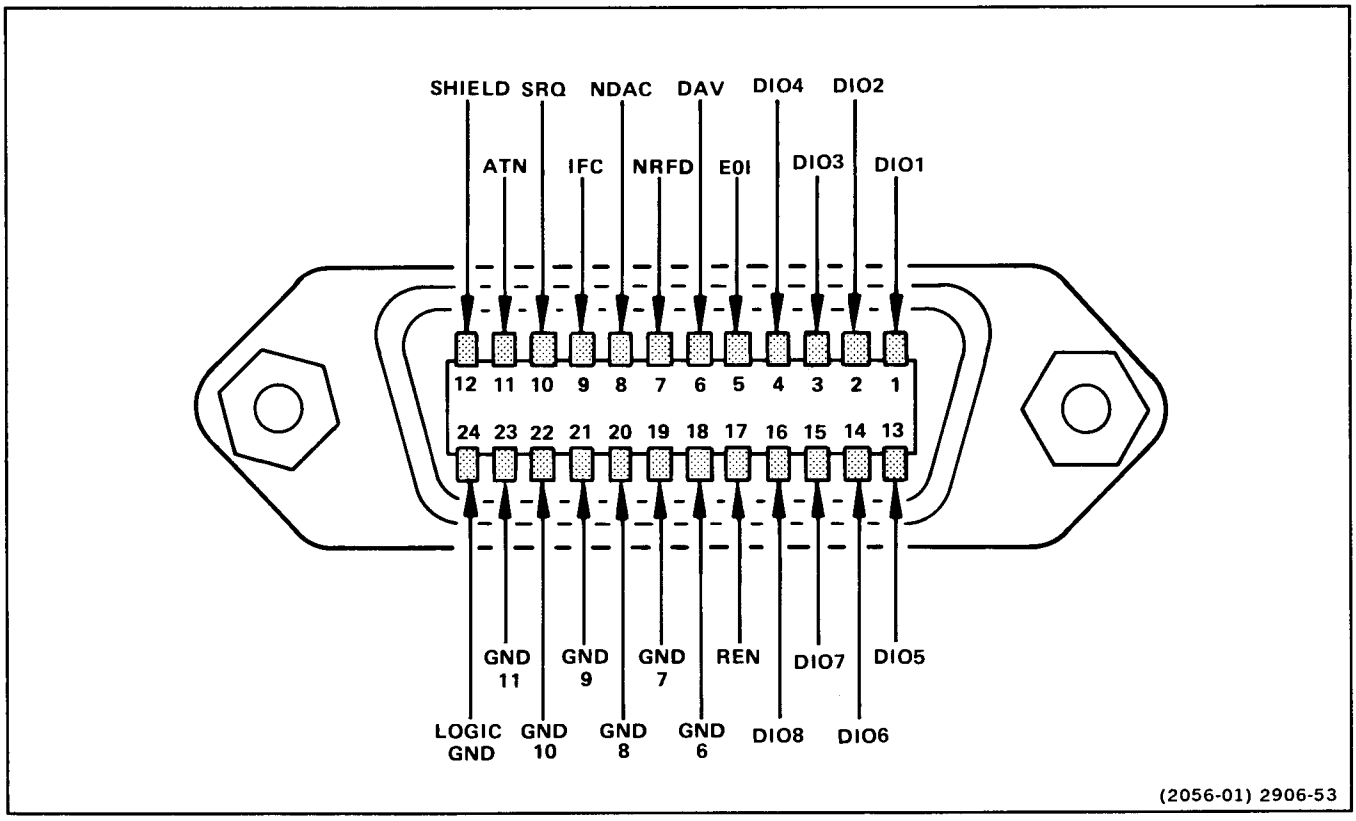


Figure 7-3. GPIB connector and pin assignments.

GPIB Connector

Physical arrangement of the 24-pin GPIB connector located on the right side panel of the 336, meets IEEE-488 (1978) GPIB standards. Sixteen pin are assigned to specific signals, and eight pins are assigned to shields and grounds. Voltage and current values required at the connector nodes are based on TTL technology (power source not to exceed +5.5 volts, referenced to ground). The logic levels are defined as follows. Logical 1 is a TRUE state, low-voltage level (less than or equal to +0.8 V), that is implemented when the signal line is asserted. Logical 0 is a FALSE state, high-voltage level (greater than or equal to +2 V), that is implemented when the signal line is not asserted. See Figure 7-3 for an illustration of connector pin assignments and physical arrangement.

Use a standard shielded GPIB cable with all the shields and grounds correctly connected to interconnect the 336 to other instruments on the bus. See the "Accessories" foldout at the rear of this manual for recommended part numbers.

Interface Functions and Commands

Since the 336 is a talker only, not all of the interface functions are enabled. Table 7-1 is a listing of the function subsets, including a description of the 336 capabilities with regard to those subsets. Table 7-2 is a listing of the interface commands to which the 336 responds, along with a brief description of each response.

Table 7-1
336 GPIB Function Subsets

Identification	Description	States Omitted	Other Requirements	Other Required Subsets Used
SH1 (Source Handshake)	Complete Capability	None	None	T1
AH1 (Acceptor Handshake)	Complete Capability	None	None	None
T1 (Talker)	Basic Talker, Serial Poll, Talk Only Mode	None	Omit [MLA∧(ACDS)]	SH1 and AH1
L0 (Listener)	No Capability	All	None	None
SR1 (Service Request)	Complete Capability	None	None	T1
RL0 (Remote/Local)	No Capability	All	None	None
PP0 (Parallel Poll)	No Capability	All	None	None
DC2 (Device Clear)	Omit Selective Device Clear	None	Omit [SDC∧(LADS)]	AH1
DT0 (Device Trigger)	No Capability	All	None	None
C0 (Controller)	No Capability	All	None	None

Table 7-2
Interface Commands

GPIB Message	336 Interface Response
Interface Clear (IFC)	The 336 returns to the serial-poll-idle state (SPIS) and enters the talker-idle state (TIDS). End or Identify (EOI) and new byte available (nba) become unasserted. An asserted service request (SRQ) remains on. The 336 interface then waits for IFC to become unasserted before processing other GPIB traffic, including attention (ATN).
Device Clear (DCL)	If received during transmission of data, the 336 clears the buffer containing the ID message and waveform data and removes any SRQ (except power on). The 336 remains addressed to talk, and begins sending the ID message and waveform data from the beginning without receiving a new My Talk Address (MTA) when the IFC is unasserted. To cease transmission of the message, the controller must also sent Untalk (UNT). DCL will not clear an SRQ issued by the 336 as part of the power-on routine. To remove the power-on SRQ, the 336 must be made a talker and the status byte sent. This ensures that the controller knows the 336 is powered up on the bus.
Serial Poll Enable (SPE)	The 336 interface enters the serial-poll-mode state (SPMS).
Serial Poll Disable (SPD)	The 336 leaves the serial-poll-mode state.
My Talk Address (MTA)	This is the address set by the user with the GPIB control menu. The bus controller sends MTA to the 336 to obtain its status byte in a serial poll or to start its transmission of waveform data.
Untalk (UNT)	336 untalks. This command must be sent by the controller along with DCL after receiving a Stop SRQ from the 336 to actually stop the transmission. MTA must be received by the 336 to begin a new waveform transmission after it has been untalked.
Other Talk Address (OTA)	No response.

GPIB Menu Operation

The GPIB Menu is selected using the Main MENU control buttons. It is one of the DATA OUT choices available with the first Main MENU that appears when the MENU ON/OFF button is pressed to turn the MENU display on. The GPIB Menu (see Figure 7-4) is used to control the GPIB section of Option 01. With the GPIB Menu displayed, the MENU 1 button (INCR) and MENU 2 button (DECR) are used to set the talk address of the 336. The addresses available are from 0 to 30 (decimal) inclusive. Incrementing past 30 or decrementing past 0 sets the 336 to the TALK ONLY Mode.

The 336 waveform data transmission can be initiated in two ways: either by pressing the MENU 3 button (TRANSMIT), or by being addressed to talk under direction of a bus controller. Either method will cause the waveform to be transmitted, but the sequence of events that occur in the 336 GPIB interface and on the bus depends on the setting of the instruments my talk address (either addressable or set to TALK ONLY).

ADDRESSABLE. With a controller on the bus, the 336 GPIB interface should be set to a talk address. This gives the controller maximum control of bus transactions. In this mode, a possible series of actions that may occur when the operator wants to send a waveform is as follows:

1. The MENU 3 (TRANSMIT) button is pressed in.

2. A service request message (SRQ) is sent to the controller, and the 336 interface waits for the controller to respond.

3. The controller may respond by doing a serial poll. (This is optional and would not be required if the 336 were the only instrument on the bus.) A typical serial-poll routine would be in the following sequence:

   a. Controller asserts the attention message (ATN) TRUE to gain control of the bus, then sends unlisten (UNL) and untalk (UNT). This prevents the listeners from receiving status bytes and prevents the current talker from sending data when the ATN is removed.

   b. Controller then sends the serial-poll enable message (SPE) to place all devices on the bus in the serial-poll mode.

   c. During the serial poll, the controller sends ATN and each device's My Talk Address (MTA), one at a time. As each device receives its own MTA, the controller will remove the ATN message, and the addressed device will send its status byte. The status byte will indicate to the controller each device's present state and which one(s) requires attention.

NOTE

The 336 will send (or attempt to send) its status byte as soon as the controller removes the ATN message.

   d. Upon finishing the serial poll, the controller sends ATN and the serial-poll-disable message (SPD), placing all devices in the serial-poll-idle state.

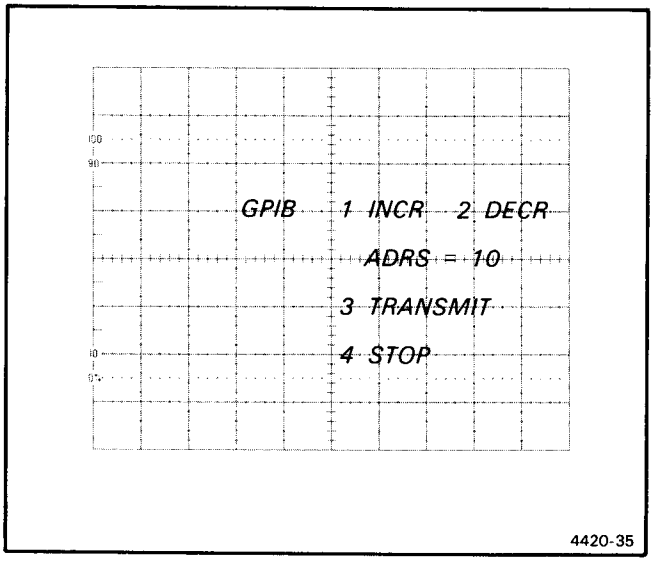


Figure 7-4. GPIB Control Menu.

4. After the poll, the controller may reconfigure the bus, assigning listeners to receive the waveform data from the 336, if necessary.

5. With the listener(s) assigned, the controller then sends the 336 its My Talk Address (MTA) to make the 336 a talker. When the controller removes the ATN message this time, the 336 sends the waveform data. When both Channel 1 and Channel 2 waveforms are displayed, pressing the MENU 3 (TRANSMIT) button (or a request by the controller) sends the Channel 1 data followed by the Channel 2 data. The ID message and waveform data is handshaked out to the listeners, one byte at a time. At the end of the waveform data message, the transmission is terminated by sending carriage return (CR) and line feed (LF) with end or identify (EOI).

NOTE

Once the waveform message is completed and EOI sent, the 336 must receive its My Talk Address (MTA) again before it will transmit any other messages. The controller cannot place the 336 in the TALK ONLY Mode or make it a permanent talker.

Under direction of a bus controller, the 336 will initiate a message transmission whenever it receives its talk address. Either a status byte or a waveform message (depending on the state of the 336 GPIB interface when the MTA is sent) will be transmitted by the 336 when the controller removes the ATN message.

The operator has the choice of stopping a transmission in progress by pressing the MENU 4 button (STOP). The action that occurs when stop is pressed depends on whether the 336 is addressable or in the TALK ONLY Mode. For the addressable condition, when STOP is pressed, the 336 issues a service request and the STOP status byte. When the controller receives the status byte from the 336, it would then have the capability to control the bus as the application requires. It can, for example, send Device Clear (DCL) and Untalk (UNT) to abort the transmission (the normal choice when the operator wishes to stop the transmission).

TALK ONLY MODE. When the 336 is in the TALK ONLY Mode, the controller has less control of the 336 GPIB interface. In this mode, the 336 will never enter the talker idle state (TIDS) because it is permanently a talker. The TALK ONLY Mode is most useful when there is no controller on the bus, and the 336 is used to transmit waveform data to a listener. In the TALK ONLY Mode with no bus controller, a typical series of actions that may occur when the operator wants to send a waveform is as follows:

1. The MENU 3 button (TRANSMIT) is pressed.

2. A service request (SRQ) is sent, and the 336 begins to begins to handshake the waveform data to a listener.
3. The transmission is completed, the message is terminated with a carriage return (CR) and a line feed (LF) with End or Identify (EOI), and the SRQ message is removed.

If the MENU 4 button (STOP) is pressed in the TALK ONLY Mode, the 336 completes the current handshake, then sends the message terminator (CR and LF with EOI).

The TALK ONLY Mode is not recommended with a controller on the bus. When the 336 is in TALK ONLY, a bus controller can not assign any other talkers on the bus. When there is no bus controller on the bus to respond to a service request, the 336 must be set to the TALK ONLY Mode to be able to transmit waveform data to an assigned listener.

Power-up State

The state of the GPIB existing when the 336 is powered up is as follows:

1. If the 336 is powered on during a bus transmission, an error may occur in the handshake routine in progress.
2. A power-on service request is issued. The power-on service request must be handled by a controller to remove it from the bus. When a controller receives the power-on status byte, it may reinitiate a bus transmission if one was in progress during the 336 power-on routine.
3. The 336 GPIB interface is in the talker-idle and serial-poll idle states.
4. Each power up completely resets the 336 interface, and the interface will be ready to transmit waveform data as soon as the 336 power-up routine is completed.

NOTE

When no waveform data has been acquired, or none is available to send, a request for transmitting waveform data will be replied with by only the ID portion of the normal waveform message.

Power-down State

When the 336 is powered down, a power-down routine stores the current instrument settings. VIEW waveform data is retained, but STORE waveform data is cleared from the display memory. The instrument will power on with the same operating conditions that were present at power off (with the exception of diagnostics mode).

GPIB Status Bytes

Status information relating to the state of the 336 GPIB interface is sent to the controller in the status byte during a serial poll. Two possible conditions exist: status with a service request asserted, and status with no service request asserted. Table 7-3 contains a listing of the status bytes available in the 336.

When the controller is responding to a service request from another device, the 336 status bytes without a service request asserted tell the controller the state of the 336. After the other device service request is handled, the controller uses the status reported by all the devices on the bus to determine what action occurs next. The action depends on controller programming.

As an example, assume that the 336 is in the middle of a transmission, and some other device on the bus issues a service request. The controller interrupts the transmission of the 336 by asserting attention (ATN) TRUE, and then it does a serial poll to determine the status of each device on the bus. Having handled the service request, the controller can then use the status reported by the 336 to restart or continue the transmission.

The controller may interrupt the 336 either synchronously (in step with the handshake) or asynchronously (with no regard to the handshake progress). If the controller interrupts synchronously, the last data byte sent will be data accepted (DAC) by all the assigned listeners and is not lost. An asynchronous interruption may or may not cause the loss of a byte, depending upon the point of interruption.

Table 7-3
336 GPIB Status Bytes

SRQ Condition	Status	Status Byte (decimal)
ASSERTED	POWER ON	65
	TRANSMIT REQUEST	195
	TON TRANSMIT REQUEST	196
	STOP REQUEST	197
UNASSERTED REQUEST	POWER ON	1
	TRANSMIT	131
	TON TRANSMIT REQUEST	132
	STOP REQUEST	133
	NO STATUS	0

The method of interruption may determine what action takes place to restart the 336 transmission. If no data is lost, the controller can reassign listeners and remove attention (ATN), and the 336 will resume transmission at the point of interruption. If data may have been lost, the controller might send device clear (DCL) to clear the data from the 336 output buffer and all the listeners. After reassigning listeners, the controller then removes attention, and the 336 will begin transmitting the waveform data message from the beginning (including the ID portion of the message).

If untalk (UNT) was also sent, the 336 must also receive its talk address before it will begin transmitting again.

336 GPIB Message Protocol

When the 336 is connected to a bus having a bus controller, it will send a message whenever it receives its My Talk Address (MTA). The talk address is set by the operator using the GPIB control menu (see GPIB Menu Operation).

If a Device Clear (DCL) message is received by the 336 during a transmission, the 336 stops transmitting and clears its GPIB output buffers of the waveform message being sent. Pending events are halted and an asserted SRQ is removed. DCL will not halt the power-on routine, nor will it remove the SRQ issued at power on. The power-on SRQ must be handled by making the 336 a talker and letting the power-up status byte be sent. This ensures that the bus controller knows the 336 is powered up on the bus. The DCL messages does not move the 336 out of the talker state, it remains addressed. As soon as the DCL message is removed and attention is unasserted, the 336 will start sending the waveform message that was interrupted from the beginning without receiving its talk address. To actually halt the transmission from the 336, the controller must also send Untalk (UNT). The 336 will require the reception of its My Talk Address again before it becomes a talker once it has been untalked.

336 Message

The message sent by the 336 conforms to Tektronix Standard, "General Purpose Interface Bus, Codes, Formats, Conventions and Features Standard."

The term "message" as used here, refers to a device-dependent remote message. It is not an interface message, and it does not interfere with interface message coding or use.

A message represents a given amount of information, with the beginning and ending clearly defined. It is communicated between the 336 (as a talker) and one or more devices acting as listeners. The message begins when the 336 first begins functioning as a talker and all assigned listeners begin functioning as listeners.

MESSAGE FORMAT. A waveform message consists of an identification block (ID) and zero or more waveforms (only one waveform per message in the 336), separated by delimiters. The following message format is described using BNF (bacus normal form) notation. The BNF symbols are defined in Table 7-4.

Table 7-4
BNF Symbol Notation

Symbol	Definition
<>	Defined element.
::=	Is defined as.
()	Explanation.
{}	Grouping.
|	Exclusive OR.
&	AND-designates concurrent messages on the bus (the element on the right of & is concurrent with the last element of the expression on the left.
"	String argument delimiter.
:	Link argument delimiter.
;	Message unit delimiter.
,	Argument delimiter.
%	Precedes a binary block argument.

The transmitted message is in the following format:

<MESSAGE>::=<ID>[;<WAVEFORM>...]
<TERMINATOR>

When the optional [;<WAVEFORM>] is omitted, the format is changed
to:

<MESSAGE>::=<ID>;<TERMINATOR>

Each of the defined elements <> is further broken down as follows:

<ID>::=ID <SCOPE TYPE>,<C AND F
VERSION>,<FIRMWARE VERSION>

For the 336 message, the elements are further defined as follows:

<SCOPE TYPE>::=SONY-TEK/336 (Identifies the instrument as a SONY/TEK 336 Digital Storage Oscilloscope.)

<C AND F VERSION>::=V81.1 (States the version of Tektronix Standard GPIB Codes and Formats in use—Version 81.1.)

<FIRMWARE VERSION>::=FV:00000 (States the firmware version installed in the instrument.)

An example of the ID element is:

ID SONY-TEK/336,V81.1,FV:V4.4

NOTE

All punctuation, including spaces, must be as shown. The waveform element is in the following format:

<WAVEFORM>::=<PREAMBLE>,<BLOCK BINARY CURVE>

These message elements are further defined as follows:

<PREAMBLE>::=WFMPRE<WPA>[{,<WPA>}...]

Where <WPA>::=(WAVEFORM PREAMBLE ARGUMENTS)

The following waveform preamble arguments <WPA> are listed in the order in which they are transmitted in a message. After each, a brief description is given.

<WAVEFORM ID>::=WFID:"{CH1|CH2}{AC|GND|DC}"

The defined elements of <WAVEFORM ID> are: the VERT MODE selected for the waveform and the Input Coupling.

<NUMBER OF POINTS>::=NR.PT:{1024}

The defined element is the length of the data record for the waveform being transmitted (1024 bytes for the 336).

<POINT FORMAT>::=PT.FMT:Y

The Y-coordinate is transmitted, but the X-coordinate is determined from the data point number and the X INCREMENT.

<X INCREMENT>::=XINCR:{100|50|20|10|5|2|1|500|200}

The defined element increment multiplied by the X UNITS is the time between data points.

<X ORIGIN>::=XZERO:0

X ORIGIN is defined as zero.

<POINT OFFSET>::=PT.OFF:{0|128|512|896}

The defined element is the STORE Mode trigger point, determined by the ACQ WINDOW selection for real-time sampled waveforms. The menu-selectable choices are: PRE TRIG, MID TRIG, or POST TRIG. For equivalent-time sampled waveforms, the trigger point is FULL POST TRIG (all acquired data occurs after the trigger event).

<X UNITS>::=XUNIT:{MS|US|NS}

X UNITS are used with the X INCREMENTS to establish the time scale of the transmitted waveform data.

<Y MULTIPLIER>::=YMULT:{200|400|800|2|4|8|20|40|80}

The defined element is a vertical scaling factor determined by the VOLTS/DIV setting at which the waveform data was acquired.

<Y ORIGIN>::=YZERO:0

Y ORIGIN is defined as zero.

<Y VALUE OFFSET>::=YOFF:<GND REF VALUE>

The defined element is the value of the vertical position of the ground reference.

<Y UNITS>::=YUNIT:{V|MV|UV|DIV}

Defined element is the unit attached to the vertical value of each data point.

<DATA ENCODING>::=ENCDG:BIN

Curve data encoding is in low-level binary code.

<BINARY FORMAT>::=BN.FMT:RP

Each number sent is a binary, positive integer.

<BYTES PER NUMBER>::=BYT/NR:1

One byte is sent for each number.

<BITS PER NUMBER>::=BIT/NR:8

Eight bits are in each byte.

This ends the message preamble. The message continues with the binary information.

<BLOCK BINARY CURVE>::=CURVE %<BINARY COUNT><BINARY DATA POINT>...<CHECKSUM>

These defined elements contain the waveform data and are further broken down as follows:

<BINARY COUNT>::= (A two-byte binary integer to specify the number of data bytes plus the checksum byte—data bytes plus one. The high-order byte is sent before the low-order byte.)

<BINARY DATA POINTS>::= (The binary value of the waveform at a specific data point.) This area contains a binary data-point-defined element for each data point in the waveform message.

<CHECKSUM>::= (The two's complement of the modulo 256 sum of the preceding binary data bytes and the binary count bytes. Does not include the % symbol preceding the binary count.)

After the binary information of the waveform message is transmitted, the message is ended with the terminator.

<TERMINATOR>::=CRLF&EOI (Carriage Return then Line Feed and End or Identify). Line Feed sent concurrently with End or Identify terminates the message transmission.

The following example illustrates a typical waveform message with the ID element added to make a complete message.

```
ID SONY-TEK/336,V81.1,FV:V4.4,WFMPRE
WFID:"CH1 DC",NR.PT:1024,PT.FMT:Y,
XINCR:50,XZERO:0,PT.OFF:128,XUNITS:US,
YMULT:40,YZERO:0, YOFF:43,
YUNIT:MV,ENCDG:BIN,BN.FMT:RP,
BYT/NR:1, BIT/NR:8,CURVE %
<BINARY COUNT><BINARY DATA POINT>...
<CHECKSUM>CRLF&EOI
```

A more detailed explanation of the codes and formats is contained in the Tektronix Interface Standard (GPIB, Codes, Formats, Conventions and Features Standard).

Calculating Coordinate Values

The absolute coordinate values of the waveform data points are calculated using the information obtained from the message. In the point format used (PT.FMT:Y), only the Y-axis values are transmitted; the X-axis values are determined from both the data point number and the X-increment value. The transmitted data is used in the following formulas:

$X_n = XO + DX(n - NO)$ and $Y_n = YO + SY(y_n - YR)$,

where the symbols used are defined as follows:

X_n, Y_n::= Absolute X- and Y-coordinate values at point n.

n::= data point number in the waveform curve (n = 1,2,3, ...1024).

DX::= X-increment (horizontal distance between data points).

NO::= X-point offset (trigger point).

XO::= X-origin.

YO::= Y-origin.

SY::= Y-multiplier (scaling factor).

y_n::= Y-data point value.

YR::= Y-value offset (ground reference).

X-COORDINATE VALUES. As an example, the following information obtained from a sample message is used to find the X-coordinate of data point 28.

n = 28

XO = 0

DX = 50

NO = 128

X-UNITS = μs

Substituting these values into the formula for Xn:

$X_{28} = 0 + 50(28 - 128)$

$= 50(-100) = -5000$

Adding the X-units, we find that the absolute coordinate value at data point 28 with respect to the trigger point (NO = 128) is:

$X_{28} = -5000\ \mu s = -5$ ms.

Positive X-coordinate values will be obtained for data points occurring after the trigger point.

NOTE

The position of the trigger point is determined by the ACQ WINDOW selection (PRE TRIG, MID TRIG, or POST TRIG for real-time sampling or FULL POST TRIG for equivalent-time sampling).

The SEC/DIV switch setting and the horizontal graticule location of data points 28 and 128 (the trigger point) can then be determined from the X-increment, X-units, and absolute X-coordinate values.

Since there are 1000 data points spanning the full 10 horizontal graticule divisions, the SEC/DIV switch setting can be found by the equation:

$$\text{SEC/DIV switch setting} = \frac{1000\ DX}{10} = 100\ DX$$

where the units of DX are as specified by the X-units message element.

Substituting values into the formula, we obtain:

$$\text{SEC/DIV switch setting} = 100 \text{ data points/div} \times$$
$$= 50\ \mu\text{s/data point}$$
$$= 5000\ \mu\text{s/div}$$
$$= 5 \text{ ms/div}$$

The horizontal distance of data point 28 from the beginning of the trace can then be calculated from the formula:

$$\text{Horizontal distance} = \frac{DX\ (n)}{\text{SEC/DIV switch setting}}$$

Substituting values into the formula, we obtain:

$$\text{Horizontal distance} = \frac{50\ \mu\text{s/data point} \times 28 \text{ data points}}{5 \text{ ms/div}}$$
$$= \frac{1400\ \mu\text{s}}{5 \text{ ms/div}} = \frac{1.4 \text{ ms}}{5 \text{ ms/div}}$$
$$= 0.28 \text{ division.}$$

The horizontal distance from the beginning of the trace at which the trigger occurs can also be calculated using the same formula:

$$\text{Horizontal distance} = \frac{50\ \mu\text{s/data point} \times 128 \text{ data points}}{5 \text{ ms/div}}$$
$$= \frac{6400\ \mu\text{s}}{5 \text{ ms/div}} = \frac{1.4 \text{ ms}}{5 \text{ ms/div}}$$
$$= 1.28 \text{ divisions.}$$

Y-COORDINATE VALUES. In a similar manner, the absolute value of the Y-coordinate at data point 28 may also be calculated using the transmitted information. Continuing with the preceding example, the following Y-axis values are obtained from the previously given sample message:

$y_n = 63$ (assumed value for example)

$YO = 0$

$SY = 40$

$YR = 43$

Y-units = mV

Substituting these values into the equation for Y_n :

$$Y_n = YO + SY(yn - YR)$$

$$Y_{28} = 0 + 40(63 - 43)$$

$$Y_{28} = 40(20) = 800$$

Adding the Y-units, we find that the absolute Y-coordinate value at data point 28 is:

$Y_{28} = 800$ mV.

The positive value of Y_{28} indicates that the data point is located above the ground reference. Negative Y-coordinate values will be obtained for data points occurring below the ground reference. The Vertical POSITION control may be adjusted to place the ground reference at any desired location within the graticule area. Therefore the physical location of any data point (along the vertical axis) is determined by the positioning of the ground reference.

Knowing that the vertical resolution is 25 data points per division and using the given Y-axis example value, the vertical displacement of data point 28 above the ground reference can then be calculated from the formula:

$$\text{Vertical displacement} = \frac{Y_n}{25\ SY}$$

where the units of SY are as specified by the Y-units message element.

Substituting values into the formula, we obtain:

$$\text{Vertical displacement} = \frac{800\text{ mV}}{25\text{ data points/div} \times 40\text{ mV/data point}}$$

$$= \frac{800\text{ mV}}{1000\text{ mV/div}}$$

$$= 0.8 \text{ division above ground reference.}$$

GPIB DRIVER PROGRAMS

Two sample driver program listings for use with the 336 Digital Storage Oscilloscope are provided. The first is useful when using a Tektronix 4050-series Active Terminal as a bus controller, and the second is useful when using the Tektronix 4041 GPIB controller with the 4006, the 4010, or the 4012 terminal.

When the 336 is used in a system, either one of the sample programs or an operator-developed program must be started after the 336 is powered up on the bus. These programs, when used with the appropriate controller, will handle the 336 SRQ, copy the waveform message, and display the waveform with graticule and waveform preamble. When using the 336 on an operating system, actual programming will depend on the system's requirements.

4050-Series Program Listing

When entering this program for use, the remarks (REM) lines, which are listed to aid the user in understanding the program, may be omitted. If the remark lines are left out, the remaining program lines must be numbered as listed (or the program edited to the correct line numbers for subroutines and branching).

Program Listing

```
1 REM {Program to receive, decode, and
2 REM display waveforms from 336}
3 GO TO 100
4 PAGE
5 GO TO 320
6 REM Press user's key 1 to request a new waveform.
8 PAGE
9 GO TO 100
10 REM Press user's key 2 to restart from beginning.
12 GO TO 2330
14 REM Press user's key 3 for list of instructions.
100 INIT
110 SET KEY
120 F=0
130 A1=1
140 P=0
150 K=1
160 DIM A$(300)
170 REM Disable SRQ handling until ready.
180 ON SRQ THEN 1810
190 REM Set the 336 to a talk address.
200 PRINT "ENTER THE TALK ADDRESS OF THE 336. ";
210 INPUT A
220 REM SRQ handling routine.
230 ON SRQ THEN 1750
240 PRINT "WAITING FOR DATA ACQUISITION REQUEST."
250 REM If transmit request SRQ is received, then F=1
260 REM If a poll was made, then P=1
270 IF P=0 THEN 290
280 GOSUB 1910
290 IF F=0 THEN 270
```

```
300 GOSUB 330
310 GO TO 230
320 WBYTE @20,95:
330 T=0
340 PRINT "NEW WAVEFORM PLOT REQUESTED."
350 FOR W=1 TO 300
360 NEXT W
370 PAGE
380 REM Initialize variables for waveform plot.
390 A$=""
400 A1=1
410 REM Set alternate record separator to "%" for start
420 REM of binary block.
430 PRINT @37,0:37,255,255
440 INPUT %A:A$
450 REM Above reads the waveform preamble into A$ and
460 REM halts transmission at the "%" sign.
470 Y=POS(A$,"NR.PT",1)
480 REM If Y=0 then no waveform was sent. Close
490 REM out the program.
500 IF Y=0 THEN 1700
510 REM Get the number of points to be transferred.
520 M$=SEG(A$,Y,12)
530 S=VAL(M$)
540 DELETE C
550 REM Create a numeric variable of the proper size
560 REM to hold the curve data.
570 DIM C(S)
580 REM Make a talker again to get rest of waveform.
590 WBYTE @64+A:
600 REM B1 is upper byte of byte count, B2 is the
610 REM lower byte of byte count, B3 is checksum data.
620 REM C should have all the curve points.
630 RBYTE B1,B2,C,B3,B5
640 REM Next data item is either a ";" or a <CR>.
650 REM If <CR>, it is the end of the transfer.
660 REM Check out the binary block for errors using
670 REM the checksum.
680 B4=SUM(C)+B1+B2+B3
690 REM * modulo 256.
700 IF B4/256=INT(B4/256) THEN 740
710 PRINT "ERROR IN BINARY BLOCK TRANSFER. ";
720 PRINT "GGGGDATA MAY NOT BE VALID"
730 REM Draw the scope grid on the display.
740 VIEWPORT 20,120,10,90
750 IF T=1 THEN 860
760 WINDOW 0,10,0,8
770 FOR I=0 TO 10
780 IF K=197 OR K=0 THEN 2050
790 AXIS 0,0,I,I
800 NEXT I
810 AXIS 0.2,0.2,5,4
820 MOVE 0,1.45
830 GOSUB 1840
840 MOVE 0,6.45
850 GOSUB 1840
860 WINDOW 1,S-24,28,228
870 REM Draw the waveform on the display.
880 MOVE 1,C(I)
890 FOR I=1 TO S-24
```

```
900 DRAW I,C(I)
910 IF K=197 OR K=0 THEN 2050
920 NEXT I
930 HOME
940 WINDOW 0,130,0,100
950 VIEWPORT 0,130,0,100
960 REM Label graph with parameters from waveform
970 REM preamble.
980 REM **** Decode horizontal sweep speed.
990 DATA "S","MS","US","NS"
1000 REM Get the waveform preamble XUNITS.
1010 T$=SEG(A$,POS(A$,"XUN",1),12)
1020 T5=POS(T$,":",1)+1
1030 T6=POS(T$,",",T5)
1040 T$=SEG(T$,T5,T6-T5)
1050 IF T$<>"UNK" THEN 1220
1055 T$="UNCAL"
1057 GO TO 1220
1060 RESTORE 990
1070 FOR I=1 TO 4
1080 READ Z$
1090 IF Z$=T$ THEN 1110
1100 NEXT I
1110 RESTORE 990
1120 FOR J=1 TO I-1
1130 READ T$
1140 NEXT J
1150 REM **** Now get the horizontal sweep speed number.
1160 S$=SEG(A$,POS(A$,"XIN",1),12)
1170 S9=VAL(S$)/10
1180 REM Now we have the number and multiplier,
1185 REM calculate the sweep speed.
1190 S$=STR(S9)
1200 S$=S$&" "
1210 T$=S$&T$
1220 MOVE 80,3+(T=0)*90
1230 PRINT T$
1240 REM Now decode the vertical units of measurement.
1250 T$=SEG(A$,POS(A$,"YUN",1),12)
1260 T5=POS(T$,":",1)+1
1270 T6=POS(T$,",",T5)
1280 T$=SEG(T$,T5,T6-T5)
1290 IF T$<>"DIV" THEN 1320
1300 T$="UNCAL"
1310 GO TO 1470
1320 Z$=T$
1330 REM Now get the YMULT (volts/division) number.
1340 T$=SEG(A$,POS(A$,"YMULT",1),12)
1350 T9=VAL(T$)*25
1360 IF T9<100 OR Z$="V" THEN 1420
1370 T9=T9/1000
1380 IF Z$<>"UV" THEN 1410
1390 Z$="MV"
1400 GO TO 1420
1410 Z$="V"
1420 T$=STR(T9)
1430 REM Now decode the volts for screen
1440 REM representation on display.
1450 T$=T$&" "
1460 T$=T$&Z$
```

```
1470 MOVE 40,3+(T=0)*90
1480 PRINT T$
1490 REM Get the channel display information.
1500 T$=SEG(A$,POS(A$,"WFID",1),20)
1510 T9=POS(T$,"""",1)+1
1520 T8=POS(T$,"""",T9)
1530 T$=SEG(T$,T9,T8-T9)
1540 MOVE 60,3+(T=0)*90
1550 PRINT T$
1560 HOME
1570 REM See if last of xfer, or another waveform coming.
1580 IF B5=13 THEN 1620
1590 IF K=197 OR K=0 THEN 2050
1600 T=T+1
1610 GO TO 390
1620 INPUT @A:B$
1630 WBYTE @20,95:
1640 F=0
1650 P=0
1660 K=1
1670 GO TO 310
1680 REM Waveform NOT received; send what was
1690 REM received to screen and end.
1700 PRINT "THERE IS NO WAVEFORM AVAILABLE, ";
1710 PRINT "THE INSTRUMENT RESPONSE IS:"
1720 PRINT A$
1730 GO TO 1630
1740 REM SRQ handling subroutine.
1750 POLL D,K;A
1760 P=1
1770 IF K=195 THEN 1800
1780 F=0
1790 RETURN
1800 F=1
1810 RETURN
1820 REM Subroutine to print 0% and 100% graticule
1830 REM lines on the screen.
1840 G$="."
1850 FOR I=1 TO 56
1860 PRINT G$;
1870 IF K=197 OR K=0 THEN 2050
1880 NEXT I
1890 RETURN
1900 REM SRQ Reporting subroutine.
1910 IF K=197 OR K=0 THEN 2050
1920 IF K=196 THEN 2190
1930 IF K=195 THEN 2000
1940 IF K=65 THEN 2260
1950 F=0
1960 P=0
1970 PRINT "STATUS BYTE IS ";K;". UNDEFINED STATUS BYTE."
1980 WBYTE @20,95:
1990 RETURN
2000 F=1
2010 P=0
2020 K=1
2030 RETURN
2040 REM Routine to stop with 197 or 0 status byte.
2050 WBYTE @20,95:
2060 PAGE
```

```
2070 IF K<>197 THEN 2140
2080 REM Status byte is 197.
2090 PRINT "STATUS BYTE = ";K;". TRANSMIT STOP REQUEST."
2100 F=0
2110 P=0
2120 K=1
2130 GO TO 230
2140 PRINT "STATUS BYTE = ";K;". STOP WITH NO STATUS."
2150 GO TO 2100
2160 REM Routine to handle status byte 196.
2170 F=0
2180 P=0
2190 PAGE
2200 PRINT "PROGRAM HAS BEEN HALTED BECAUSE THE 336 IS"
2210 PRINT "IN THE TALK ONLY MODE.J"
2220 PRINT "SET THE 336 TO A TALK ADDRESS AND PRESS MENU"
2230 PRINT "BUTTON 4 TO HALT THE DATA TRANSFER ATTEMPT."
2240 GO TO 100
2250 REM Routine to handle status byte 65.
2260 PAGE
2270 PRINT "STATUS BYTE = 65, POWER ON SERVICE REQUEST."
2280 F=0
2290 P=0
2300 K=1
2310 GO TO 230
2320 REM Instructions for user's keys.
2330 WBYTE @20,95:
2340 PAGE
2350 PRINT "PRESSING USER'S KEY 1 STARTS A NEW WAVEFORM ";
2360 PRINT "WITHOUT ASKING"
2370 PRINT "FOR THE ADDRESS AGAIN. THE ADDRESS MUST HAVE ";
2380 PRINT "BEEN PREVIOUSLY"
2390 PRINT "ENTERED FOR THIS TO BE A VALID CHOICE."
2400 PRINT "JPRESSING USER'S KEY 2 RESTARTS THE PROGRAM "
2410 PRINT "FROM THE BEGINNING."
2420 PRINT "JPRESSING USER'S KEY 3 LISTS THE FUNCTION ";
2430 PRINT "OF THE USER'S KEYS."
2440 PRINT "IF PRESSED DURING A WAVEFORM PLOT, THE PLOT ";
2450 PRINT "WILL BE HALTED."
2460 PRINT "JAFTER THE ADDRESS HAS BEEN ENTERED, AND THE ";
2470 PRINT "PROGRAM IS WAITING"
2480 PRINT "FOR A DATA ACQUISITION, PRESSING MENU BUTTON 3 ";
2490 PRINT "WITH THE 336 GPIB MENU"
2500 PRINT "DISPLAYED, STARTS A NEW WAVEFORM PLOT. ONCE ";
2510 PRINT "STARTED, MENU"
2520 PRINT "BUTTON 4 MAY BE PRESSED TO STOP THE PLOT."
2530 PRINT "IF A TRANSMISSON IS IN PROGRESS WHEN STOPPED, ";
2510 PRINT "THE STATUS BYTE"
2520 PRINT "WILL BE RETURNED AS 197. A ZERO STATUS BYTE ";
2530 PRINT "WILL BE RETURNED"
2540 PRINT "IF NO TRANSMISSION IS IN PROGRESS WHEN THE STOP "
2550 PRINT "REQUEST IS MADE."
2560 PRINT "JTYPE IN RUN<CR> TO COMMENCE THE WAVEFORM ";
2570 PRINT "ACQUISITION PROGRAM."
```

4041 Driver Program

The 4041 controller uses different commands than the 4050-series active terminals to handle the 336 on the bus. The following sample program will get the waveform data from the 336, decode it, and display it on the following terminals: 4006, 4010, or 4012.

```
100  ! Program to get, decode, and display the waveforms from
110  ! the SONY/TEK 336 Oscilloscope using the 4041 controller.
120  ! This program will run on the 4006, 4010, or 4012 terminals only.
130  !
200    Init all
210    Disable srq
220  ! Erase the screen.
230  !
240    Print chr$(27)&chr$(12)
250  ! Get address of the 336.
260  !
270    Wait 1
280    Print "ENTER THE GPIB ADDRESS OF THE SONY/TEK 336."
290    Input addr$
300  !
310  !
320    On srq then gosub Srqhdl
330    Enable srq
340  !
350  ! Numcur will hold the number of waveforms to be transferred.
360  ! Set it to two for initialization.
370    Numcur=2
380    Dim a$ to 3000
390    A$=""
400  !
410  !
420  ! Set up physical and logical unit.
430  ! Set up so only EOI can terminate the communication.
440  !
450    Set driver "gpib0(eom=<0>):"
460    Open #1:"gpib0(pri="&addr$&",eom=<0>):"
470  !
480  ! Get all information and put in big string a$.
490  Input #1:a$
500  !
510  !
520  ! Check to see if waveform is transferred.
530    Check=pos(a$,"NR.PT",1)
540    If check=0 then goto Nowfm
550  !
560  ! Break data down into two parts for CH 1 and CH 2.
570  ! Each part will be broken into header and curve.
580  !
590    Dim head1$ to 200
600    Head1$=""
610    Perc=pos(a$,"CURVE %",1)
620    Head1$=seg$(a$,1,perc+6)
630  !
640    Dim curve1$ to 1200
650    A$=seg$(a$,perc+7,3000)
660    Semi1=pos(a$,";WFMPRE",1)
670    If semi1=0 then gosub Onecurve
680    Curve1$=seg$(a$,1,semi1-1)
690  !
```

```
700   ! Manipulate the waveform ID for waveform no.1.
710   !
720     Chcoup1$=seg$(head1$,pos(head1$,"WFID:",1)+6,6)
730     Xunit1$=seg$(head1$,pos(head1$,"XUNIT:",1),8)
740     Yunit1$=seg$(head1$,pos(head1$,"YUNITS:",1),8)
750   !
760   ! If Numcur=1 for just one waveform is to be transferred,
770   ! then don't try to find the second curve.
780     If Numcur=1 then goto Scopeid
790     Dim head2$ to 200
800     A$=seg$(a$,semi1+1,3000)
810     Perc=pos(a$,"CURVE %",1)
820     Head2$=seg$(a$,1,perc+6)
830   !
840     Dim curve2$ to 1200
850     Curve2$=seg$(a$,perc+7,1200)
860   !
870   ! Manipulate the waveform ID for waveform no.2.
880   !
890     Chcoup2$=seg$(head2$,pos(head2$,"WFID:",1)+6,6)
900     Xunit2$=seg$(head2$,pos(head2$,"XUNIT:",1),8)
910     Yunit2$=seg$(head2$,pos(head2$,"YUNIT:",1),8)
920   !
930   ! Now, everything is in order. The next steps manipulate
940   ! the information.
950   !
960   !
970 Scopeid: ! Print scope ID.
980   !
990   !
1000     Idpos=pos(head1$,";WFMPRE",1)
1010     Id$=seg$(head1$,3,idpos-3)
1020     Print "THE SCOPE ID IS:"
1030     Print ""
1040     Print id$
1050   !
1060   !
1070   ! Convert the data in curve$ to an array of intergers
1080   ! by taking the ascii of each character and put in array.
1090   !
1100     Dim point(1027)
1110     For i=1 to 1027
1120      Point(i)=asc(seg$(curve1$,i,1))
1130     Next i
1140   !
1150     Print chr$(27);chr$(12)
1160     Wait 1
1170   !
1180   ! Draw the scope grid on the terminal screen.
1190   !
1200   !
1210   ! Draw 9 horizontal lines from (0,70) to (1020,70),
1220   ! then increment 80 for y dimension.
1230   !
1240     X1$=" @"
1250     X2$="?→"
1260     Y=70
1270   !
1280     For i=1 to 9
1290      Ytemp=y
```

```
1300    Gosub Convert
1310  ! Enter graphics mode.
1320    Gs$=chr$(29)
1330  ! Draw the line.
1340    Print gs$;y$;x1$;x2$;
1350    Y=y+80
1360    Next i
1370  !
1380  ! Change back to alphanumeric mode.
1390    Print chr$(31)
1400  !
1410    Y1$=chr$(34)&chr$(102)
1420    Y2$="6f"
1430    X=0
1440    For i=1 to 11
1450    Xtemp=x
1460    Gosub Convert
1470    Print gs$;y1$;x$;y2$;x$;
1480    X=x+102
1490    Next i
1500  !
1510  !
1520  ! Now call the plot routine to plot the curve data of
1530  ! waveform no. 1. All data points are already in array.
1540  !
1550    Gosub Plot
1560  !
1570  ! Position the cursor to print waveform ID no. 1.
1580    Print gs$;chr$(55);chr$(127);"%∧";
1590  ! Print waveform ID no. 1.
1600    Print chr$(31);chr$(10);
1610    Print chcoup1$;"      ";xunit1$;"      ";yunit1$
1620  !
1630  ! If just one waveform is sent, then done.
1640    If Numcur=1 then goto Done.
1650  !
1660    For i=1 to 1027
1670  ! Now, manipulate the data for waveform no. 2 and
1680  ! put it in an array.
1690    Point(i)=asc(seg$(curve2$,i,1))
1700    Next i
1710  !
1720  ! Call the Plot subroutine to plot waveform no. 2.
1730  !
1740    Gosub Plot
1750  !
1760  ! Position the cursor to print waveform ID no. 2.
1770    Print gs$;" ∨";"%∧";
1780    Print chr$(31)
1790  !
1800  ! Print waveform ID no. 2.
1810    Print chcoup2$;"      ";xunit2$;"      ";yunit2$
1820  !
1830 Done: ! Abort the program.
1840  !
1850  ! Postion the cursor to (0,0).
1860    Print gs$;" ";chr$(96);" @";
1870  ! Place in alphanumeric mode.
1880    Print chr$(31);
1890  !
```

```
1900   ! Program ended.
1910     Stop
1920   !
1930   !
1940 Plot: ! Subroutine to draw the waveform curve.
1950   !
1960     Print gs$;
1970     X=0
1980     For i=3 to 1022
1990      Ytemp=point(i)*3.4+10
2000   !
2010   !
2020   !
2030     Xtemp=x
2040     Gosub Convert
2050   !
2060     X=x+1
2070   !
2080     Print y$;x$;
2090     Next i
2100     Print chr$(31)
2110     Return
2120   !
2130   !
2140 Nowfm: ! Routine to handle the case of no waveform. If no
2150   ! waveform is transferred, then print header and abort the program.
2160     Print "THERE IS NO WAVEFORM DATA TO TRANSFER."
2170     Print ""
2180     Print a$
2190     Stop
2200   !
2210 Onecurve: ! Routine to handle a one-waveform transfer.
2220   !
2230   ! If there in only one curve, then copy the data until <CRLF>.
2240   !
2250     Semi1=pos(a$,chr$(13)&chr$(10),1)
2260   !
2270   ! Set the Numcur flag to 1 to indicate that there is only one
2280   ! curve to transfer before returning to main program.
2290     Numcur=1
2300     Return
2310   !
2320   !
2330   !
2340 Convert: ! Convert xtemp and y temp to x$ and y$ where x$
2350   ! and y$ each contain two bytes (high & low) for its position.
2360   !
2370   ! This routine breaks ytemp and/or xtemp into 10-bit binary
2380   ! numbers and then into two five-bit numbers. Tag two bits 01
2390   ! into the higher five bits to make a seven-bit number for the
2400   ! high byte. Tag two bits 10 (for x) or 11 (for y) to complete
2410   ! the low-byte number of x or y.
2420   !
2430   ! Mask all the bits except the last five to zero.
2440     Ytemp1=ytemp band 31
2450   ! Tag 11 into the front of this five-bit number.
2460     Ytemp1=ytemp1 bor 96
2470   ! Ytemp1 is ascii of the low byte of y
2480     Ylow$=chr$(ytemp1)
2490   !
```

```
2500   ! Mask out all bits except 5 to 9 (five bits for the high byte).
2510     Ytemph=ytemp band 992
2520   ! Divide by 32 to shift right five times.
2530     Ytemph=ytemph/32
2540   ! Tag 01 in front of it to make it a seven-bit number.
2550   ! Present for the ascii of the high byte of y position.
2560     Ytemph=ytemph bor 32
2570     Yhigh$=chr$(ytemph)
2580     Y$=yhigh$&ylow$
2590   ! Y$ now contains two bytes for the y position.
2600   !
2610   ! Converting xtemp is similar to ytemp except that 10 will
2620   ! be tagged to the low byte of x position instead of 11 for
2630   ! the y position.
2640     Xtempl=xtemp band 31
2650     Xtempl=xtempl bor 64
2660     Xlow$=chr$(xtempl)
2670   !
2680     Xtemph=xtemp band 992
2690     Xtemph=xtemph/32
2700     Xtemph=xtemph bor 32
2710     Xhigh$=chr$(xtemph)
2720     X$=xhigh$&xlow$
2730   ! x$ now contains two bytes for x position.
2740     Return
3000 Srqhdl: ! Routine to handle the srq.
3010     Poll stb,dev;val(addr$)
3020     Print "STATUS BYTE IS :";stb
3030     Resume
```

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

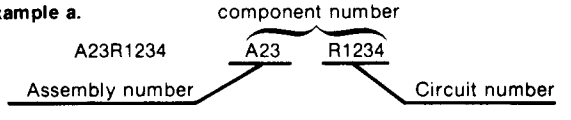
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

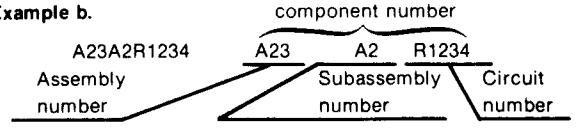
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
0000M	SONY/TEKTRONIX CORPORATION	P O BOX 14, HANEDA AIRPORT	TOKYO 149, JAPAN
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC. SEMICONDUCTOR GROUP	P.O. BOX 5012	DALLAS, TX 75222
02735	RCA CORPORATION, SOLID STATE DIVISION	ROUTE 202	SOMERVILLE, NY 08876
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
05397	UNION CARBIDE CORPORATION, MATERIALS SYSTEMS DIVISION	11901 MADISON AVENUE	CLEVELAND, OH 44101
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
15454	RODAN INDUSTRIES, INC.	2905 BLUE STAR ST.	ANAHEIM, CA 92806
17856	SILICONIX, INC.	2201 LAURELWOOD DRIVE	SANTA CLARA, CA 95054
18518	MSI ELLCTRONICS INC.	34-32 57TH ST	WOODSIDE, NY 11377
24546	CORNING GLASS WORKS, ELECTRONIC COMPONENTS DIVISION	550 HIGH STREET	BRADFORD, PA 16701
24931	SPECIALITY CONNECTOR CO., INC.	2620 ENDRESS PLACE	GREENWOOD, IN 46142
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
31918	IEE/SCHADOW INC.	8081 WALLACE ROAD	EDEN PRAIRIE, MN 55343
50157	MIDWEST COMPONENTS INC.	P. O. BOX 787 1981 PORT CITY BLVD.	MUSKEGON, MI 49443
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
56708	ZILOG INC.	14060 BUBB RD.	CUPERTINO, CA 95014
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
59821	CENTRALAB INC SUB NORTH AMERICAN PHILIPS CORP	7158 MERCHANT AVE	EL PASO, TX 79915
71279	CAMBRIDGE THERMIONIC CORP.	445 CONCORD AVE.	CAMBRIDGE, MA 02138
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
74970	JOHNSON, E. F., CO.	299 10TH AVE. S. W.	WASECA, MN 56093
77820	BENDIX CORP., THE, ELECTRICAL COMPONENTS DIVISION	SHERMAN AVE.	SIDNEY, NY 13838
78488	STACKPOLE CARBON CO.		ST. MARYS, PA 15857
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
95121	QUALITY COMPONENTS, INC.	P O BOX 113	ST. MARYS, PA 15857
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO, CA 91341
T0020	UNITED CHEMI-CON INC.	1128 LEXINGTON AUVE.	ROCHESTER, NY 14606

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-8099-00	.300101	.300340	CKT BOARD ASSY:MAIN	0000M	670-8099-00
A1	670-8099-01	.300341		CKT BOARD ASSY:MAIN	0000M	670-8099-01
A2	670-8098-00	.300101	.300340	CKT BOARD ASSY:TRIGGER	0000M	670-8098-00
A2	670-8098-01	.300341		CKT BOARD ASSY:TRIGGER	0000M	670-8098-01
A3	670-8097-00	.300101	.300340	CKT BOARD ASSY:SWEEP	0000M	670-8097-00
A3	670-8097-01	.300341		CKT BOARD ASSY:SWEEP	0000M	670-8097-01
A4	670-8096-00	.300101	.300340	CKT BOARD ASSY:CONTROL	0000M	670-8096-00
A4	670-8096-01	.300341		CKT BOARD ASSY:CONTROL	0000M	670-8096-01
A5	670-8086-00			CKT BOARD ASSY:ACQUISITION	0000M	670-8086-00
A6	670-8088-00	.300101	.300340	CKT BOARD ASSY:DISPLAY	0000M	670-8088-00
A6	670-8088-01	.300341		CKT BOARD ASSY:DISPLAY	0000M	670-8088-01
A7	670-8087-00	.300101	.300340	CKT BOARD ASSY:CPU	0000M	670-8087-00
A7	670-8087-01	.300341		CKT BOARD ASSY:CPU	0000M	670-8087-01
A8	670-8136-00			CKT BOARD ASSY:OPTION	0000M	670-8136-00
A9	670-8095-00			CKT BOARD ASSY:MOTHER KEYBOARD	0000M	670-8095-00
A10	670-8094-00			CKT BOARD ASSY:KEYBOARD	0000M	670-8094-00
A11	670-8093-00			CKT BOARD ASSY:VERTICAL OUTPUT	0000M	670-8093-00
A12	670-8092-00	.300100	.300340	CKT BOARD ASSY:HORIZONTAL OUTPUT	0000M	670-8092-00
A12	670-8092-01	.300341		CKT BOARD ASSY:HORIZONTAL OUTPUT	0000M	670-8092-01
A13	670-8091-00			CKT BOARD ASSY:DC/DC CONVERTER	0000M	670-8091-00
A14	670-8090-00	.300100	.300340	CKT BOARD ASSY:PRIMARY	0000M	670-8090-00
A14	670-8090-01	.300341		CKT BOARD ASSY:PRIMARY	0000M	670-8090-01
A15	670-8089-00	.300100	.300340	CKT BOARD ASSY:HIGH VOLTAGE	0000M	670-8089-00
A15	670-8089-01	.300341		CKT BOARD ASSY:HIGH VOLTAGE	0000M	670-8089-01
A19	388-7593-00			CKT BOARD ASSY:ATTENUATOR	0000M	388-7593-00
A19	----- -----			(NO ELECTRICAL PARTS)		
A20	388-7593-00			CKT BOARD ASSY:ATTENUATOR	0000M	388-7593-00
A20	----- -----			(NO ELECTRICAL PARTS)		
.						
.						
A1	670-8099-00	.300100	.300340	CKT BOARD ASSY:MAIN	0000M	670-8099-00
A1	670-8099-01	.300341		CKT BOARD ASSY:MAIN	0000M	670-8099-01
.						
A1C2	----- -----			(SELECTED)		
A1C2	283-0329-00			CAP.,FXD,CER DI:0.39PF,10%,500V	0000M	283-0329-00
A1C2	281-0537-00			CAP.,FXD,CER DI:0.68PF,20%,600V	95121	OC-.68MM 20%
A1C2	283-0240-00			CAP.,FXD,CER DI:1PF,20%,500V	56289	53C141
A1C3	285-0560-00			CAP.,FXD,PLASTIC:0.022UF,10%,630V	0000M	285-0560-00
A1C10	281-0237-00			CAP.,VAR,CER DI:3.3-18PF,250V	0000M	281-0237-00
A1C12	281-0138-00			CAP.,VAR,PLSTC:0.4-1.2PF,600V	74970	1890509075
A1C14	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C20	281-0260-00			CAP.,VAR,CER DI:1.3-3PF		
A1C22	281-0236-00			CAP.,VAR,CER DI:2.8-10PF,250V	0000M	281-0236-00
A1C24	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A1C32	283-0005-00			CAP.,FXD,CER DI:0.01UF,+100-0%,250V	72982	8131N300Z5U0103P
A1C39	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C40	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C50	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	55680	ULA1A01TEA
A1C51	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A1C90	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	55680	ULA1A01TEA
A1C100	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	55680	ULA1A01TEA
A1C102	281-0237-00			CAP.,VAR,CER DI:3.3-18PF,250V	0000M	281-0237-00
A1C133	281-0906-00			CAP.,NTWK,FXD:(4)0.01UF,10%,25V		
A1C148	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1C149	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C170	281-0906-00			CAP.,NTWK,FXD:(4)0.01UF,10%,25V		
A1C195	281-0237-00			CAP.,VAR,CER DI:3.3-18PF,250V	0000M	281-0237-00
A1C302	281-0138-00			CAP.,VAR,PLSTC:0.4-1.2PF,600V	74970	1890509075
A1C303	285-0560-00			CAP.,FXD,PLASTIC:0.022UF,10%,630V	0000M	285-0560-00
A1C310	281-0237-00			CAP.,VAR,CER DI:3.3-18PF,250V	0000M	281-0237-00
A1C312	281-0138-00			CAP.,VAR,PLSTC:0.4-1.2PF,600V	74970	1890509075
A1C314	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C320	281-0260-00			CAP.,VAR,CER DI:1.3-3PF		
A1C322	281-0236-00			CAP.,VAR,CER DI:2.8-10PF,250V	0000M	281-0236-00
A1C324	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A1C332	283-0005-00			CAP.,FXD,CER DI:0.01UF,+100-0%,250V	72982	8131N300Z5U0103P
A1C339	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C339	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C340	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C400	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	55680	ULA1A01TEA
A1C402	281-0237-00			CAP.,VAR,CER DI:3.3-18PF,250V	0000M	281-0237-00
A1C434	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C436	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C494	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A1C700	283-0329-00			CAP.,FXD,CER DI:0.39PF,10%,500V	0000M	283-0329-00
A1C720	283-0329-00			CAP.,FXD,CER DI:0.39PF,10%,500V	0000M	283-0329-00
A1C734	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C744	281-0242-00			CAP.,VAR,CER DI:1.5-5.5PF,250V		
A1C766	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A1C813	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C814	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A1C815	283-0154-00			CAP.,FXD,CER DI:22PF,5%,50V	72982	8111B061C0G220J
A1C816	281-0260-00			CAP.,VAR,CER DI:1.3-3PF		
A1C848	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	55680	ULA1A01TEA
A1C901	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C904	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	55680	ULA1A01TEA
A1C906	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	55680	ULA1A01TEA
A1C908	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	55680	ULA1A01TEA
A1C910	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C912	281-0237-00			CAP.,VAR,CER DI:3.3-18PF,250V	0000M	281-0237-00
A1C914	281-0242-00			CAP.,VAR,CER DI:1.5-5.5PF,250V		
A1C916	281-0260-00			CAP.,VAR,CER DI:1.3-3PF		
A1C980	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C982	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A1CR32	152-0323-03			SEMICOND DEVICE:SIG,SI,BAX 13	0000M	152-0323-03
A1CR332	152-0323-03			SEMICOND DEVICE:SIG,SI,BAX 13	0000M	152-0323-03
A1CR818	152-0612-00			SEMICOND DEVICE:V VAR CAP.,4V,17.5PF	18518	152-0612-00
A1CR819	152-0612-00			SEMICOND DEVICE:V VAR CAP.,4V,17.5PF	18518	152-0612-00
A1CR834	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR836	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1J1	131-0679-02			CONNECTOR,RCPT,:BNC,MALE,3 CONTACT	24931	28JR270-1
A1J301	131-0679-02			CONNECTOR,RCPT,:BNC,MALE,3 CONTACT	24931	28JR270-1
A1K3	148-0151-00			RELAY,REED:250 OHM,10%,5V	0000M	148-0151-00
A1K4	148-0152-00			RELAY,REED:200 OHM	0000M	148-0152-00
A1K10	148-0154-00			RELAY,REED:200 OHM	0000M	148-0154-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1K20	148-0152-00			RELAY,REED:200 OHM	0000M	148-0152-00
A1K22	148-0154-00			RELAY,REED:200 OHM	0000M	148-0154-00
A1K31	148-0153-00			RELAY,REED:250 OHM,10%,5V	0000M	148-0153-00
A1K303	148-0151-00			RELAY,REED:250 OHM,10%,5V	0000M	148-0151-00
A1K304	148-0152-00			RELAY,REED:200 OHM	0000M	148-0152-00
A1K310	148-0154-00			RELAY,REED:200 OHM	0000M	148-0154-00
A1K320	148-0152-00			RELAY,REED:200 OHM	0000M	148-0152-00
A1K322	148-0154-00			RELAY,REED:200 OHM	0000M	148-0154-00
A1K331	148-0153-00			RELAY,REED:250 OHM,10%,5V	0000M	148-0153-00
A1L10	108-1195-00			COIL,RF:FIXED,10UH	0000M	108-1195-00
A1L90	108-1193-00			COIL,RF:FIXED,100UH	0000M	108-1193-00
A1L100	108-1193-00			COIL,RF:FIXED,100UH	0000M	108-1193-00
A1L400	108-1193-00			COIL,RF:FIXED,100UH	0000M	108-1193-00
A1P910	131-3024-00			CONN,RCPT,ELEC:EDGECARD,STRAIGHT 2 X 10	0000M	131-3024-00
A1P920	131-3024-00			CONN,RCPT,ELEC:EDGECARD,STRAIGHT 2 X 10	0000M	131-3024-00
A1P930	131-3024-00			CONN,RCPT,ELEC:EDGECARD,STRAIGHT 2 X 10	0000M	131-3024-00
A1P940	131-3024-00			CONN,RCPT,ELEC:EDGECARD,STRAIGHT 2 X 10	0000M	131-3024-00
A1P950	131-3024-00			CONN,RCPT,ELEC:EDGECARD,STRAIGHT 2 X 10	0000M	131-3024-00
A1P960	131-3024-00			CONN,RCPT,ELEC:EDGECARD,STRAIGHT 2 X 10	0000M	131-3024-00
A1Q40	151-1032-00			TRANSISTOR:SILICON,FET,DUAL	17856	DN399
A1Q144	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q156	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q190	153-0656-00			TRANSISTOR:SELECTED,MATCHED	0000M	153-0656-00
A1Q230	153-0656-00			TRANSISTOR:SELECTED,MATCHED	0000M	153-0656-00
A1Q340	151-1032-00			TRANSISTOR:SILICON,FET,DUAL	17856	DN399
A1Q444	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q456	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q800	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q820	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A1Q830	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A1Q832	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A1Q840	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A1Q842	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A1R1	307-0452-00			RES.,FXD,FUSIBLE:47 OHM,5%,0.25W		
A1R3	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A1R11	313-0391-00			RES.,FXD,FILM:390 OHM,5%,0.166W	0000M	313-0391-00
A1R12	321-0790-01			RES.,FXD,FILM:990K OHM,0.5%,0.125W	91637	HFF1104G99002D
A1R13	----- -----			(SELECTED)		
A1R13	313-0100-00			RES.,FXD,FILM: 100 OHM,5%,0.166W	0000M	313-0100-00
A1R13	313-0150-00			RES.,FXD,FILM: 15 OHM,5%,0.166W	0000M	313-0150-00
A1R13	313-0200-00	.300101	.300200	RES.,FXD,FILM: 20 OHM,5%,0.166W	0000M	313-0200-00
A1R13	313-0220-00	.300101	.300200	RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A1R13	313-0240-00	.300101	.300200	RES.,FXD,FILM: 24 OHM,5%,0.166W	0000M	313-0240-00
A1R14	321-1289-01			RES.,FXD,FILM:10.1K OHM,0.5%,0.125W	91637	MFF1816G10101D
A1R15	313-0360-00			RES.,FXD,FILM:36 OHM,5%,0.166W	0000M	313-0360-00
A1R17	313-0301-00	.300101	.300125	RES.,FXD,FILM:300 OHM,5%,0.166W	0000M	313-0301-00
A1R17	313-0201-00	.300126		RES.,FXD,FILM: 200 OHM,5%,0.166W	0000M	313-0201-00
A1R18	----- -----			(SELECTED)		
A1R18	313-0100-00			RES.,FXD,FILM: 100 OHM,5%,0.166W	0000M	313-0100-00
A1R18	313-0150-00			RES.,FXD,FILM: 15 OHM,5%,0.166W	0000M	313-0150-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1R22	321-0807-01			RES.,FXD,FILM:900K OHM,0.5%,0.125W	91637	MFF1816G90002D
A1R23	313-0360-00			RES.,FXD,FILM:36 OHM,5%,0.166W	0000M	313-0360-00
A1R24	321-0389-01	.300101	.300200	RES.,FXD,FILM:110K OHM,0.5%,0.125W	91637	MFF1816G11002D
A1R24	321-1389-01	.300201		RES.,FXD,FILM:111K OHM,0.5%,0.125W	91637	MFF1816G11102D
A1R25	313-0101-00	.300101	.300125	RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A1R25	313-0100-00	.300126		RES.,FXD,FILM: 100 OHM,5%,0.166W	0000M	313-0100-00
A1R30	321-0481-01			RES.,FXD,FILM:1M OHM,0.5%,0.125W	91637	MFF1816G10003D
A1R32	313-0334-00			RES.,FXD,FILM:330K OHM,5%,0.166W	0000M	313-0334-00
A1R34	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A1R40	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A1R42	326-0001-00			RES.,FXD,FILM:22 OHM,1%,0.166W	0000M	326-0001-00
A1R48	326-0001-00			RES.,FXD,FILM:22 OHM,1%,0.166W	0000M	326-0001-00
A1R100	326-0010-00			RES.,FXD,FILM:470 OHM,1%,0.166W	0000M	326-0010-00
A1R102	311-0635-04			RES.,VAR,NONWIR:1K OHM,20%,0.5W	0000M	311-0735-04
A1R104	326-0005-00	.300101	.300125	RES.,FXD,FILM:160 OHM,1%,0.166W		
A1R104	326-0007-00	.300126		RES.,FXD,FILM:240 OHM,1%,0.166W	0000M	326-0007-00
A1R105	326-0013-00	.300101	.300125	RES.,FXD,FILM:1K OHM,1%,0.166W	0000M	326-0013-00
A1R105	326-0005-00	.300126		RES.,FXD,FILM:160 OHM,1%,0.166W		
A1R108	311-2041-00	.300101	.300125	RES.,VAR,NONWIR:CKT BD,10K OHM,10%,0.5W	0000M	311-2041-00
A1R108	311-0635-04	.300126		RES.,VAR,NONWIR:1K OHM,20%,0.5W	0000M	311-0735-04
A1R110	326-0010-00			RES.,FXD,FILM:470 OHM,1%,0.166W	0000M	326-0010-00
A1R118	311-2041-00			RES.,VAR,NONWIR:CKT BD,10K OHM,10%,0.5W	0000M	311-2041-00
A1R120	326-0030-00			RES.,FXD,FILM:7.5K OHM,1%,0.166W	0000M	326-0030-00
A1R122	326-0003-00			RES.,FXD,FILM:100 OHM,1%,0.166W	0000M	326-0003-00
A1R131	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A1R133	313-0162-00			RES.,FXD,FILM:1.6K OHM,5%,0.166W	0000M	313-0162-00
A1R140	326-0008-00			RES.,FXD,FILM:200 OHM,1%,0.166W	0000M	326-0008-00
A1R144	326-0008-00			RES.,FXD,FILM:200 OHM,1%,0.166W	0000M	326-0008-00
A1R148	326-0009-00			RES.,FXD,FILM:330 OHM,1%,0.166W	0000M	326-0009-00
A1R150	326-0029-00			RES.,FXD,FILM:1.3K OHM,1%,0.166W	0000M	326-0029-00
A1R151	311-2041-00			RES.,VAR,NONWIR:CKT BD,10K OHM,10%,0.5W	0000M	311-2041-00
A1R152	326-0014-00			RES.,FXD,FILM:1.2K OHM,1%,0.166W	0000M	326-0014-00
A1R153	313-0153-00			RES.,FXD,FILM: 15K OHM,5%,0.166W	0000M	313-0153-00
A1R156	326-0009-00			RES.,FXD,FILM:330 OHM,1%,0.166W		
A1R160	307-0926-00			RES.,NTWK,FXD FI:(2)400,(3)200,(2)100 OHM		
A1R161	313-0432-00			RES.,FXD,FILM:4.3K OHM,5%,0.166W	0000M	313-0432-00
A1R164	311-0609-03			RES.,VAR,NONWW:2K OHM,20%,0.5W	0000M	311-0609-03
A1R170	313-0681-00			RES.,FXD,FILM:680 OHM,5%,0.166W	0000M	313-0681-00
A1R171	313-0681-00			RES.,FXD,FILM:680 OHM,5%,0.166W	0000M	313-0681-00
A1R172	313-0681-00			RES.,FXD,FILM:680 OHM,5%,0.166W	0000M	313-0681-00
A1R174	313-0222-00			RES.,FXD,FILM:2.2K OHM,5%,0.166W	0000M	313-0222-00
A1R190	326-0012-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	326-0012-00
A1R196	326-0002-00			RES.,FXD,FILM:62 OHM,1%,0.166W	0000M	326-0002-00
A1R200	326-0007-00			RES.,FXD,FILM:240 OHM,1%,0.166W	0000M	326-0007-00
A1R202	326-0002-00			RES.,FXD,FILM:62 OHM,1%,0.166W	0000M	326-0002-00
A1R210	326-0006-00			RES.,FXD,FILM:220 OHM,1%,0.166W	0000M	326-0006-00
A1R214	307-0925-00			RES.,NTWK,FXD FI:(2)470 OHM,(1)330 OHM,5%	0000M	307-0925-00
A1R215	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A1R217	311-2041-00			RES.,VAR,NONWIR:CKT BD,10K OHM,10%,0.5W	0000M	311-2041-00
A1R220	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A1R230	326-0012-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	326-0012-00
A1R240	326-0006-00			RES.,FXD,FILM:220 OHM,1%,0.166W	0000M	326-0006-00
A1R301	307-0452-00			RES.,FXD,FUSIBLE:47 OHM,5%,0.25W		
A1R303	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1R312	321-0790-01			RES.,FXD,FILM:990K OHM,0.5%,0.125W	91637	HFF1104G99002D
A1R313	----- -----			(SELECTED)		
A1R313	313-0100-00			RES.,FXD,FILM: 100 OHM,5%,0.166W	0000M	313-0100-00
A1R313	313-0150-00			RES.,FXD,FILM: 15 OHM,5%,0.166W	0000M	313-0150-00
A1R313	313-0200-00	.300101	.300200	RES.,FXD,FILM: 20 OHM,5%,0.166W	0000M	313-0200-00
A1R313	313-0220-00	.300101	.300200	RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A1R313	313-0240-00	.300101	.300200	RES.,FXD,FILM: 24 OHM,5%,0.166W	0000M	313-0240-00
A1R314	321-1289-01			RES.,FXD,FILM:10.1K OHM,0.5%,0.125W	91637	MFF1816G10101D
A1R315	313-0360-00			RES.,FXD,FILM:36 OHM,5%,0.166W	0000M	313-0360-00
A1R317	313-0301-00	.300101	.300125	RES.,FXD,FILM:300 OHM,5%,0.166W	0000M	313-0301-00
A1R317	313-0201-00	.300126		RES.,FXD,FILM: 200 OHM,5%,0.166W	0000M	313-0201-00
A1R318	----- -----			(SELECTED)		
A1R318	313-0100-00			RES.,FXD,FILM: 100 OHM,5%,0.166W	0000M	313-0100-00
A1R318	313-0150-00			RES.,FXD,FILM: 15 OHM,5%,0.166W	0000M	313-0150-00
A1R322	321-0807-01			RES.,FXD,FILM:900K OHM,0.5%,0.125W	91637	MFF1816G90002D
A1R323	313-0360-00			RES.,FXD,FILM:36 OHM,5%,0.166W	0000M	313-0360-00
A1R324	321-0389-01	.300101	.300200	RES.,FXD,FILM:110K OHM,0.5%,0.125W	91637	MFF1816G11002D
A1R324	321-1389-01	.300201		RES.,FXD,FILM:111K OHM,0.5%,0.125W	91637	MFF1816G11102D
A1R325	313-0101-00	.300101	.300125	RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A1R325	313-0100-00	.300126		RES.,FXD,FILM: 100 OHM,5%,0.166W	0000M	313-0100-00
A1R330	321-0481-01			RES.,FXD,FILM:1M OHM,0.5%,0.125W	91637	MFF1816G10003D
A1R332	313-0334-00			RES.,FXD,FILM:330K OHM,5%,0.166W	0000M	313-0334-00
A1R334	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A1R338	307-0912-00			RES.,NTWK,FXD FI:(6)10K OHM,5%,0.125W	0000M	307-0912-00
A1R340	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A1R342	326-0001-00			RES.,FXD,FILM:22 OHM,1%,0.166W	0000M	326-0001-00
A1R348	326-0001-00			RES.,FXD,FILM:22 OHM,1%,0.166W	0000M	326-0001-00
A1R400	326-0010-00			RES.,FXD,FILM:470 OHM,1%,0.166W	0000M	326-0010-00
A1R402	311-0635-04			RES.,VAR,NONWIR:1K OHM,20%,0.5W	0000M	311-0735-04
A1R404	326-0004-00			RES.,FXD,FILM:150 OHM,1%,0.166W	0000M	326-0004-00
A1R410	326-0010-00			RES.,FXD,FILM:470 OHM,1%,0.166W	0000M	326-0010-00
A1R418	311-2041-00			RES.,VAR,NONWIR:CKT BD,10K OHM,10%,0.5W	0000M	311-2041-00
A1R420	326-0030-00			RES.,FXD,FILM:7.5K OHM,1%,0.166W	0000M	326-0030-00
A1R422	326-0003-00			RES.,FXD,FILM:100 OHM,1%,0>166W	0000M	326-0003-00
A1R431	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A1R433	313-0162-00	.300101	.300125	RES.,FXD,FILM:1.6K OHM,5%,0.166W	0000M	313-0162-00
A1R433	313-0132-00	.300126		RES.,FXD,FILM: 1.3K OHM,5%,0.166W	0000M	313-0132-00
A1R440	326-0008-00			RES.,FXD,FILM:200 OHM,1%,0.166W	0000M	326-0008-00
A1R444	326-0008-00			RES.,FXD,FILM:200 OHM,1%,0.166W	0000M	326-0008-00
A1R448	326-0009-00			RES.,FXD,FILM:330 OHM,1%,0.166W	0000M	326-0009-00
A1R451	311-2041-00			RES.,VAR,NONWIR:CKT BD,10K OHM,10%,0.5W	0000M	311-2041-00
A1R453	313-0153-00			RES.,FXD,FILM: 15K OHM,5%,0.166W	0000M	313-0153-00
A1R456	326-0009-00			RES.,FXD,FILM:330 OHM,1%,0.166W	0000M	326-0009-00
A1R460	307-0926-00			RES.,NTWK,FXD FI:(2)400 OHM,(3) 200 OHM		
A1R461	313-0432-00			RES.,FXD,FILM:4.3K OHM,5%,0.166W	0000M	313-0432-00
A1R464	311-0609-03			RES.,VAR,NONWW:2K OHM,20%,0.5W	0000M	311-0609-03
A1R470	313-0681-00			RES.,FXD,FILM:680 OHM,5%,0.166W	0000M	313-0681-00
A1R471	313-0681-00			RES.,FXD,FILM:680 OHM,5%,0.166W	0000M	313-0681-00
A1R472	313-0681-00			RES.,FXD,FILM:680 OHM,5%,0.166W	0000M	313-0681-00
A1R474	313-0222-00			RES.,FXD,FILM:2.2K OHM,5%,0.166W	0000M	313-0222-00
A1R490	326-0012-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	326-0012-00
A1R496	326-0002-00			RES.,FXD,FILM:62 OHM,1%,0.166W	0000M	326-0002-00
A1R500	326-0007-00			RES.,FXD,FILM:240 OHM,1%,0.166W	0000M	326-0007-00
A1R502	326-0002-00			RES.,FXD,FILM:62 OHM,1%,0.166W	0000M	326-0002-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1R510	326-0006-00			RES.,FXD,FILM:220 OHM,1%,0.166W	0000M	326-0006-00
A1R514	307-0925-00			RES.,NTWK,FXD FI:(2)470 OHM,(1)330 OHM,5%	0000M	307-0925-00
A1R520	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A1R530	326-0012-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	326-0012-00
A1R540	326-0006-00			RES.,FXD,FILM:220 OHM,1%,0.166W	0000M	326-0006-00
A1R702	307-0925-00			RES.,NTWK,FXD FI:(2)470 OHM,(1)330 OHM,5%	0000M	307-0925-00
A1R712	313-0202-00			RES.,FXD,FILM: 2K OHM,5%,0.166W	0000M	313-0202-00
A1R713	313-0391-00			RES.,FXD,FILM:390 OHM,5%,0.166W	0000M	313-0391-00
A1R714	313-0202-00			RES.,FXD,FILM: 2K OHM,5%,0.166W	0000M	313-0202-00
A1R715	313-0152-00			RES.,FXD,FILM:1.5K OHM,5%,0.166W	0000M	313-0152-00
A1R722	307-0925-00			RES.,NTWK,FXD FI:(2)470 OHM,(1)330 OHM,5%	0000M	307-0925-00
A1R734	326-0006-00			RES.,FXD,FILM:220 OHM,1%,0.166W	0000M	326-0006-00
A1R736	326-0006-00			RES.,FXD,FILM:220 OHM,1%,0.166W	0000M	326-0006-00
A1R740	313-0510-00			RES.,FXD,FILM: 51 OHM,5%,0.166W	0000M	313-0510-00
A1R741	313-0510-00			RES.,FXD,FILM: 51 OHM,5%,0.166W	0000M	313-0510-00
A1R742	313-0620-00			RES.,FXD,FILM: 62 OHM,5%,0.166W	0000M	313-0620-00
A1R744	307-0925-00			RES.,NTWK,FXD FI:(2)470 OHM,(1)330 OHM,5%	0000M	307-0925-00
A1R746	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A1R750	313-0620-00			RES.,FXD,FILM: 62 OHM,5%,0.166W	0000M	313-0620-00
A1R766	313-0621-00			RES.,FXD,FILM:620 OHM,5%,0.166W	0000M	313-0621-00
A1R768	313-0222-00			RES.,FXD,FILM:2.2K OHM,5%,0.166W	0000M	313-0222-00
A1R800	326-0006-00			RES.,FXD,FILM:220 OHM,1%,0.166W	0000M	326-0006-00
A1R801	313-0182-00			RES.,FXD,FILM:2K OHM,5%,0.166W	0000M	313-0182-00
A1R802	313-0221-00			RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A1R808	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A1R812	313-0563-00			RES.,FXD,FILM:56K OHM,5%,0.166W	0000M	313-0563-00
A1R813	313-0104-00			RES.,FXD,FILM:100K OHM,5%,0.166W	0000M	313-0104-00
A1R814	313-0163-00			RES.,FXD,FILM:16K OHM,5%,0.166W	0000M	313-0163-00
A1R816	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A1R818	313-0164-00			RES.,FXD,FILM:160K OHM,5%,0.166W	0000M	313-0164-00
A1R820	326-0006-00			RES.,FXD,FILM:220 OHM,1%,0.166W	0000M	326-0006-00
A1R822	313-0221-00			RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A1R824	313-0471-00			RES.,FXD,FILM:470 OHM,5%,0.166W	0000M	313-0471-00
A1R826	313-0471-00			RES.,FXD,FILM:470 OHM,5%,0.166W	0000M	313-0471-00
A1R830	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A1R832	313-0680-00			RES.,FXD,FILM:68 OHM,5%,0.166W	0000M	313-0680-00
A1R834	313-0470-00			RES.,FXD,FILM:47 OHM,5%,0.166W	0000M	313-0470-00
A1R836	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A1R837	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A1R840	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A1R842	313-0680-00			RES.,FXD,FILM:68 OHM,5%,0.166W	0000M	313-0680-00
A1R844	313-0470-00			RES.,FXD,FILM:47 OHM,5%,0.166W	0000M	313-0470-00
A1R846	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A1R847	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A1R848	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A1R900	326-0026-00			RES.,FXD,FILM:82K OHM,1%,0.166W	0000M	326-0026-00
A1R906	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A1R908	307-0452-00			RES.,FXD,FUSIBLE:47 OHM,5%,0.25W		
A1R916	321-0466-00			RES.,FXD,FILM:698K OHM,1%,0.125W	91637	MFF1816G69802F
A1R917	313-0244-00			RES.,FXD,FILM:240K OHM,5%,0.166W	0000M	313-0244-00
A1R918	321-0446-00			RES.,FXD,FILM:432K OHM,1%,0.125W	91637	MFF1816G43202F
A1R919	313-0201-00			RES.,FXD,FILM: 200 OHM,5%,0.166W	0000M	313-0201-00
A1R920	311-0635-04			RES.,VAR,NONWIR:1K OHM,20%,0.5W	0000M	311-0735-04
A1R921	313-0132-00			RES.,FXD,FILM: 1.3K OHM,5%,0.166W	0000M	313-0132-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1R922	313-0132-00			RES.,FXD,FILM: 1.3K OHM,5%,0.166W	0000M	313-0132-00
A1R923	313-0132-00			RES.,FXD,FILM: 1.3K OHM,5%,0.166W	0000M	313-0132-00
A1R924	311-0635-04			RES.,VAR,NONWIR:1K OHM,20%,0.5W	0000M	311-0735-04
A1R925	313-0132-00			RES.,FXD,FILM: 1.3K OHM,5%,0.166W	0000M	313-0132-00
A1R926	311-0609-03			RES.,VAR,NONWW:2K OHM,20%,0.5W	0000M	311-0609-03
A1R970	313-0431-00			RES.,FXD,FILM:430 OHM,5%,0.166W	0000M	313-0431-00
A1R971	313-0431-00			RES.,FXD,FILM:430 OHM,5%,0.166W	0000M	313-0431-00
A1R972	313-0331-00			RES.,FXD,FILM: 330 OHM,5%,0.166W	0000M	313-0331-00
A1R974	313-0431-00			RES.,FXD,FILM:430 OHM,5%,0.166W	0000M	313-0431-00
A1R975	313-0431-00			RES.,FXD,FILM:430 OHM,5%,0.166W	0000M	313-0431-00
A1R976	313-0331-00			RES.,FXD,FILM: 330 OHM,5%,0.166W	0000M	313-0331-00
A1R982	313-0104-00			RES.,FXD,FILM:100K OHM,5%,0.166W	0000M	313-0104-00
A1R984	313-0164-00			RES.,FXD,FILM:160K OHM,5%,0.166W	0000M	313-0164-00
A1R986	313-0104-00			RES.,FXD,FILM:100K OHM,5%,0.166W	0000M	313-0104-00
A1R988	313-0104-00			RES.,FXD,FILM:100K OHM,5%,0.166W	0000M	313-0104-00
A1R992	311-0633-02			RES.,VAR,NONWIR:5K OHM,0.50W	0000M	311-0633-02
A1R994	326-0019-00			RES.,FXD,FILM:4.7K OHM,1%,0.166W	0000M	326-0019-00
A1RT107	313-0242-00	.300126		RES.,FXD,FILM: 2.4K OHM,5%,0.166W	0000M	313-0242-00
A1RT109	307-0124-00	.300126		RES.,THERMAL:5K OHM,10%	50157	1D1618
A1RT218	313-0821-00	.300126		RES.,FXD,FILM: 820 OHM,5%,0.166W	0000M	313-0821-00
A1RT219	307-0124-00	.300126		RES.,THERMAL:5K OHM,10%	50157	1D1618
A1RT408	313-0242-00	.300126		RES.,FXD,FILM: 2.4K OHM,5%,0.166W	0000M	313-0242-00
A1RT409	307-0124-00	.300126		RES.,THERMAL:5K OHM,10%	50157	1D1618
A1RT819	307-0181-00			RES.,THERMAL:100K OHM,10%,4MW/DEG C	15454	1DE104-K-220EC
A1U10	156-1837-00			MICROCIRCUIT,:DRIVER,W/STROBE		
A1U20	156-1837-00			MICROCIRCUIT,:DRIVER,W/STROBE		
A1U50	156-1822-00			MICROCIRCUIT,DI:C2MOS,8 BIT,ADDRESS LATCH	0000M	156-1822-00
A1U100	156-0534-00			MICROCIRCUIT,LI:DUAL DIFF AMPL,14 LD DIP	80009	156-0534-00
A1U133	156-1946-00			HYBRID,CIRCUIT:INLINE BLOCK	0000M	156-1946-00
A1U160	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A1U170	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A1U174	156-0644-00			MICROCIRCUIT,DI:QUAD BILATERAL SWITCH	80009	156-0644-00
A1U220	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A1U250	119-1671-00			HYBRID CIRCUIT:INLINE BLOCK	0000M	119-1671-00
A1U260	119-1671-00			HYBRID CIRCUIT:INLINE BLOCK	0000M	119-1671-00
A1U400	156-0534-00			MICROCIRCUIT,LI:DUAL DIFF AMPL,14 LD DIP	80009	156-0534-00
A1U430	156-1822-00			MICROCIRCUIT,DI:C2MOS,8 BIT,ADDRESS LATCH	0000M	156-1822-00
A1U433	156-1946-00			HYBRID,CIRCUIT:INLINE BLOCK	0000M	156-1946-00
A1U460	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A1U470	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A1U474	156-0644-00			MICROCIRCUIT,DI:QUAD BILATERAL SWITCH	80009	156-0644-00
A1U700	156-1349-00			MICROCIRCUIT,LI:DUAL INDEP DIFF AMPL	02735	CA3054
A1U720	156-1349-00			MICROCIRCUIT,LI:DUAL INDEP DIFF AMPL	02735	CA3054
A1U740	156-1349-00			MICROCIRCUIT,LI:DUAL INDEP DIFF AMPL	02735	CA3054
A1U980	156-0686-00			MICROCIRCUIT,LI:OPNL AMPL,HIGH IMPEDANCE	02735	CA3130S
A1VR434	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2	670-8098-00	.300100	.300340	CKT BOARD ASSY:TRIGGER	0000M	670-8098-00
A2	670-8098-01	.300341		CKT BOARD ASSY:TRIGGER	0000M	670-8098-01
A2C10	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C12	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C20	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A2C40	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A2C42	281-0775-00	.300101	.300200	CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C72	290-0267-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	162D105X0035CD2
A2C74	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C102	281-0258-00			CAP.,VAR,CER DI:2.5-20.5PF,250V		
A2C104	281-0257-00			CAP.,VAR,CER DI:4-28PF,250V		
A2C106	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A2C150	281-0774-00			CAP.,FXD,CER DI:0.022UF,20%,100V	12969	CGE223MEZ
A2C160	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A2C170	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A2C180	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A2C182	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A2C202	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A2C210	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A2C220	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C222	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C240	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C242	281-0775-00	.300301	.300200	CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C244	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C310	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C324	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A2C400	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C406	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C408	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C442	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C460	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C462	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C480	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C482	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C483	290-0246-00			CAP.,FXD,ELCTLT:3.3UF,10%,15V	56289	162D335X9015CD2
A2C485	290-0246-00			CAP.,FXD,ELCTLT:3.3UF,10%,15V	56289	162D335X9015CD2
A2C490	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C494	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C700	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A2C702	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A2C704	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A2C706	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A2CR32	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A2CR96	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A2CR180	152-0323-03			SEMICOND DEVICE:SIG,SI,BAX 13	0000M	152-0323-03
A2CR182	152-0323-03			SEMICOND DEVICE:SIG,SI,BAX 13	0000M	152-0323-03
A2CR200	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A2CR210	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A2CR216	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A2CR240	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A2CR242	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A2CR430	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2CR432	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A2CR600	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A2J960	131-3023-00			CONN,RCPT,ELEC:FEMALE,ANGLE 2 X 10	0000M	131-3023-00
A2J962	131-3022-00			CONN,RCPT,ELEC:FEMALE,ANGLE 2 X 5	0000M	131-3022-00
A2K100	148-0157-00			RELAY,REED:500 OHM,5V	0000M	148-0157-00
A2K110	148-0157-00			RELAY,REED:500 OHM,5V	0000M	148-0157-00
A2K120	148-0157-00			RELAY,REED:500 OHM,5V	0000M	148-0157-00
A2K140	148-0157-00			RELAY,REED:500 OHM,5V	0000M	148-0157-00
A2K150	148-0157-00			RELAY,REED:500 OHM,5V	0000M	148-0157-00
A2K160	148-0157-00			RELAY,REED:500 OHM,5V	0000M	148-0157-00
A2K170	148-0157-00			RELAY,REED:500 OHM,5V	0000M	148-0157-00
A2L700	108-1193-00			COIL,RF:FIXED,100UH		
A2L702	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A2L704	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A2L706	108-0947-00			COIL,RF:50NH	80009	108-0947-00
A2Q10	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q20	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q30	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A2Q32	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A2Q40	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q50	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q60	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A2Q70	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A2Q80	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A2Q90	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A2Q100	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A2Q160	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A2Q170	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A2Q180	151-1155-00			TRANSISTOR:FET,N-CHAN,8-12MA	0000M	151-1155-00
A2Q190	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q240	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A2Q242	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A2Q244	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A2Q250	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A2Q252	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A2Q254	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A2Q300	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2Q320	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A2R20	313-0470-00			RES.,FXD,FILM:47 OHM,5%,0.166W	0000M	313-0470-00
A2R22	313-0470-00			RES.,FXD,FILM:47 OHM,5%,0.166W	0000M	313-0470-00
A2R24	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A2R32	313-0271-00			RES.,FXD,FILM:270 OHM,5%,0.166W	0000M	313-0271-00
A2R34	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A2R50	313-0470-00			RES.,FXD,FILM:47 OHM,5%,0.166W	0000M	313-0470-00
A2R52	313-0470-00			RES.,FXD,FILM:47 OHM,5%,0.166W	0000M	313-0470-00
A2R54	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A2R70	313-0470-00			RES.,FXD,FILM:47 OHM,5%,0.166W	0000M	313-0470-00
A2R72	313-0123-00			RES.,FXD,FILM:12K OHM,5%,0.166W	0000M	313-0123-00
A2R74	313-0133-00			RES.,FXD,FILM:13K OHM,5%,0.166W	0000M	313-0133-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2R76	313-0470-00			RES.,FXD,FILM:47 OHM,5%,0.166W	0000M	313-0470-00
A2R78	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A2R80	313-0133-00			RES.,FXD,FILM:13K OHM,5%,0.166W	0000M	313-0133-00
A2R82	313-0123-00			RES.,FXD,FILM:12K OHM,5%,0.166W	0000M	313-0123-00
A2R90	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A2R92	313-0510-00			RES.,FXD,FILM: 51 OHM,5%,0.166W	0000M	313-0510-00
A2R94	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A2R96	313-0151-00			RES.,FXD,FILM:150 OHM,5%,0.166W	0000M	313-0151-00
A2R98	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A2R102	321-0807-00			RES.,FXD,FILM:900K OHM,1%,0.125W	91637	HFF1104F90002F
A2R106	321-1389-00			RES.,FXD,FILM:111K OH,1%,0.125W		
A2R160	313-0104-00			RES.,FXD,FILM:100K OHM,5%,0.166W	0000M	313-0104-00
A2R170	313-0563-00			RES.,FXD,FILM:56K OHM,5%,0.166W	0000M	313-0563-00
A2R172	321-0481-00			RES.,FXD,FILM:1M OHM,1%,0.125W	24546	NA4D1004F
A2R174	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A2R176	313-0100-00			RES.,FXD,FILM: 100 OHM,5%,0.166W	0000M	313-0100-00
A2R178	313-0100-00			RES.,FXD,FILM: 100 OHM,5%,0.166W	0000M	313-0100-00
A2R190	313-0122-00			RES.,FXD,FILM:1.2K OHM,5%,0.166W	0000M	313-0122-00
A2R192	313-0391-00			RES.,FXD,FILM:390 OHM,5%,0.166W	0000M	313-0391-00
A2R200	313-0303-00			RES.,FXD,FILM:30K OHM,5%,0.166W	0000M	313-0303-00
A2R202	313-0562-00			RES.,FXD,FILM:5.6K OHM,5%,0.166W	0000M	313-0562-00
A2R204	313-0683-00			RES.,FXD,FILM:68K OHM,5%,0.166W	0000M	313-0683-00
A2R206	313-0623-00			RES.,FXD,FILM:62K OHM,5%,0.166W		
A2R210	313-0510-00			RES.,FXD,FILM: 51 OHM,5%,0.166W	0000M	313-0510-00
A2R212	313-0822-00			RES.,FXD,FILM:8.2K OHM,5%,0.166W	0000M	313-0822-00
A2R214	313-0163-00			RES.,FXD,FILM:16K OHM,5%,0.166W	0000M	313-0163-00
A2R216	313-0273-00			RES.,FXD,FILM:27K OHM,5%,0.166W	0000M	313-0273-00
A2R220	313-0202-00			RES.,FXD,FILM: 2K OHM,5%,0.166W	0000M	313-0202-00
A2R222	313-0202-00			RES.,FXD,FILM: 2K OHM,5%,0.166W	0000M	313-0202-00
A2R224	313-0512-00			RES.,FXD,FILM: 5.1K OHM,5%,0.166W	0000M	313-0512-00
A2R226	313-0512-00			RES.,FXD,FILM: 5.1K OHM,5%,0.166W	0000M	313-0512-00
A2R240	307-0900-00			RES.,NTWK,FXD FI:(4)100 OHM,5%,0.25W	0000M	307-0900-00
A2R244	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A2R250	313-0271-00	.300101	.300125	RES.,FXD,FILM:270 OHM,5%,0.166W	0000M	313-0271-00
A2R250	313-0221-00	.300126		RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A2R251	311-2093-00	.300126		RES.,VAR,NONWW: TRMR,100 OHM,10%,0.5W	0000M	311-2093-00
A2R252	313-0511-00	.300101	.300200	RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A2R252	313-0331-00	.300201		RES.,FXD,FILM: 330 OHM,5%,0.166W	0000M	313-0331-00
A2R254	313-0621-00			RES.,FXD,FILM:620 OHM,5%,0.166W	0000M	313-0621-00
A2R256	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A2R258	311-2084-00			RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	0000M	311-2084-00
A2R260	313-0100-00			RES.,FXD,FILM: 100 OHM,5%,0.166W	0000M	313-0100-00
A2R264	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A2R270	313-0271-00			RES.,FXD,FILM:270 OHM,5%,0.166W	0000M	313-0271-00
A2R300	313-0122-00			RES.,FXD,FILM:1.2K OHM,5%,0.166W	0000M	313-0122-00
A2R302	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A2R304	313-0510-00	.300101	.300125	RES.,FXD,FILM: 51 OHM,5%,0.166W	0000M	313-0510-00
A2R304	313-0620-00	.300126		RES.,FXD,FILM: 62 OHM,5%,0.166W	0000M	313-0620-00
A2R306	313-0510-00	.300101	.300125	RES.,FXD,FILM: 51 OHM,5%,0.166W	0000M	313-0510-00
A2R306	313-0620-00	.300126		RES.,FXD,FILM: 62 OHM,5%,0.166W	0000M	313-0620-00
A2R308	313-0241-00			RES.,FXD,FILM:240 OHM,5%,0.166W	0000M	313-0241-00
A2R310	313-0151-00			RES.,FXD,FILM:150 OHM,5%,0.166W	0000M	313-0151-00
A2R312	313-0751-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	313-0751-00
A2R314	313-0751-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	313-0751-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2R320	311-2084-00			RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	0000M	311-2084-00
A2R324	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A2R330	311-2084-00			RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	0000M	311-2084-00
A2R332	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A2R402	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A2R404	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A2R406	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A2R407	313-0301-00			RES.,FXD,FILM:300 OHM,5%,0.166W	0000M	313-0301-00
A2R420	307-0907-00			RES.,NTWK,FXD FI:(4)3.3K OHM,5%,0.25W	0000M	307-0907-00
A2R430	307-0909-00			RES.,NTWK,FXD FI:(4)10K OHM,5%,0.25W		
A2R432	307-0909-00			RES.,NTWK,FXD FI:(4)10K OHM,5%,0.25W		
A2R440	307-0907-00			RES.,NTWK,FXD FI:(4)3.3K OHM,5%,0.25W	0000M	307-0907-00
A2R442	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A2R460	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A2R462	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A2R480	311-2093-00			RES.,VAR,NONWW: TRMR,100 OHM,10%,0.5W	0000M	311-2093-00
A2R482	311-2093-00			RES.,VAR,NONWW: TRMR,100 OHM,10%,0.5W	0000M	311-2093-00
A2R484	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A2R486	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A2R490	307-0903-00			RES.,NTWK,FXD FI:(6)1K,5%,0.125W		
A2R492	313-0331-00			RES.,FXD,FILM: 330 OHM,5%,0.166W	0000M	313-0331-00
A2R494	313-0241-00			RES.,FXD,FILM:240 OHM,5%,0.166W	0000M	313-0241-00
A2R496	313-0241-00			RES.,FXD,FILM:240 OHM,5%,0.166W	0000M	313-0241-00
A2R498	313-0331-00			RES.,FXD,FILM: 330 OHM,5%,0.166W	0000M	313-0331-00
A2R600	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A2R602	307-0907-00			RES.,NTWK,FXD FI:(4)3.3K OHM,5%,0.25W	0000M	307-0907-00
A2R604	313-0123-00			RES.,FXD,FILM:12K OHM,5%,0.166W	0000M	313-0123-00
A2R620	307-0907-00			RES.,NTWK,FXD FI:(4)3.3K OHM,5%,0.25W	0000M	307-0907-00
A2TP190	214-0579-00	.300101	.300200	TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A2U200	156-1816-00			MICROCIRCUIT,DI:NORTON,AMP	0000M	156-1816-00
A2U400	156-0515-00			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX	80009	156-0515-00
A2U420	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A2U440	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A2U460	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A2U480	156-1835-00			MICROCIRCUIT,LI:PP DETECTOR HYBRID	0000M	156-1835-00
A2U490	156-0205-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	04713	MC10102 (P OR L)
A2U494	156-0687-00			MICROCIRCUIT,DI:QUAD EXCLUSIVE-OR COMP	80009	156-0687-00
A2U600	156-1822-00			MICROCIRCUIT,DI:C2MOS,8 BIT,ADDRESS LATCH	0000M	156-1822-00
A2U620	156-1822-00			MICROCIRCUIT,DI:C2MOS,8 BIT,ADDRESS LATCH	0000M	156-1822-00
A2U640	156-1837-00			MICROCIRCUIT,:DRIVER,W/STROBE		
A2U650	156-0515-00			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX	80009	156-0515-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3	670-8097-00	.300100	.300340	CKT BOARD ASSY:SWEEP	0000M	670-8097-00
A3	670-8097-01	.300341		CKT BOARD ASSY:SWEEP	0000M	670-8097-01
A3C100	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3C102	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3C104	290-1020-00			CAP.,FXD,ELCTLT:330UF,+75-10%,10V		
A3C106	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3C108	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3C200	290-0246-00			CAP.,FXD,ELCTLT:3.3UF,10%,15V	56289	162D335X9015CD2
A3C202	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3C270	281-0788-00			CAP.,FXD,CER DI:470PF,10%,100V	96733	R3015
A3C272	281-0813-00			CAP.,FXD CER DI:0.047UF,20%,50V	04222	GC705-E-473M
A3C274	290-0246-00			CAP.,FXD,ELCTLT:3.3UF,10%,15V	56289	162D335X9015CD2
A3C300	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C320	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A3C322	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A3C324	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C400	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A3C434	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3C440	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C442	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C444	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C450	295-0169-00			CAP.,SET,MTCHD:1UF,0.01UF,0.001UF,MTCHD 1%	80009	295-0169-00
A3C454	281-0258-00			CAP.,VAR,CER DI:2.5-20.5PF,250V		
A3C458	281-0799-00			CAP.,FXD CER DI:62PF,2%,100V	04222	MA101A620GAA
A3C460	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C462	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3C500	283-0013-00			CAP.,FXD,CER DI:0.01UF,+100-0%,1000V	59660	818-602ZSUO103P
A3C540	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C542	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C544	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C550	295-0169-00			CAP.,SET,MTCHD:1UF,0.01UF,0.001UF,MTCHD 1%	80009	295-0169-00
A3C554	281-0258-00			CAP.,VAR,CER DI:2.5-20.5PF,250V		
A3C558	281-0799-00			CAP.,FXD CER DI:62PF,2%,100V	04222	MA101A620GAA
A3C560	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C562	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3C630	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A3C632	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3C634	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3C636	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3C638	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A3C640	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A3C690	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A3CR140	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A3CR142	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A3CR144	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A3CR452	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A3CR552	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A3CR680	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A3J950	131-3023-00			CONN,RCPT,ELEC:FEMALE,ANGLE 2 X 10	0000M	131-3023-00
A3J952	131-3021-00			CONN,RCPT,ELEC:FEMALE,ANGLE 2 X 3	0000M	131-3021-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3L100	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A3L102	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A3L104	108-1192-00			COIL,RF:FIXED,1MH	0000M	108-1192-0
A3L106	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A3L108	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A3L600	108-1192-00			COIL,RF:FIXED,1MH	0000M	108-1192-00
A3L640	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A3Q300	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q422	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A3Q430	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q432	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q450	151-1092-00			TRANSISTOR:SILICON,FE,N CHANNEL,SI	0000M	151-1092-00
A3Q452	151-1092-00			TRANSISTOR:SILICON,FE,N CHANNEL,SI	0000M	151-1092-00
A3Q480	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q482	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q484	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q490	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q492	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q522	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A3Q530	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q532	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q550	151-1092-00			TRANSISTOR:SILICON,FE,N CHANNEL,SI	0000M	151-1092-00
A3Q552	151-1092-00			TRANSISTOR:SILICON,FE,N CHANNEL,SI	0000M	151-1092-00
A3Q580	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q582	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q584	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A3Q590	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q592	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A3Q600	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A3R100	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A3R102	307-0907-00			RES.,NTWK,FXD FI:(4)3.3K OHM,5%,0.25W	0000M	307-0907-00
A3R122	307-0907-00			RES.,NTWK,FXD FI:(4)3.3K OHM,5%,0.25W	0000M	307-0907-00
A3R142	307-0904-00			RES.,NTWK,FXD FI:(4)10K,5%,0.125W		
A3R160	307-0907-00			RES.,NTWK,FXD FI:(4)3.3K OHM,5%,0.25W	0000M	307-0907-00
A3R200	313-0303-00			RES.,FXD,FILM:30K OHM,5%,0.166W	0000M	313-0303-00
A3R248	313-0122-00			RES.,FXD,FILM:1.2K OHM,5%,0.166W	0000M	313-0122-00
A3R250	313-0122-00			RES.,FXD,FILM:1.2K OHM,5%,0.166W	0000M	313-0122-00
A3R252	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A3R258	313-0392-00			RES.,FXD,FILM:3.9K OHM,5%,0.166W	0000M	313-0392-00
A3R260	313-0512-00			RES.,FXD,FILM: 5.1K OHM,5%,0.166W	0000M	313-0512-00
A3R266	313-0202-00			RES.,FXD,FILM: 2K OHM,5%,0.166W	0000M	313-0202-00
A3R270	313-0751-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	313-0751-00
A3R272	313-0202-00			RES.,FXD,FILM: 2K OHM,5%,0.166W	0000M	313-0202-00
A3R274	313-0302-00			RES.,FXD,FILM:3K OHM,5%,0.166W	0000M	313-0302-00
A3R276	313-0391-00			RES.,FXD,FILM:390 OHM,5%,0.166W	0000M	313-0391-00
A3R300	313-0182-00			RES.,FXD,FILM:2K OHM,5%,0.166W	0000M	313-0182-00
A3R302	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A3R304	313-0163-00			RES.,FXD,FILM:16K OHM,5%,0.166W	0000M	313-0163-00
A3R310	313-0513-00			RES.,FXD,FILM:51K OHM,5%,0.166W	0000M	313-0513-00
A3R312	313-0513-00			RES.,FXD,FILM:51K OHM,5%,0.166W	0000M	313-0513-00
A3R314	326-0027-00			RES.,FXD,FILM:100K OHM,1%,0.166W	0000M	326-0027-00
A3R316	326-0032-00			RES.,FXD,FILM:15K OHM,1%,0.166W	0000M	326-0032-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3R318	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A3R320	313-0623-00			RES.,FXD,FILM:62K OHM,5%,0.166W		
A3R322	326-0033-00			RES.,FXD,FILM:13K OHM,1%,0.166W	0000M	326-0033-00
A3R324	313-0132-00			RES.,FXD,FILM: 1.3K OHM,5%,0.166W	0000M	313-0132-00
A3R400	119-1723-00			CAPACITOR-RES:		
A3R422	313-0271-00			RES.,FXD,FILM:270 OHM,5%,0.166W	0000M	313-0271-00
A3R423	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A3R424	311-2084-00			RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	0000M	311-2084-00
A3R426	313-0182-00			RES.,FXD,FILM:2K OHM,5%,0.166W	0000M	313-0182-00
A3R428	313-0361-00			RES.,FXD,FILM: 360 OHM,5%,0.166W	0000M	313-0361-00
A3R430	307-0908-00			RES.,FXD,FILM:(4)330 OHM,5%,0.25W		
A3R434	313-0100-00			RES.,FXD,FILM: 100 OHM,5%,0.166W	0000M	313-0100-00
A3R436	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A3R450	307-0906-00			RES.,FXD,FILM:(4)100K OHM,5%,0.25W		
A3R460	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A3R462	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A3R480	326-0013-00			RES.,FXD,FILM:1K OHM,1%,0.166W	0000M	326-0013-00
A3R482	326-0010-00			RES.,FXD,FILM:470 OHM,1%,0.166W	0000M	326-0010-00
A3R483	313-0272-00			RES.,FXD,FILM:2.7K OHM,5%,0.166W	0000M	313-0272-00
A3R484	313-0362-00			RES.,FXD,FILM:3.6K OHM,5%,0.166W	0000M	313-0362-00
A3R486	313-0362-00			RES.,FXD,FILM:3.6K OHM,5%,0.166W	0000M	313-0362-00
A3R488	313-0362-00			RES.,FXD,FILM:3.6K OHM,5%,0.166W	0000M	313-0362-00
A3R490	313-0152-00			RES.,FXD,FILM:1.5K OHM,5%,0.166W	0000M	313-0152-00
A3R492	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A3R494	313-0152-00			RES.,FXD,FILM:1.5K OHM,5%,0.166W	0000M	313-0152-00
A3R500	119-1722-00			CAPACITOR-RES:		
A3R522	313-0271-00			RES.,FXD,FILM:270 OHM,5%,0.166W	0000M	313-0271-00
A3R523	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A3R524	311-2084-00			RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	0000M	311-2084-00
A3R536	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325
A3R560	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A3R562	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A3R580	313-0202-00			RES.,FXD,FILM: 2K OHM,5%,0.166W	0000M	313-0202-00
A3R582	313-0272-00			RES.,FXD,FILM:2.7K OHM,5%,0.166W	0000M	313-0272-00
A3R584	313-0362-00			RES.,FXD,FILM:3.6K OHM,5%,0.166W	0000M	313-0362-00
A3R586	313-0362-00			RES.,FXD,FILM:3.6K OHM,5%,0.166W	0000M	313-0362-00
A3R588	313-0362-00			RES.,FXD,FILM:3.6K OHM,5%,0.166W	0000M	313-0362-00
A3R590	313-0152-00			RES.,FXD,FILM:1.5K OHM,5%,0.166W	0000M	313-0152-00
A3R592	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A3R594	313-0152-00			RES.,FXD,FILM:1.5K OHM,5%,0.166W	0000M	313-0152-00
A3R600	313-0242-00			RES.,FXD,FILM: 2.4K OHM,5%,0.166W	0000M	313-0242-00
A3R601	313-0272-00			RES.,FXD,FILM:2.7K OHM,5%,0.166W	0000M	313-0272-00
A3R602	313-0242-00			RES.,FXD,FILM: 2.4K OHM,5%,0.166W	0000M	313-0242-00
A3R604	313-0132-00			RES.,FXD,FILM: 1.3K OHM,5%,0.166W	0000M	313-0132-00
A3R606	313-0152-00			RES.,FXD,FILM:1.5K OHM,5%,0.166W	0000M	313-0152-00
A3R608	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A3R610	326-0014-00			RES.,FXD,FILM:1.2K OHM,1%,0.166W	0000M	326-0014-00
A3R612	326-0013-00			RES.,FXD,FILM:1K OHM,1%,0.166W	0000M	326-0013-00
A3R614	313-0302-00			RES.,FXD,FILM:3K OHM,5%,0.166W	0000M	313-0302-00
A3R616	313-0152-00			RES.,FXD,FILM:1.5K OHM,5%,0.166W	0000M	313-0152-00
A3R620	313-0203-00			RES.,FXD,FILM:20K OHM,5%,0.166W	0000M	313-0203-00
A3R622	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A3R624	313-0152-00			RES.,FXD,FILM:1.5K OHM,5%,0.166W	0000M	313-0152-00
A3R626	313-0512-00			RES.,FXD,FILM: 5.1K OHM,5%,0.166W	0000M	313-0512-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3R628	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A3R630	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A3R680	307-0902-00			RES.,NTWK,FXD FI:(5)2.2K,5%,0.125W		
.						
A3SK200	136-0634-00			SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
.						
A3U100	156-1822-00			MICROCIRCUIT,DI:C2MOS,8 BIT,ADDRESS LATCH	0000M	156-1822-00
A3U120	156-1822-00			MICROCIRCUIT,DI:C2MOS,8 BIT,ADDRESS LATCH	0000M	156-1822-00
A3U140	156-1822-00			MICROCIRCUIT,DI:C2MOS,8 BIT,ADDRESS LATCH	0000M	156-1822-00
A3U200	155-0049-02			MICROCIRCUIT,DI:SWEEP CONTROL,W/LOCKOUT	80009	155-0049-02
A3U240	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A3U300	156-0515-00			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX	80009	156-0515-00
A3U320	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A3U400	156-0513-00			MICROCIRCUIT,DI:8-CHAN MUX	80009	156-0513-00
A3U410	156-0513-00			MICROCIRCUIT,DI:8-CHAN MUX	80009	156-0513-00
A3U420	156-1422-00			MICROCIRCUIT,LI:DUAL OPNL AMPL	0000M	156-1422-00
A3U500	156-0513-00			MICROCIRCUIT,DI:8-CHAN MUX	80009	156-0513-00
A3U510	156-0513-00			MICROCIRCUIT,DI:8-CHAN MUX	80009	156-0513-00
A3U520	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A3U600	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A3U620	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A3U640	156-0230-00			MICROCIRCUIT,DI:DUAL D MA-SLAVE FLIP-FLOP	04713	MC10131 (L OR P)
A3U680	156-0230-00			MICROCIRCUIT,DI:DUAL D MA-SLAVE FLIP-FLOP	04713	MC10131 (L OR P)

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A4	670-8096-00	.300101	.300340	CKT BOARD ASSY:CONTROL	0000M	670-8096-00
A4	670-8096-01	.300341		CKT BOARD ASSY:CONTROL	0000M	670-8096-01
A4C100	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A4C102	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A4C104	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A4C106	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A4C108	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C110	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A4C120	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A4C122	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C124	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C126	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C140	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A4C180	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C206	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A4C220	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C230	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C232	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C400	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C420	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C428	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C431	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A4C432	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A4C440	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C460	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4CR120	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A4CR122	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR124	313-0273-00			RES.,FXD,FILM:27K OHM,5%,0.166W	0000M	313-0273-00
A4CR142	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR144	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR270	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR290	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR296	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR430	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR440	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR442	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR444	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR446	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR448	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A4CR450	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A4J940	131-3023-00			CONN,RCPT,ELEC:FEMALE,ANGLE 2 X 10	0000M	131-3023-00
A4J942	131-3021-00			CONN,RCPT,ELEC:FEMALE,ANGLE 2 X 3	0000M	131-3021-00
A4K270	148-0157-00			RELAY,REED:500 OHM,5V	0000M	148-0157-00
A4L100	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A4L102	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A4L104	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A4L106	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A4L108	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A4R100	307-0922-00			RES.,NTWK,FXD FI:(8)100K,5%,0.125W		
A4R120	313-0221-00			RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A4R122	311-1980-00			RES.,VAR,NONWIR:CKT BD,5K OHM,10%,0.5W	0000M	311-1980-00
A4R124	326-0031-00	.300101	.300125	RES.,FXD,FILM:30K OHM,1%,0.166W		
A4R124	313-0273-00	.300126		RES.,FXD,FILM:27K OHM,5%,0.166W	0000M	313-0273-00
A4R126	326-0024-00			RES.,FXD,FILM:22K OHM,1%,0.166W	0000M	326-0024-00
A4R128	311-1980-00	.300101	.300125	RES.,VAR,NONWIR:CKT BD,5K OHM,10%,0.5W	0000M	311-1980-00
A4R128	311-1743-01	.300126		RES.,VAR,NONWIR:10K OHM,20%,0.5W	0000M	311-1743-01
A4R130	326-0021-00			RES.,FXD,FILM:10K OHM,1%,0.166W	0000M	326-0021-00
A4R132	313-0221-00			RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A4R136	313-0562-00			RES.,FXD,FILM:5.6K OHM,5%,0.166W	0000M	313-0562-00
A4R202	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A4R210	313-0913-00			RES.,FXD,FILM: 91K OHM,5%,0.166W	0000M	313-0913-00
A4R211	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A4R212	326-0016-00			RES.,FXD,FILM:2K OHM,1%,0.166W	0000M	326-0016-00
A4R214	326-0016-00			RES.,FXD,FILM:2K OHM,1%,0.166W	0000M	326-0016-00
A4R216	313-0104-00			RES.,FXD,FILM:100K OHM,5%,0.166W	0000M	313-0104-00
A4R220	311-2084-00			RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	0000M	311-2084-00
A4R222	313-0471-00			RES.,FXD,FILM:470 OHM,5%,0.166W	0000M	313-0471-00
A4R224	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A4R226	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A4R228	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A4R230	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A4R232	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A4R234	313-0753-00			RES.,FXD,FILM:75K OHM,5%,0.166W	0000M	313-0753-00
A4R250	313-0391-00			RES.,FXD,FILM:390 OHM,5%,0.166W	0000M	313-0391-00
A4R252	326-0028-00			RES.,FXD,FILM:3.6K OHM,1%,0.166W	0000M	326-0028-00
A4R254	313-0432-00			RES.,FXD,FILM:4.3K OHM,5%,0.166W	0000M	313-0432-00
A4R256	326-0028-00			RES.,FXD,FILM:3.6K OHM,5%,0.166W	0000M	326-0028-00
A4R258	326-0012-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	326-0012-00
A4R259	313-0432-00			RES.,FXD,FILM:4.3K OHM,5%,0.166W	0000M	313-0432-00
A4R260	326-0012-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	326-0012-00
A4R266	311-2093-00			RES.,VAR,NONWW: TRMR,100 OHM,10%,0.5W	0000M	311-2093-00
A4R268	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A4R272	313-0152-00			RES.,FXD,FILM:1.5K OHM,5%,0.166W	0000M	313-0152-00
A4R274	313-0152-00			RES.,FXD,FILM:1.5K OHM,5%,0.166W	0000M	313-0152-00
A4R275	313-0361-00			RES.,FXD,FILM: 360 OHM,5%,0.166W	0000M	313-0361-00
A4R276	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A4R277	313-0361-00			RES.,FXD,FILM: 360 OHM,5%,0.166W	0000M	313-0361-00
A4R278	313-0302-00			RES.,FXD,FILM:3K OHM,5%,0.166W	0000M	313-0302-00
A4R280	311-2084-00			RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	0000M	311-2084-00
A4R281	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A4R282	313-0392-00			RES.,FXD,FILM:3.9K OHM,5%,0.166W	0000M	313-0392-00
A4R283	313-0162-00			RES.,FXD,FILM:1.6K OHM,5%,0.166W	0000M	313-0162-00
A4R284	311-1743-00	.300101	.300125	RES.,VAR,NONWIR:TRMR,10K OHM,10%,0.5W	0000M	311-1743-00
A4R284	311-1981-00	.300126		RES.,VAR,NONWIR:CKT BD,20K OHM10%,0.5W		
A4R286	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A4R288	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A4R290	313-0752-00			RES.,FXD,FILM:7.5K OHM,5%,0.166W	0000M	313-0752-00
A4R291	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A4R292	313-0133-00			RES.,FXD,FILM:13K OHM,5%,0.166W	0000M	313-0133-00
A4R293	313-0392-00			RES.,FXD,FILM:3.9K OHM,5%,0.166W	0000M	313-0392-00
A4R294	313-0133-00			RES.,FXD,FILM:13K OHM,5%,0.166W	0000M	313-0133-00
A4R296	313-0302-00			RES.,FXD,FILM:3K OHM,5%,0.166W	0000M	313-0302-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A4R298	311-2093-00			RES.,VAR,NONWW: TRMR,100 OHM,10%,0.5W	0000M	311-2093-00
A4R299	313-0331-00	.300101	.300125	RES.,FXD,FILM: 330 OHM,5%,0.166W	0000M	313-0331-00
A4R299	313-0361-00	.300126		RES.,FXD,FILM: 360 OHM,5%,0.166W	0000M	313-0361-00
A4R410	313-0333-00			RES.,FXD,FILM:33K OHM,5%,0.166W	0000M	313-0333-00
A4R412	313-0333-00			RES.,FXD,FILM:33K OHM,5%,0.166W	0000M	313-0333-00
A4R420	307-0904-00			RES.,NTWK,FXD FI:(4)10K OHM,5%,0.125W		
A4R430	313-0153-00			RES.,FXD,FILM: 15K OHM,5%,0.166W	0000M	313-0153-00
A4R432	313-0331-00			RES.,FXD,FILM: 330 OHM,5%,0.166W	0000M	313-0331-00
A4R433	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A4R440	313-0331-00			RES.,FXD,FILM: 330 OHM,5%,0.166W	0000M	313-0331-00
A4R442	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A4R444	313-0821-00			RES.,FXD,FILM: 820 OHM,5%,0.166W	0000M	313-0821-00
A4R446	313-0621-00			RES.,FXD,FILM:620 OHM,5%,0.166W	0000M	313-0621-00
A4R450	313-0471-00			RES.,FXD,FILM:470 OHM,5%,0.166W	0000M	313-0471-00
A4R470	313-0681-00			RES.,FXD,FILM:680 OHM,5%,0.166W	0000M	313-0681-00
A4R472	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A4R474	313-0681-00			RES.,FXD,FILM:680 OHM,5%,0.166W	0000M	313-0681-00
A4R480	313-0202-00			RES.,FXD,FILM: 2K OHM,5%,0.166W	0000M	313-0202-00
A4R484	313-0392-00			RES.,FXD,FILM:3.9K OHM,5%,0.166W	0000M	313-0392-00
A4R486	313-0104-00			RES.,FXD,FILM:100K OHM,5%,0.166W	0000M	313-0104-00
A4R490	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A4R492	313-0302-00			RES.,FXD,FILM:3K OHM,5%,0.166W	0000M	313-0302-00
A4R494	313-0302-00			RES.,FXD,FILM:3K OHM,5%,0.166W	0000M	313-0302-00
A4R496	313-0302-00			RES.,FXD,FILM:3K OHM,5%,0.166W	0000M	313-0302-00
A4RT432	307-0181-00			RES.,THERMAL:100K OHM,10%,4MW/DEG C	15454	1DE104-K-220EC
ARRT440	307-0181-00			RES.,THERMAL:100K OHM,10%,4MW/DEG C	15454	1DE104-K-220EC
A4U100	156-1899-00			MICROCIRCUIT,DI:14 BIT DAC		
A4U110	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A4U120	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A4U140	156-1367-01			MICROCIRCUIT,LI:8-BIT BUFF MULT D/A CONV	0000M	156-1367-01
A4U160	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A4U180	156-1822-00			MICROCIRCUIT,DI:C2MOS,8 BIT,ADDRESS LATCH	0000M	156-1822-00
A4U200	156-1834-00			MICROCIRCUIT,DI:ANALOG,MLTPLXR HYBRID	0000M	156-1834-00
A4U220	156-0515-00			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX	80009	156-0515-00
A4U270	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A4U280	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A4U400	156-1818-00			MICROCIRCUIT,DI:CMOS,DUAL 4-BIT BINARY	0000M	156-1818-00
A4U402	156-1931-00			MICROCIRCUIT,DI:3 INPUT NAND	0000M	156-1931-00
A4U410	156-1949-00			MICROCIRCUIT,DI:QUAD 2 TO 1 SEL/MUX	0000M	156-1949-00
A4U420	156-0732-00			MICROCIRCUIT,DI:4-BY-4 RGTR FILES W/OC OUT	80009	156-0732-00
A4U430	156-1949-00			MICROCIRCUIT,DI:QUAD 2 TO 1 SEL/MUX	0000M	156-1949-00
A4U440	156-1949-00			MICROCIRCUIT,DI:QUAD 2 TO 1 SEL/MUX	0000M	156-1949-00
A4U442	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A4U450	156-1825-00			MICROCIRCUIT,DI:C2MOS,QUAD 4 TO 1 LINE	0000M	156-1825-00
A4U470	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A4U472	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A4U480	156-1949-00			MICROCIRCUIT,DI:QUAD 2 TO 1 SEL/MUX	0000M	156-1949-00
A4U490	156-1823-00			MICROCIRCUIT,DI:C2MOS,QUAD LATCH/CLEAR	0000M	156-1823-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A5	670-8086-00			CKT BOARD ASSY:ACQUISITION	0000M	670-8086-00
A5C10	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A5C20	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A5C30	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A5C32	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A5C42	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C44	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C53	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A5C56	281-0775-00	.300201		CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C60	281-0811-00			CAP.,FXD,CER DI:10PF,10%,100V	96733	R2911
A5C62	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C100	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C160	290-0246-00			CAP.,FXD,ELCTLT:3.3UF,10%,15V	56289	162D335X9015CD2
A5C162	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A5C172	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C182	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C300	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C310	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C360	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C510	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	GA101A470KAA
A5C512	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A5C550	281-0788-00			CAP.,FXD,CER DI:470PF,10%,100V	96733	R3015
A5C600	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A5C602	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A5C604	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A5C650	285-1117-00			CAP.,FXD,PLSTC:0.018UF,2%,100V	0000M	285-1117-00
A5C652	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A5C710	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C734	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A5C760	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C790	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5CR74	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A5CR500	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A5CR510	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A5CR512	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A5CR550	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A5CR552	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A5CR554	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A5CR650	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A5CR734	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A5CR736	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A5CR740	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A5CR60	153-0044-00			SEMICOND DVC SE:SIGNAL,MATCHED	80009	153-0044-00
A5J930	131-3023-00			CONN,RCPT,ELEC:FEMALE,ANGLE 2 X 10	0000M	131-3023-00
A5J932	131-3020-00			CONN,RCPT,ELEC:FEMALE,ANGLE 1 X 3	0000M	131-3020-00
A5L10	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A5L20	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A5L30	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A5L710	108-1190-00			COIL,RF:FIXED,10UH	0000M	108-1190-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A5P820	131-3013-00			CONN,RCPT,ELEC:EDGECARD,RTANGLE 2 X 15	0000M	131-3013-00
A5Q60	151-1111-00			TRANSISTOR:FET,N-CHAN,SI,2SK43-2,TO-92	0000M	151-1111-00
A5Q62	151-1111-00			TRANSISTOR:FET,N-CHAN,SI,2SK43-2,TO-92	0000M	151-1111-00
A5Q74	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A5Q94	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A5Q98	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A5Q650	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A5Q700	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A5R32	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A5R42	311-1621-00			RES.,VAR,NONWIR:200 OHM,20%,0.5W	0000M	311-1621-00
A5R47	311-2084-00			RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	0000M	311-2084-00
A5R49	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A5R50	311-2084-00			RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	0000M	311-2084-00
A5R53	313-0332-00			RES.,FXD,FILM: 3.3K OHM,5%,0.166W	0000M	313-0332-00
A5R54	313-0332-00			RES.,FXD,FILM: 3.3K OHM,5%,0.166W	0000M	313-0332-00
A5R55	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A5R56	311-0633-00	.300201		RES.,VAR,NONWIR:5K OHM,10%,0.50W	73138	82-30-1
A5R56	313-0913-00	.300201		RES.,FXD,FILM: 91K OHM,5%,0.166W	0000M	313-0913-00
A5R58	313-0102-00	.300201		RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A5R60	307-0900-00			RES.,NTWK,FXD FI:(4)100 OHM,5%,0.25W	0000M	307-0900-00
A5R62	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A5R64	313-0681-00			RES.,FXD,FILM:680 OHM,5%,0.166W	0000M	313-0681-00
A5R70	313-0201-00			RES.,FXD,FILM: 200 OHM,5%,0.166W	0000M	313-0201-00
A5R74	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A5R170	326-0011-00			RES.,FXD,FILM:510 OHM,1%,0.166W	0000M	326-0011-00
A5R172	326-0018-00			RES.,FXD,FILM:4.3K OHM,1%,0.166W	0000M	326-0018-00
A5R500	313-0222-00			RES.,FXD,FILM:2.2K OHM,5%,0.166W	0000M	313-0222-00
A5R600	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A5R602	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A5R604	313-0471-00			RES.,FXD,FILM:470 OHM,5%,0.166W	0000M	313-0471-00
A5R620	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A5R650	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A5R652	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A5R700	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A5R710	313-0151-00			RES.,FXD,FILM:150 OHM,5%,0.166W	0000M	313-0151-00
A5R730	326-0024-00	.300101	.300125	RES.,FXD,FILM:22K OHM,1%,0.166W	0000M	326-0024-00
A5R730	326-0022-00	.300126		RES.,FXD,FILM: 18K OHM,1%,0.166W	0000M	326-0022-00
A5R732	311-1743-00			RES.,VAR,NONWIR:TRMR,10K OHM,10%,0.5W	0000M	311-1743-00
A5R734	313-0222-00			RES.,FXD,FILM:2.2K OHM,5%,0.166W	0000M	313-0222-00
A5R736	313-0513-00			RES.,FXD,FILM:51K OHM,5%,0.166W	0000M	313-0513-00
A5R740	313-0102-00	.300101	.300125	RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A5R740	313-0202-00	.300126		RES.,FXD,FILM: 2K OHM,5%,0.166W	0000M	313-0202-00
A5R748	313-0103-00	.300126		RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A5R749	313-0221-00	.300126		RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A5R780	307-0923-00			RES.,NTWK,FXD FI:(8)33K,5%,0.125W	0000M	307-0923-00
A5R782	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A5R785	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A5RT68	313-0512-00	.300126		RES.,FXD,FILM: 5.1K OHM,5%,0.166W	0000M	313-0512-00
A5RT69	307-0124-00	.300126		RES.,THERMAL:5K OHM,10%	50157	1D1618

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A5U40	156-1836-00			MICROCIRCUIT,LI:AMPLIFIER HYBRID		
A5U50	156-1835-00			MICROCIRCUIT,LI:PP DECTECTOR HYBRID	0000M	156-1835-00
A5U55	156-1834-00			MICROCIRCUIT,DI:ANALOG,MLTPLXR HYBRID	0000M	156-1834-00
A5U60	156-1947-00			HYBRID,CIRCUIT:INLINE BLOCK	0000M	156-1947-00
A5U94	156-1948-00			HYBRID,CIRCUIT:INLINE BLOCK	0000M	156-1948-00
A5U100	156-1590-00			MICROCIRCUIT,LI:A/D CONV,400NS,8-BIT	0000M	156-1590-00
A5U220	156-1765-00			MICROCIRCUIT,DI:CMOS,OCTAL BFR,W/3 ST OUT	0000M	156-1765-00
A5U300	156-1893-00			MICROCIRCUIT,DI:CMOS,RAM 2K X 8	0000M	156-1893-00
A5U310	156-1828-00			MICROCIRCUIT,DI:CMOS,DUAL D-TYPE,FLIP-FLOP	0000M	156-1828-00
A5U320	156-1818-00			MICROCIRCUIT,DI:CMOS,DUAL 4-BIT BINARY	0000M	156-1818-00
A5U340	156-1818-00			MICROCIRCUIT,DI:CMOS,DUAL 4-BIT BINARY	0000M	156-1818-00
A5U360	156-1818-00			MICROCIRCUIT,DI:CMOS,DUAL 4-BIT BINARY	0000M	156-1818-00
A5U380	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A5U400	156-1765-00			MICROCIRCUIT,DI:CMOS,OCTAL BFR,W/3 ST OUT	0000M	156-1765-00
A5U420	156-1819-00			MICROCIRCUIT,DI:C2MOS,HEX BUS DRVR	0000M	156-1819-00
A5U480	156-0798-02			MICROCIRCUIT,DI:DUAL 14 TO 1 LINE SEL/MUX	01295	SN74LS153
A5U500	156-0422-02			MICROCIRCUIT,DI:UP/DOWN SYN BINARY CNTR	01295	SN74LS191
A5U600	156-1468-00			MICROCIRCUIT,LI:COMPARATOR	0000M	156-1468-00
A5U650	156-1114-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	02735	CA3160E
A5U710	156-1901-00			MICROCIRCUIT,DI:TTL,XTAL,OSCILLATOR		
A5U720	156-1824-00			MICROCIRCUIT,DI:C2MOS,QUAD 2 TO 1 LINE	0000M	156-1824-00
A5U740	156-0910-02			MICROCIRCUIT,DI:DUAL DECADE COUNTER	01295	SN74LS390
A5U750	156-1828-00			MICROCIRCUIT,DI:CMOS,DUAL D-TYPE,FLIP-FLOP	0000M	156-1828-00
A5U755	156-1766-00			MICROCIRCUIT,DI:CMOS,QUAD 2-INP NAND GATE	0000M	156-1766-00
A5U760	156-1895-00			MICROCIRCUIT,DI:PROGRAMMABLE DIVIDER		
A5U780	156-1770-00			MICROCIRCUIT,DI:OCTAL,D-TYPE,W/CLEAR		
A5U785	156-1826-00			MICROCIRCUIT,DI:2 TO 4 LINE MULTIPLEXER		
A5U790	156-1828-00			MICROCIRCUIT,DI:CMOS,DUAL D-TYPE,FLIP-FLOP	0000M	156-1828-00
A5U800	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A5VR740	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A5Y710	158-0264-00			XTAL UNIT,QTZ:20MHZ	0000M	158-0264-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A6	670-8088-00	.300100	.300340	CKT BOARD ASSY:DISPLAY	0000M	670-8088-00
A6	670-8088-01	.300341		CKT BOARD ASSY:DISPLAY	0000M	670-8088-01
A6C10	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A6C20	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A6C22	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C30	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A6C32	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C50	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A6C100	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C190	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C220	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C300	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6C330	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	GA101A470KAA
A6C340	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	GA101A470KAA
A6C380	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A6C385	285-1117-00			CAP.,FXD,PLSTC:0.018UF,2%,100V	0000M	285-1117-00
A6C502	281-0811-00			CAP.,FXD,CER DI:10PF,10%,100V	96733	R2911
A6C530	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A6C540	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A6C660	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	GA101A470KAA
A6C700	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	GA101A470KAA
A6C710	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A6CR50	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A6CR110	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A6CR502	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A6CR550	152-0833-00			SEMICOND DVC UN:SIG,4 DIODES	0000M	152-0833-00
A6CR552	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A6CR554	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A6J920	131-3023-00			CONN,RCPT,ELEC:FEMALE,ANGLE 2 X 10	0000M	131-3023-00
A6J922	131-2030-00			TERMINAL,PIN:RIGHT ANGLE		
A6L10	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A6L20	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A6L30	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A6P810	131-3013-00			CONN,RCPT,ELEC:EDGECARD,RTANGLE 2 X 15	0000M	131-3013-00
A6Q380	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A6Q390	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A6Q550	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A6R50	313-0332-00			RES.,FXD,FILM: 3.3K OHM,5%,0.166W	0000M	313-0332-00
A6R51	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A6R52	313-0123-00			RES.,FXD,FILM:12K OHM,5%,0.166W	0000M	313-0123-00
A6R54	311-1980-00			RES.,VAR,NONWIR:CKT BD,5K OHM,10%,0.5W	0000M	311-1980-00
A6R56	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A6R110	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A6R120	307-0923-00			RES.,NTWK,FXD FI:(8)33K,5%,0.125W	0000M	307-0923-00
A6R200	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A6R202	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A6R334	313-0363-00			RES.,FXD,FILM:36K OHM,5%,0.166W	0000M	313-0363-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A6R344	313-0363-00			RES.,FXD,FILM:36K OHM,5%,0.166W	0000M	313-0363-00
A6R370	311-1979-00			RES.,VAR,NONWIR:CKT BD,2K OHM,10%,0.5W	0000M	311-1979-00
A6R372	326-0020-00			RES.,FXD,FILM:5.1K OHM,1%,0.166W	0000M	326-0020-00
A6R374	313-0123-00			RES.,FXD,FILM:12K OHM,5%,0.166W	0000M	313-0123-00
A6R376	313-0473-00			RES.,FXD,FILM:47K OHM,5%,0.166W	0000M	313-0743-00
A6R380	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A6R385	321-0466-00			RES.,FXD,FILM:698K OHM,1%,0.125W	91637	MFF1816G69802F
A6R387	313-0513-00			RES.,FXD,FILM:51K OHM,5%,0.166W	0000M	313-0513-00
A6R390	313-0223-00			RES.,FXD,FILM:22K OHM,5%,0.166W	0000M	313-0223-00
A6R392	313-0473-00			RES.,FXD,FILM:47K OHM,5%,0.166W	0000M	313-0473-00
A6R394	313-0471-00			RES.,FXD,FILM:470 OHM,5%,0.166W	0000M	313-0471-00
A6R500	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A6R502	313-0332-00			RES.,FXD,FILM: 3.3K OHM,5%,0.166W	0000M	313-0332-00
A6R540	307-0911-00			RES.,NTWK,FXD FI:(4)33K OHM,5%,0.25W		
A6R554	313-0332-00			RES.,FXD,FILM: 3.3K OHM,5%,0.166W	0000M	313-0332-00
A6R700	326-0017-00			RES.,FXD,FILM:2.4K OHM,1%,0.166W	0000M	326-0017-00
A6R702	313-0273-00	.300101	.300200	RES.,FXD,FILM:27K OHM,5%,0.166W	0000M	313-0273-00
A6R702	313-0153-00	.300201		RES.,FXD,FILM: 15K OHM,5%,0.166W	0000M	313-0153-00
A6R704	311-1744-00	.300101	.300200	RES.,VAR,NONWIR:TRMR,20K OHM,10%,0.5W	0000M	311-1744-00
A6R704	311-1605-01	.300201		RES.,VAR,NONWIR:TRMR,50K OHM,10%,0.5W	0000M	311-1605-01
A6R730	313-0753-00			RES.,FXD,FILM:75K OHM,5%,0.166W	0000M	313-0753-00
A6R800	307-0900-00			RES.,NTWK,FXD FI:(4)100 OHM,5%,0.25W	0000M	307-0900-00
A6U50	156-1766-00			MICROCIRCUIT,DI:CMOS,QUAD 2-INP NAND GATE	0000M	156-1766-00
A6U100	156-1765-00			MICROCIRCUIT,DI:CMOS,OCTAL BFR,W/3 ST OUT	0000M	156-1765-00
A6U110	156-1831-00			MICROCIRCUIT,DI:GATE 2-INP NOR		
A6U120	156-1828-00			MICROCIRCUIT,DI:CMOS,DUAL D-TYPE,FLIP-FLOP	0000M	156-1828-00
A6U130	156-1826-00			MICROCIRCUIT,DI:2 TO 4 LINE MULTIPLEXER		
A6U150	156-1900-00			MICROCIRCUIT,DI:3 TO 8 DECODER,W/LATCH		
A6U160	156-1818-00			MICROCIRCUIT,DI:CMOS,DUAL 4-BIT BINARY	0000M	156-1818-00
A6U180	156-1818-00			MICROCIRCUIT,DI:CMOS,DUAL 4-BIT BINARY	0000M	156-1818-00
A6U190	156-1825-00			MICROCIRCUIT,DI-2CMOS,QUAD 4 TO 1 LINE	0000M	156-1825-00
A6U300	156-1894-00			MICROCIRCUIT,DI:CMOS,RAM 4K X 1	0000M	156-1894-00
A6U310	156-1894-00			MICROCIRCUIT,DI:CMOS,RAM 4K X 1		
A6U320	156-1893-00			MICROCIRCUIT,DI:CMOS,RAM 2K X 8	0000M	156-1893-00
A6U325	156-1893-00			MICROCIRCUIT,DI:CMOS,RAM 2K X 8	0000M	156-1893-00
A6U330	156-1815-00			MICROCIRCUIT,DI:DA CONVERTER,DUAL	0000M	156-1815-00
A6U350	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A6U355	156-0705-00			MICROCIRCUIT,DI:DUAL A/D COMPARATOR	80009	156-0705-00
A6U360	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A6U380	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A6U400	156-0515-00			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX	80009	156-0515-00
A6U500	156-1326-00			MICROCIRCUIT,DI:QUAD D TYPE FF,SCRN	80009	156-1326-00
A6U530	156-1766-00			MICROCIRCUIT,DI:CMOS,QUAD 2-INP NAND GATE	0000M	156-1766-00
A6U535	156-1818-00			MICROCIRCUIT,DI:CMOS,DUAL 4-BIT BINARY	0000M	156-1818-00
A6U540	156-1830-00			MICROCIRCUIT,DI:GATE TRIPLE,3 INP		
A6U660	156-1367-01			MICROCIRCUIT,LI:8-BIT BUFF MULT D/A CONV	0000M	156-1367-01
A6U700	156-1367-01			MICROCIRCUIT,LI:8-BIT BUFF MULT D/A CONV	0000M	156-1367-01
A6U720	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A6U722	156-0602-00			MICROCIRCUIT,DI:	01295	SN7495J
A6U730	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A7	670-8087-00	.300100	.300340	CKT BOARD ASSY:CPU	0000M	670-8087-00
A7	670-8087-01	.300341		CKT BOARD ASSY:CPU	0000M	670-8087-01
.						
A7C10	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A7C30	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A7C102	290-1014-00			CAP.,FXD,ELCTLT:1UF,35V	0000M	290-1014-00
A7C112	290-1014-00			CAP.,FXD,ELCTLT:1UF,35V	0000M	290-1014-00
A7C130	290-1014-00			CAP.,FXD,ELCTLT:1UF,35V	0000M	290-1014-00
A7C180	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A7C182	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A7C200	290-1014-00			CAP.,FXD,ELCTLT:1UF,35V	0000M	290-1014-00
A7C220	290-1014-00			CAP.,FXD,ELCTLT:1UF,35V	0000M	290-1014-00
A7C300	290-1014-00			CAP.,FXD,ELCTLT:1UF,35V	0000M	290-1014-00
A7C510	290-1014-00			CAP.,FXD,ELCTLT:1UF,35V	0000M	290-1014-00
A7C550	290-1014-00			CAP.,FXD,ELCTLT:1UF,35V	0000M	290-1014-00
.						
A7CR132	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A7CR160	152-0833-00			SEMICOND DVC UN:SIG,4 DIODES	0000M	152-0833-00
A7CR162	152-0833-00			SEMICOND DVC UN:SIG,4 DIODES	0000M	152-0833-00
A7CR300	152-0832-00			SEMICOND DVC UN:SIG,4 DIODES		
.						
A7SE200	276-0524-00			SHLD BEAD,ELEK:FERRITE 0.8MH AT 2MH		
A7SE220	276-0524-00			SHLD BEAD,ELEK:FERRITE 0.8MH AT 2MH		
A7SE300	276-0524-00			SHLD BEAD,ELEK:FERRITE 0.8MH AT 2MH		
A7SE302	276-0524-00			SHLD BEAD,ELEK:FERRITE 0.8MH AT 2MH		
.						
A7J602	131-0993-00			BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
A7J604	131-0993-00			BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
A7J910	131-3023-00			CONN,RCPT,ELEC:FEMALE,ANGLE 2 X 10	0000M	131-3023-00
.						
A7L10	108-1196-00			COIL,RF:RIPPLE FIL,10UH,1A	0000M	108-1196-00
A7L30	108-1195-00			COIL,RF:FIXED,10UH	0000M	108-1195-00
A7L110	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
.						
A7P600	131-3011-00			CONN,RCPT,ELEC:EDGECARD,ANGLE 2 X 5	0000M	131-3011-00
A7P700	131-3012-00			CONN,RCPT,ELEC:EDGECARD,ANGLE 2 X 8	0000M	131-3012-00
A7P800	131-3013-00			CONN,RCPT,ELEC:EDGECARD,RTANGLE 2 X 15	0000M	131-3013-00
.						
A7R102	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A7R104	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A7R106	307-0901-00			RES.,NTWK,FXD FI:(4)4.7K OHM,5%,0.125W		
A7R130	307-0901-00			RES.,NTWK,FXD FI:(4)4.7K OHM,5%,0.125W		
A7R132	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A7R170	307-0913-00			RES.,NTWK,FXD FI:(8)4.7K OHM		
A7R180	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A7R300	307-0905-00			RES.,NTWK,FXD FI:(4)1K OHM,5%,0.25W	0000M	307-0905-00
A7R302	307-0905-00			RES.,NTWK,FXD FI:(4)1K OHM,5%,0.25W	0000M	307-0905-00
A7R304	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A7R530	307-0905-00			RES.,NTWK,FXD FI:(4)1K OHM,5%,0.25W	0000M	307-0905-00
A7R532	307-0905-00			RES.,NTWK,FXD FI:(4)1K OHM,5%,0.25W	0000M	307-0905-00
A7R550	307-0905-00			RES.,NTWK,FXD FI:(4)1K OHM,5%,0.25W	0000M	307-0905-00
.						
A7SK100	136-0623-00			SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	CS9002-40
A7SK200	136-0694-00			SKT,PL-IN ELEK:MICROCIRCUIT,28 CONTACT	73803	CS9002-28

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A7SK220	136-0694-00			SKT,PL-IN ELEK:MICROCIRCUIT,28 CONTACT	73803	CS9002-28
A7SK300	136-0694-00			SKT,PL-IN ELEK:MICROCIRCUIT,28 CONTACT	73803	CS9002-28
A7U100	156-0983-00			MICROCIRCUIT,DI:MICROPROCESSOR EIGHT BIT	56708	Z 80 ACS
A7U110	156-1901-00			MICROCIRCUIT,DI:TTL,XTAL,OSCILLATOR		
A7U115	156-0895-01			MICROCIRCUIT,DI:14 BIT BINARY CNTR,BURN-IN	04713	MC14020BCLD
A7U130	156-1828-00			MICROCIRCUIT,DI:CMOS,DUAL D-TYPE,FLIP-FLOP	0000M	156-1828-00
A7U170	156-1820-00			MICROCIRCUIT,DI:C2MOS,BUFFER W/3 ST OUT	0000M	156-1820-00
A7U180	156-0645-02			MICROCIRCUIT,DI:HEX INV ST NAND GATES,SCRN	01295	SN74LS14
A7U182	156-1970-00			MICROCIRCUIT,DI:SUPPLY VOLTAGE SUPERVISOR		
A7U190	156-1766-00			MICROCIRCUIT,DI:CMOS,QUAD 2-INP NAND GATE	0000M	156-1766-00
A7U200	160-2070-00			MICROCIRCUIT,DI:32K X 8 MASK ROM 1	0000M	160-2070-00
A7U220	160-2071-00			MICROCIRCUIT,DI:16K X 8 MASK ROM 2	0000M	160-2071-00
A7U300	156-1817-00			MICROCIRCUIT,DI:CMOS,RAM 8K X 8	0000M	156-1817-00
A7U500	156-1826-00			MICROCIRCUIT,DI:2 TO 4 LINE MULTIPLEXER		
A7U510	156-1826-00			MICROCIRCUIT,DI:2 TO 4 LINE MULTIPLEXER		
A7U520	156-1827-00			MICROCIRCUIT,DI:3 TO 8 LINE DECODER		
A7U530	156-1827-00			MICROCIRCUIT,DI:3 TO 8 LINE DECODER		
A7U540	156-1829-00			MICROCIRCUIT,DI:GATE,QUAD 2-INP OR		
A7U550	156-1829-00			MICROCIRCUIT,DI:GATE,QUAD 2-INP OR		
A7Y110	158-0265-00			XTAL UNIT,QTZ:4.9152MHZ,200K	0000M	158-0265-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A8	670-8136-00			CKT BOARD ASSY:OPTION	0000M	670-8136-00
A8BT110	146-0048-00			BATTERY,STORAGE:3.6V,50 MAH	0000M	146-0048-00
A8C10	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A8C140	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A8C300	290-1014-00			CAP.,FXD,ELCTLT:1UF,35V	0000M	290-1014-00
A8C400	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A8C404	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A8C420	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A8C430	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A8CR110	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A8CR120	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A8CR404	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A8CR430	152-0835-00			SEMICOND DVC UN:ARRAY SIGNAL	0000M	152-0835-00
A8CR440	152-0834-00			SEMICOND DVC UN:ARRAY SIGNAL	0000M	152-0834-00
A8E300	276-0524-00			SHLD BEAD,ELEK:FERRITE 0.8MH AT 2MH		
A8J400	131-3010-00			CONN,RCPT,ELEC:FEMALE,GPIB,2A CONT	0000M	131-3010-00
A8L10	108-1196-00			COIL,RF:RIPPLE FIL,10UH,1A	0000M	108-1196-00
A8P840	131-3013-00			CONN,RCPT,ELEC:EDGECARD,RTANGLE 2 X 15	0000M	131-3013-00
A8Q120	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A8R100	321-0217-00			RES.,FXD,FILM:1.78K OHM,1%,0.125W	91637	MFF1816G17800F
A8R102	321-0332-00			RES.,FXD,FILM:28K OHM,1%,0.125W	91637	MFF1816G28001F
A8R104	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A8R110	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A8R112	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A8R114	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A8R120	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A8R130	307-0911-00			RES.,NTWK,FXD FI:(4)33K OHM,5%,0.25W		
A8R132	307-0911-00			RES.,NTWK,FXD FI:(4)33K OHM,5%,0.25W		
A8R300	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A8R302	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A8R304	307-0923-00			RES.,NTWK,FXD FI:(8)33K,5%,0.125W	0000M	307-0923-00
A8R404	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A8S130	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A8SK300	136-0694-00			SKT,PL-IN ELEK:MICROCIRCUIT,28 CONTACT	73803	CS9002-28
A8SK310	136-0694-00			SKT,PL-IN ELEK:MICROCIRCUIT,28 CONTACT	73803	CS9002-28
A8U100	156-1898-00			MICROCIRCUIT,DI:PROGRAMMABLE VOLTAGE REF		
A8U130	156-1821-00			MICROCIRCUIT,DI:C2MOS,HEX,NON-INV	0000M	156-1821-00
A8U140	156-1823-00			MICROCIRCUIT,DI:C2MOS,QUAD LATCH/CLEAR	0000M	156-1823-00
A8U300	156-1817-00			MICROCIRCUIT,DI:CMOS,RAM 8K X 8	0000M	156-1817-00
A8U310	156-1817-00			MICROCIRCUIT,DI:CMOS,RAM 8K X 8	0000M	156-1817-00
A8U400	156-1257-01			MICROCIRCUIT,DI:GPIB TALKER/LISTENER	0000M	156-1257-01
A8U410	156-1414-02			MICROCIRCUIT,DI: OCTAL GPIB BUS XCVR	27014	DS75160A
A8U420	156-1415-01			MICROCIRCUIT,DI: OCTAL GPIB XCVR-MANAGEMENT	27014	DS75161A
A8VR430	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A9	670-8095-00			CKT BOARD ASSY:MOTHER KEYBOARD	0000M	670-8095-00
A9C100	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9CR110	152-0833-00			SEMICOND DVC UN:SIG,4 DIODES	0000M	152-0833-00
A9CR120	152-0833-00			SEMICOND DVC UN:SIG,4 DIODES	0000M	152-0833-00
A9CR130	152-0833-00			SEMICOND DVC UN:SIG,4 DIODES	0000M	152-0833-00
A9CR140	152-0833-00			SEMICOND DVC UN:SIG,4 DIODES	0000M	152-0833-00
A9CR150	152-0833-00			SEMICOND DVC UN:SIG,4 DIODES	0000M	152-0833-00
A9CR160	152-0833-00			SEMICOND DVC UN:SIG,4 DIODES	0000M	152-0833-00
A9CR170	152-0833-00			SEMICOND DVC UN:SIG,4 DIODES	0000M	152-0833-00
A9J200	131-3053-00			CONN,RCPT,ELEC:FEMALE,1 X 20	0000M	131-3053-00
A9J201	131-3052-00			CONN,RCPT,ELEC:FEMALE,1 X 3	0000M	131-3052-00
A9P400	131-3028-00			CONN,RCPT,ELEC:EDGECARD,STRAIGHT 1 X 3	0000M	131-3028-00
A9P480	131-3027-00			CONN,RCPT,ELEC:EDGECARD,STRAIGHT 1 X 8	0000M	131-3027-00
A9P500	131-3028-00			CONN,RCPT,ELEC:EDGECARD,STRAIGHT 1 X 3	0000M	131-3028-00
A9R140	307-0923-00			RES.,NTWK,FXD FI:(8)33K,5%,0.125W	0000M	307-0923-00
A9R160	307-0921-00			RES.,NTWK,FXD FI:(8)33K OHM,5%,0.25W	0000M	307-0921-00
A9R202	307-0900-00			RES.,NTWK,FXD FI:(4)100 OHM,5%,0.25W	0000M	307-0900-00
A9R400	311-1631-00			RES.,VAR,NONWIR:10K OHM,10%,0.1W,W/SW	0000M	311-1631-00
A9R420	313-0912-00			RES.,FXD,FILM:9.1K OHM,5%,0.166W	0000M	313-0912-00
A9R422	311-1623-00			RES.,VAR,NONWIR:10K OHM,10%,0.25W	0000M	311-1623-00
A9R424	313-0332-00			RES.,FXD,FILM: 3.3K OHM,5%,0.166W	0000M	313-0332-00
A9R440	311-1631-00			RES.,VAR,NONWIR:10K OHM,10%,0.1W,W/SW	0000M	311-1631-00
A9R442	313-0912-00			RES.,FXD,FILM:9.1K OHM,5%,0.166W	0000M	313-0912-00
A9R460	311-1631-00			RES.,VAR,NONWIR:10K OHM,10%,0.1W,W/SW	0000M	311-1631-00
A9R462	313-0912-00			RES.,FXD,FILM:9.1K OHM,5%,0.166W	0000M	313-0912-00
A9R480	311-1623-00			RES.,VAR,NONWIR:10K OHM,10%,0.25W	0000M	311-1623-00
A9R490	311-1630-00			RES.,FXD,FILM:10K OHM,10%,0.1W,W/SWITCH		
A9R500	311-1623-00			RES.,VAR,NONWIR:10K OHM,10%,0.25W	0000M	311-1623-00
A9S120	260-2149-00			SW,ROTARY:4 BIT BINARY	0000M	260-2149-00
A9S122	260-2165-00			SWITCH,TOGGLE:SPDT,0.4VA,20V MAX	0000M	260-2165-00
A9S140	260-2149-00			SW,ROTARY:4 BIT BINARY	0000M	260-2149-00
A9S142	260-2165-00			SWITCH,TOGGLE:SPDT,0.4VA,20V MAX	0000M	260-2165-00
A9S160	260-2148-00			SW,ROTARY:4 BIT BINARY	0000M	260-2148-00
A9S162	260-2164-00			SWITCH,SLIDE:SPDT,6A,125VAC	0000M	260-2164-00
A9S300	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A9S320	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A9U100	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A9U120	156-1765-00			MICROCIRCUIT,DI:CMOS,OCTAL BFR,W/3 ST OUT	0000M	156-1765-00
A9U200	156-0732-00			MICROCIRCUIT,DI:4-BY-4 RGTR FILES W/OC OUT	80009	156-0732-00
A9U220	156-1900-00			MICROCIRCUIT,DI:3 TO 8 DECODER,W/LATCH		

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10	670-8094-00			CKT BOARD ASSY:KEYBOARD	0000M	670-8094-00
A10P100	131-3051-00			CONN,RCPT,ELEC:HEADER,1 X 20	0000M	131-3051-00
A10P101	131-3050-00			CONN,RCPT,ELEC:HEADER,1 X 3	0000M	131-3050-00
A10R100	311-1624-00			RES.,VAR,NONWIR:10K OHM,10%,0.25W		
A10R120	311-1624-00			RES.,VAR,NONWIR:10K OHM,10%,0.25W	0000M	311-1624-00
A10R140	311-1624-00			RES.,VAR,NONWIR:10K OHM,10%,0.25W	0000M	311-1624-00
A10S100	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S102	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A10S104	260-2154-00			SWITHC,KEY:SPST,W/LED RED	0000M	260-2154-00
A10S106	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S108	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S110	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S120	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S122	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A10S124	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A10S126	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S128	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S130	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S140	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A10S142	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A10S144	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A10S146	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S148	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S150	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S162	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A10S164	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A10S166	260-2156-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2156-00
A10S168	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00
A10S170	260-2155-00			SWITCH,KEY:SPST,W/LED GREEN	0000M	260-2155-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11	670-8093-00			CKT BOARD ASSY:VERTICAL OUTPUT	0000M	670-8093-00
A11C52	290-1011-00			CAP.,FD,ELCTLT:220UF,10V		
A11C53	290-1011-00			CAP.,FD,ELCTLT:220UF,10V		
A11C64	281-0237-00			CAP.,VAR,CER DI:3.3-18PF,250V	0000M	281-0237-00
A11C72	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11C82	283-0732-00			CAP.,FXD,CER DI:3PF,5%,500V	0000M	283-0732-00
A11C84	283-0732-00			CAP.,FXD,CER DI:3PF,5%,500V	0000M	283-0732-00
A11C86	281-0237-00			CAP.,VAR,CER DI:3.3-18PF,250V	0000M	281-0237-00
A11C87	281-0260-00			CAP.,VAR,CER DI:1.3-3PF		
A11C90	281-0775-00	.300101	.300125	CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11C100	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11C120	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A11C142	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11C143	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11C146	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11C151	281-0237-00			CAP.,VAR,CER DI:3.3-18PF,250V	0000M	281-0237-00
A11C154	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11C156	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11C160	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A11CR74	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A11E60	276-0543-02			SHIELDING BEAD,:	78488	57-3096
A11E70	276-0543-02			SHIELDING BEAD,:	78488	57-3096
A11J222	131-3019-00			CONN,RCPT,ELEC:FEMALE,ANGLE 1 X 8	0000M	131-3019-00
A11L53	108-0948-00			COIL,RF:FIXED,100UH	0000M	108-0948-00
A11Q56	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A11Q60	151-0367-00			TRANSISTOR:SILICON,NPN,SEL FROM 3571TP	04713	EP7426
A11Q70	151-0367-00			TRANSISTOR:SILICON,NPN,SEL FROM 3571TP	04713	EP7426
A11Q90	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A11Q94	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A11Q100	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A11Q102	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A11Q108	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A11Q110	151-0333-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS918	04713	SPS1752
A11Q112	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A11Q140	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A11Q142	151-0773-00			TRANSISTOR:SI,NPN	0000M	151-0773-00
A11Q152	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A11Q154	151-0773-00			TRANSISTOR:SI,NPN	0000M	151-0773-00
A11R54	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A11R55	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A11R56	313-0471-00			RES.,FXD,FILM:470 OHM,5%,0.166W	0000M	313-0471-00
A11R60	321-0082-00			RES.,FXD,FILM:69.8 OHM,1%,0.125W	91637	MFF1816G69R80F
A11R62	321-0082-00			RES.,FXD,FILM:69.8 OHM,1%,0.125W	91637	MFF1816G69R80F
A11R64	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A11R66	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A11R70	311-2005-00			RES.,VAR,NONWIR:CKT BD,100 OHM,10%,0.5W	0000M	311-2005-00
A11R72	313-0241-00			RES.,FXD,FILM:240 OHM,5%,0.166W	0000M	313-0241-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A11R74	311-0635-04			RES.,VAR,NONWIR:1K OHM,20%,0.5W	0000M	311-0735-04
A11R76	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A11R78	313-0751-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	313-0751-00
A11R79	313-0221-00			RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A11R80	313-0751-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	313-0751-00
A11R81	313-0221-00			RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A11R82	313-0122-00			RES.,FXD,FILM:1.2K OHM,5%,0.166W	0000M	313-0122-00
A11R84	313-0122-00			RES.,FXD,FILM:1.2K OHM,5%,0.166W	0000M	313-0122-00
A11R86	311-2041-00			RES.,VAR,NONWIR:CKT BD,10K OHM,10%,0.5W	0000M	311-2041-00
A11R87	311-0609-03			RES.,VAR,NONWW:2K OHM,20%,0.5W	0000M	311-0609-03
A11R90	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A11R92	313-0821-00			RES.,FXD,FILM: 820 OHM,5%,0.166W	0000M	313-0821-00
A11R94	313-0821-00			RES.,FXD,FILM: 820 OHM,5%,0.166W	0000M	313-0821-00
A11R96	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A11R97	313-0151-00			RES.,FXD,FILM:150 OHM,5%,0.166W	0000M	313-0151-00
A11R98	313-0151-00			RES.,FXD,FILM:150 OHM,5%,0.166W	0000M	313-0151-00
A11R99	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A11R100	313-0821-00			RES.,FXD,FILM: 820 OHM,5%,0.166W	0000M	313-0821-00
A11R102	311-2041-00			RES.,VAR,NONWIR:CKT BD,10K OHM,10%,0.5W	0000M	311-2041-00
A11R104	313-0361-00			RES.,FXD,FILM: 360 OHM,5%,0.166W	0000M	313-0361-00
A11R106	313-0471-00			RES.,FXD,FILM:470 OHM,5%,0.166W	0000M	313-0471-00
A11R108	313-0361-00			RES.,FXD,FILM: 360 OHM,5%,0.166W	0000M	313-0361-00
A11R110	313-0821-00			RES.,FXD,FILM: 820 OHM,5%,0.166W	0000M	313-0821-00
A11R112	313-0331-00			RES.,FXD,FILM: 330 OHM,5%,0.166W	0000M	313-0331-00
A11R120	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A11R124	313-0472-00	.300101	.300200	RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A11R124	313-0332-00	.300201		RES.,FXD,FILM: 3.3K OHM,5%,0.166W	0000M	313-0332-00
A11R126	311-2041-00			RES.,VAR,NONWIR:CKT BD,10K OHM,10%,0.5W	0000M	311-2041-00
A11R140	313-0391-00			RES.,FXD,FILM:390 OHM,5%,0.166W	0000M	313-0391-00
A11R142	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A11R143	307-0899-00			RES.,FXD,FILM:510 OHM,2%,2W	0000M	307-0899-00
A11R146	313-0221-00			RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A11R148	313-0221-00			RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A11R150	313-0201-00			RES.,FXD,FILM: 200 OHM,5%,0.166W	0000M	313-0201-00
A11R151	311-0605-03			RES.,VAR,NONWW::TRMR,200 OHM,20%,0.5W	0000M	311-0605-03
A11R152	313-0391-00			RES.,FXD,FILM:390 OHM,5%,0.166W	0000M	313-0391-00
A11R154	313-0220-00			RES.,FXD,FILM: 22 OHM,5%,0.166W	0000M	313-0220-00
A11R156	307-0899-00			RES.,FXD,FILM:510 OHM,2%,2W	0000M	307-0899-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A12	670-8092-00	.300100	.300340	CKT BOARD ASSY:HORIZONTAL OUTPUT	0000M	670-8092-00
A12	670-8092-01	.300341		CKT BOARD ASSY:HORIZONTAL OUTPUT	0000M	670-8092-01
A12C100	290-1019-00			CAP.,FXD,ELCTLT:47UF,-10+0%,10V		
A12C102	290-1019-00			CAP.,FXD,ELCTLT:47UF,-10+0%,10V		
A12C120	283-0328-00			CAP.,FXD,CER DI:0.03UF,+80-20%,200V	72982	8131N225Z5U0303Z
A12C130	283-0329-00			CAP.,FXD,CER DI:0.39PF,10%,500V	0000M	283-0329-00
A12C142	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C220	283-0328-00			CAP.,FXD,CER DI:0.03UF,+80-20%,200V	72982	8131N225Z5U0303Z
A12C230	283-0329-00			CAP.,FXD,CER DI:0.39PF,10%,500V	0000M	283-0329-00
A12C510	283-0328-00			CAP.,FXD,CER DI:0.03UF,+80-20%,200V	72982	8131N225Z5U0303Z
A12C602	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C614	281-0537-00			CAP.,FXD,CER DI:0.68PF,20%,600V	95121	OC-.68MM 20%
A12C640	283-0328-00			CAP.,FXD,CER DI:0.03UF,+80-20%,200V	72982	8131N225Z5U0303Z
A12C660	283-0328-00			CAP.,FXD,CER DI:0.03UF,+80-20%,200V	72982	8131N225Z5U0303Z
A12CR100	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A12CR106	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A12CR120	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A12CR206	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A12CR220	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A12CR600	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A12CR602	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A12CR604	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A12CR606	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A12CR608	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A12J100	131-3018-00			CONN,RCPT,ELEC:FEMALE,ANGLE 1 X 4	0000M	131-3018-00
A12Q100	151-0775-00			TRANSISTOR:SI,PNP	0000M	151-0775-00
A12Q120	151-0776-00			TRANSISTOR:SI,NPN	0000M	151-0776-00
A12Q140	151-0770-00			TRANSISTOR:SI,NPN	0000M	151-0770-00
A12Q160	151-0739-00			TRANSISTOR:SI,PNP	0000M	151-0739-00
A12Q200	151-0775-00			TRANSISTOR:SI,PNP	0000M	151-0775-00
A12Q220	151-0776-00			TRANSISTOR:SI,NPN	0000M	151-076-00
A12Q240	151-0770-00			TRANSISTOR:SI,NPN	0000M	151-0770-00
A12Q260	151-0739-00			TRANSISTOR:SI,PNP	0000M	151-0739-00
A12Q600	151-0775-00			TRANSISTOR:SI,PNP	0000M	151-0775-00
A12Q620	151-0776-00			TRANSISTOR:SI,NPN	0000M	151-0776-00
A12Q640	151-0770-00			TRANSISTOR:SI,NPN	0000M	151-0770-00
A12Q660	151-0739-00			TRANSISTOR:SI,PNP	0000M	151-0739-00
A12R100	313-0751-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	313-0751-00
A12R106	313-0123-00			RES.,FXD,FILM:12K OHM,5%,0.166W	0000M	313-0123-00
A12R110	313-0333-00			RES.,FXD,FILM:33K OHM,5%,0.166W	0000M	313-0333-00
A12R122	313-0151-00			RES.,FXD,FILM:150 OHM,5%,0.166W	0000M	313-0151-00
A12R130	322-0327-00			RES.,FXD,FILM:	91637	CMF6042G24901F
A12R140	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A12R142	313-0751-00			RES.,FXD,FILM:750 OHM,5%,0.166W	0000M	313-0751-00
A12R144	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A12R162	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A12R200	311-0605-03			RES.,VAR,NONWW::TRMR,200 OHM,20%,0.5W	0000M	311-0605-03
A12R202	313-0621-00			RES.,FXD,FILM:620 OHM,5%,0.166W	0000M	313-0621-00
A12R210	313-0333-00			RES.,FXD,FILM:33K OHM,5%,0.166W	0000M	313-0333-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A12R222	313-0151-00			RES.,FXD,FILM:150 OHM,5%,0.166W	0000M	313-0151-00
A12R230	322-0327-00			RES.,FXD,FILM:	91637	CMF6042G24901F
A12R244	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A12R262	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A12R264	313-0124-00			RES.,FXD,FILM:120K OHM,5%,0.166W	0000M	313-0124-00
A12R600	313-0202-00			RES.,FXD,FILM: 2K OHM,5%,0.166W	0000M	313-0202-00
A12R602	313-0123-00			RES.,FXD,FILM:12K OHM,5%,0.166W	0000M	313-0123-00
A12R604	313-0122-00			RES.,FXD,FILM:1.2K OHM,5%,0.166W	0000M	313-0122-00
A12R606	313-0222-00			RES.,FXD,FILM:2.2K OHM,5%,0.166W	0000M	313-0222-00
A12R608	313-0511-00			RES.,FXD,FILM: 510 OHM,5%,0.166W	0000M	313-0511-00
A12R610	313-0513-00			RES.,FXD,FILM:51K OHM,5%,0.166W	0000M	313-0513-00
A12R614	322-0327-00			RES.,FXD,FILM:	91637	CMF6042G24901F
A12R618	313-0184-00			RES.,FXD,FILM:180K OHM,5%,0.166W	0000M	313-0184-00
A12R620	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A12R622	313-0162-00			RES.,FXD,FILM:1.6K OHM,5%,0.166W	0000M	313-0162-00
A12R624	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A12VR260	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A13	670-8091-00			CKT BOARD ASSY:DC/DC CONVERTER	0000M	670-8091-00
A13C35	285-1273-00			CAP.,FXD,PLSTC:0.0022UF,20%,250V		
A13C152	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A13C156	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50%-10%,10V	T0020	10VB5L100
A13C165	290-0246-00			CAP.,FXD,ELCTLT:3.3UF,10%,15V	05397	T322B335K015AS
A13C170	281-0755-00			CAP.,FXD,CER DI:1.8PF,0.1%,500V	96733	R2731
A13C172	290-1008-00			CAP.,FXD,ELCTLT:100UF,50V		
A13C174	290-1009-00			CAP.,FXD,ELCTLT:10UF,160V		
A13C182	290-1010-00			CAP.,FXD,ELCTLT:470UF,16V	0000M	290-1010-00
A13C184	290-0949-00			CAP.,FXD,ELCTLT:1000UF,20%,6.3V		
A13C186	290-1010-00			CAP.,FXD,ELCTLT:470UF,16V	0000M	290-1010-00
A13C188	290-1010-00			CAP.,FXD,ELCTLT:470UF,16V	0000M	290-1010-00
A13C189	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A13C190	285-1282-00			CAP.,FXD,PLASTIC:0.068UF,10%,630V		
A13C192	290-1010-00			CAP.,FXD,ELCTLT:470UF,16V	0000M	290-1010-00
A13C202	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	T0020	10VB5L100
A13C206	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A13C226	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	T0020	10VB5L100
A13C228	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A13C246	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A13C250	290-0755-00			CAP.,FXD,ELCTLT:100UF,+50-10%,10V	T0020	10VB5L100
A13CR135	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A13CR156	152-0694-00			SEMICOND DEVICE:RECT,SI,420V,1A	0000M	152-0694-00
A13CR158	152-0694-00			SEMICOND DEVICE:RECT,SI,420V,1A	0000M	152-0694-00
A13CR160	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A13CR170	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A13CR172	152-0694-00			SEMICOND DEVICE:RECT,SI,420V,1A	0000M	152-0694-00
A13CR174	152-0694-00			SEMICOND DEVICE:RECT,SI,420V,1A	0000M	152-0694-00
A13CR182	152-0606-00			SEMICOND DEVICE:POW,SI,100V,8A	0000M	152-0606-00
A13CR184	152-0773-00			SEMICOND DEVICE:RECT	0000M	152-0773-00
A13CR186	152-0773-00			SEMICOND DEVICE:RECT	0000M	152-0773-00
A13CR188	152-0607-00			SEMICOND DEVICE:POW,SI,100V,8A	0000M	152-0607-00
A13CR189	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A13CR224	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A13CR242	152-0832-00			SEMICOND DEVICE:SIG,SI,100MA,75V	0000M	152-0832-00
A13J120	131-3017-00			CONN,RCPT,ELEC:FEMALE,STRAIGHT 1 X 8	0000M	131-3017-00
A13J220	131-3026-00			CONN,RCPT,ELEC:FEMALE,STRAIGHT 1 X 12-4	0000M	131-3026-00
A13L182	108-1196-00			COIL,RF:RIPPLE FIL,10UH,1A	0000M	108-1196-00
A13L183	108-1196-00			COIL,RF:RIPPLE FIL,10UH,1A	0000M	108-1196-00
A13L184	108-1194-00			COIL,RF:FIXED,27UH	0000M	108-1194-00
A13L186	108-1196-00			COIL,RF:RIPPLE FIL,10UH,1A	0000M	108-1196-00
A13L187	108-1196-00			COIL,RF:RIPPLE FIL,10UH,1A	0000M	108-1196-00
A13Q150	151-0601-00			TRANSISTOR:SILICON,NPN	0000M	151-0601-00
A13Q152	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A13Q156	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A13Q160	153-0656-00			TRANSISTOR:SELECTED,MATCHED	0000M	153-0656-00
A13Q162	153-0656-00			TRANSISTOR:SELECTED,MATCHED	0000M	153-0656-00
A13Q200	151-0772-00			TRANSISTOR:SI,PNP	0000M	151-0772-00
A13Q220	151-0772-00			TRANSISTOR:SI,PNP	0000M	151-0772-00
A13Q240	151-0771-00			TRANSISTOR:SI,NPN	0000M	151-0771-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A13R35	308-0850-00			RES.,FXD,WW:5.1 OHM,10%,5W	0000M	308-0850-00
A13R134	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A13R135	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A13R138	315-0620-00			RES.,FXD,CMPSN:62 OHM,5%,0.25W	01121	CB6205
A13R148	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A13R150	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A13R152	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A13R156	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325
A13R158	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A13R159	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A13R160	313-0102-00			RES.,FXD,FILM: 1K OHM,5%,0.166W	0000M	313-0102-00
A13R161	313-0472-00			RES.,FXD,FILM:4.7K OHM,5%,0.166W	0000M	313-0472-00
A13R162	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A13R164	313-0432-00			RES.,FXD,FILM:43K OHM,5%,0.166W	0000M	313-0432-00
A13R166	313-0101-00			RES.,FXD,FILM:100 OHM,5%,0.166W	0000M	313-0101-00
A13R167	311-1620-00			RES.,VAR,NONWIR:1K OHM,20%,0.5W	0000M	311-1620-00
A13R168	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535
A13R170	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A13R172	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A13R174	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A13R189	315-0111-00			RES.,FXD,CMPSN:110 OHM,5%,0.25W	01121	CB1115
A13R192	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A13R200	313-0162-00			RES.,FXD,FILM:1.6K OHM,5%,0.166W	0000M	313-0162-00
A13R202	313-0681-00			RES.,FXD,FILM:680 OHM,5%,0.166W	0000M	313-0681-00
A13R204	321-0231-00			RES.,FXD,FILM:2.49K OHM,1%,0.125W	91637	MFF1816G24900F
A13R206	321-0264-00			RES.,FXD,FILM:5.49K OHM,1%,0.125W	91637	MFF1816G54900F
A13R220	313-0221-00			RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A13R224	313-0361-00			RES.,FXD,FILM: 360 OHM,5%,0.166W	0000M	313-0361-00
A13R226	321-0289-01			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	MFF1816G10001D
A13R228	321-0289-01			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	MFF1816G10001D
A13R240	313-0221-00			RES.,FXD,FILM: 220 OHM,5%,0.166W	0000M	313-0221-00
A13R242	313-0241-00			RES.,FXD,FILM:240 OHM,5%,0.166W	0000M	313-0241-00
A13R246	321-0318-02			RES.,FXD,FILM:20K OHM,0.5%,0.125W	91637	CMF55116D20001D
A13R248	321-0289-01			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	MFF1816G10001D
A13S30	260-1849-00			SWITCH,PUSH:DPDT,4A,250VAC,W/BRKT	31918	NE15/F2U103EE
A13T190	120-1506-01			XFMR,PWR,STU:	0000M	120-1506-01
A13U160	156-1897-00			MICROCIRCUIT,DI:PHOTO COUPLER		
A13U200	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A13U220	156-1771-00			MICROCIRCUIT,LI:DUAL OP AMP	0000M	156-1771-00
A13U250	156-1166-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	0000M	156-1166-00
A13VR150	152-0149-00			SEMICOND DEVICE:ZENER,0.4W,10V,5%	04713	SZG35009K3
A13VR162	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A13VR189	152-0217-00			SEMICOND DEVICE:ZENER,0.4W,8.2V,5%	04713	SZG20

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A14	670-8090-00	.300100	.300340	CKT BOARD ASSY:PRIMARY	0000M	670-8090-00
A14	670-8090-01	.300341		CKT BOARD ASSY:PRIMARY	0000M	670-8090-01
A14C12	285-1272-00			CAP.,FXD,PLSTC:0.22UF,20%,250V		
A14C13	285-1273-00			CAP.,FXD,PLSTC:0.0022UF,20%,250V		
A14C50	290-1012-00			CAP.,FXD,ELCTLT:330UF,20%,200V		
A14C52	290-1012-00			CAP.,FXD,ELCTLT:330UF,20%,200V		
A14C53	285-0891-00			CAP.,FXD,PLSTC:0.1UF,1.5%,100V	80009	285-0891-00
A14C94	285-0013-00			CAP.,FXD,CER DI:2200PF,10%,50V		
A14C120	290-1007-00			CAP.,FXD,ELCTLT:22UF,20%,16V	0000M	290-1007-00
A14C122	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A14C130	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C142	283-0279-00			CAP.,FXD,CER DI:0.001UF,20%,3000V	59660	878-521-S-Y5S-10
A14CR50	152-0694-00			SEMICOND DEVICE:RECT,SI,420V,1A	0000M	152-0694-00
A14CR51	152-0694-00			SEMICOND DEVICE:RECT,SI,420V,1A	0000M	152-0694-00
A14CR52	152-0694-00			SEMICOND DEVICE:RECT,SI,420V,1A	0000M	152-0694-00
A14CR53	152-0694-00			SEMICOND DEVICE:RECT,SI,420V,1A	0000M	152-0694-00
A14CR100	152-0608-00			SEMICOND DEVICE:POW,SI,1000V,0.2A	0000M	152-0608-00
A14CR130	152-0608-00			SEMICOND DEVICE:POW,SI,1000V,0.2A	0000M	152-0608-00
A14CR144	152-0831-00			SEMICOND DEVICE:RECT,SI,0.2A,1500V	0000M	152-0831-00
A14CR146	152-0608-00			SEMICOND DEVICE:POW,SI,1000V,0.2A		
A14L12	108-1189-01			COIL,RF:FIXED,20MH COM MODE CH	0000M	108-1189-01
A14L53	108-1200-00			COIL,RF:FIXED,72UF,2A	0000M	108-1200-00
A14L144	108-1191-00			COIL,RF:FIXED,1.5MH,10%	0000M	108-1191-00
A14P120	131-3016-00			CONN,RCPT,ELEC:EDGECARD,ANGLE 1 X 8	0000M	131-3016-00
A14P220	131-3025-00			CONN,RCPT,ELEC:EDGECARD,ANGLE 1 X 12-4	0000M	131-3025-00
A14Q102	151-0543-00			TRANSISTOR:SILICON,UJT	0000M	151-0543-00
A14Q124	151-0543-00			TRANSISTOR:SILICON,UJT	0000M	151-0543-00
A14R12	301-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.50W	01121	EB4745
A14R50	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	01121	CB1545
A14R52	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	01121	CB1545
A14R90	315-0564-00			RES.,FXD,CMPSN:560K OHM,5%,0.25W	01121	CB5645
A14R92	302-0683-00			RES.,FXD,CMPSN:68K OHM,10%,0.50W	01121	EB6831
A14R94	302-0683-00			RES.,FXD,CMPSN:68K OHM,10%,0.50W	01121	EB6831
A14R102	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A14R120	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A14R122	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A14R125	315-0225-00			RES.,FXD,CMPSN:2.2M OHM,5%,0.25W	01121	CB2255
A14R126	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A14R130	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A14R144	301-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.50W	01121	EB1035
A14RV40	119-1673-00			DELAY LINE,ELEC:SURGE VOLTAGE,220V	0000M	119-1673-00
A14RV42	119-1673-00			DELAY LINE,ELEC:SUGRE VOLTAGE,220V	0000M	119-1673-00
A14T130	120-1505-01			XFMR,PWR,STU:STORAGE CONVERTER	0000M	120-1505-01
A14U120	156-1897-00			MICROCIRCUIT,DI:PHOTO COUPLER		

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A15	670-8089-00	.300100	.300340	CKT BOARD ASSY:HIGH VOLTAGE	0000M	670-8089-00
A15	670-8089-01	.300341		CKT BOARD ASSY:HIGH VOLTAGE	0000M	670-8089-01
A15C10	283-0076-00			CAP.,FXD,CER DI:27PF,10%,500V	59660	831-500S2L27OK
A15C22	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831610Y5U0102P
A15C30	283-0076-00			CAP.,FXD,CER DI:27PF,10%,500V	59660	831-500S2L27OK
A15C40	283-0005-00			CAP.,FXD,CER DI:0.01UF,+100-0%,250V	72982	8131N300Z5U0103P
A15C52	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A15C56	283-0002-00			CAP.,FXD,CER DI:0.01UF,+80-20%,500V	59821	SDDH69L103Z
A15C68	283-0002-02			CAP.,FXD,CER DI:0.01UF,+80-20%,500V		
A15C76	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A15C78	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A15C80	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A15C82	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	12969	CGB102KEX
A15C102	290-1017-00			CAP.,FXD,ELCTLT:470UF,20%,6.3V		
A15C105	283-0351-00			CAP.,FXD,CER DI:5000PF,20%,3000V	59660	848-562Z5U0502M
A15C150	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	59821	2DDH66J103Z
A15C154	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	59821	2DDH66J103Z
A15C162	283-0002-00			CAP.,FXD,CER DI:0.01UF,+80-20%,500V	59821	SDDH69L103Z
A15CR10	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A15CR36	152-0242-00			SEMICOND DEVICE:SILICON,225V,200MA	07263	FDH5004
A15CR56	152-0831-00			SEMICOND DEVICE:RECT,SI,0.2A,1500V	0000M	152-0831-00
A15CR60	152-0831-00			SEMICOND DEVICE:RECT,SI,0.2A,1500V	0000M	152-0831-00
A15CR68	152-0831-00			SEMICOND DEVICE:RECT,SI,0.2A,1500V	0000M	152-0831-00
A15CR72	152-0831-00			SEMICOND DEVICE:RECT,SI,0.2A,1500V	0000M	152-0831-00
A15Q50	151-1092-00			TRANSISTOR:SILICON,FE,N CHANNEL,SI	0000M	151-1092-00
A15Q54	151-0667-00			TRANSISTOR:SILICON,NPN		
A15Q72	151-0667-00			TRANSISTOR:SILICON,NPN		
A15Q100	151-1095-00			TRANSISTOR:SILICON,PNP	0000M	151-1095-00
A15Q102	151-1095-00			TRANSISTOR:SILICON,PNP	0000M	151-1095-00
A15R10	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A15R20	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A15R22	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A15R38	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A15R40	311-0613-00			RES.,VAR,NONWIR:100K OHM,10%,0.50W	73138	82-27-2
A15R50	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A15R52	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535
A15R54	315-0475-00			RES.,FXD,CMPSN:4.7M OHM,5%,0.25W	01121	CB4755
A15R56	313-0103-00			RES.,FXD,FILM: 10K OHM,5%,0.166W	0000M	313-0103-00
A15R70	301-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.5W	01121	EB1045
A15R74	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A15R78	321-0481-00			RES.,FXD,FILM:1M OHM,1%,0.125W	24546	NA4D1004F
A15R86	313-0334-00			RES.,FXD,FILM:330K OHM,5%,0.166W	0000M	313-0334-00
A15R100	313-0620-00			RES.,FXD,FILM: 62 OHM,5%,0.166W	0000M	313-0620-00
A15R102	313-0620-00			RES.,FXD,FILM: 62 OHM,5%,0.166W	0000M	313-0620-00
A15R150	311-0698-00			RES.,VAR,NONWIR:1M OHM,0.50W	73138	82PRIMEG-36B
A15R152	313-0683-00			RES.,FXD,FILM:68K OHM,5%,0.166W	0000M	313-0683-00
A15R154	313-0333-00			RES.,FXD,FILM:33K OHM,5%,0.166W	0000M	313-0333-00
A15R160	311-0606-00			RES.,VAR,NONWIR:500K OHM,30%,0.50W	73138	82-24-0
A15T100	120-1508-01			XFMR,PWR,STPDN:HEATER,TRIODE	0000M	120-1508-01

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
.						
A15U80	156-1114-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	02735	CA3160E
A15U100	119-1684-00			MULTIPLIER,HV:2X,2/DC RESTORER	0000M	119-1684-00
.						
A15VR38	152-0286-00			SEMICOND DEVICE:ZENER,0.4W,75V,5%	80009	152-0286-00
A15VR40	152-0286-00			SEMICOND DEVICE:ZENER,0.4W,75V,5%	80009	152-0286-00
A15VR58	152-0268-00			SEMICOND DEVICE:ZENER,0.4W,56V,5%	80009	152-0268-00
.						
A15W160	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
.						
.						
.						
				CHASSIS PARTS		
.						
B186	119-1672-00			FAN,TUBEAXIAL:12VDC,12400RPM		
.						
DL500	175-1477-00			CABLE,DELAY LINE:150 OHM,11NS P/F	80009	175-1477-00
.						
F010	159-0016-00			FUSE,CARTRIDGE:3AG,1.5A,250V,FAST-BLOW	71400	AGC 1 1/2
.						
J001	131-0679-02			CONNECTOR,RCPT,:BNC,MALE,3 CONTACT	24931	28JR270-1
J100	136-0801-00			JACK,TIP:BANANA,GRAY		
J102	136-0801-00			JACK,TIP:BANANA,GRAY		
J104	136-0800-00			JACK,TIP:BANANA,BLACK		
J106	131-0126-00			CONNECTOR,RCPT,:BNC,FEMALE	77820	9663-1 NT-34
J108	131-0126-00			CONNECTOR,RCPT,:BNC,FEMALE	77820	9663-1 NT-34
J112	136-0387-00			JACK,TIP:GRAY	71279	450-4352-01-0318
J301	131-0679-02			CONNECTOR,RCPT,:BNC,MALE,3 CONTACT	24931	28JR270-1
.						
L100	108-1173-00			COIL,TUBE DEFL:ROTATION		
.						
P010	131-3004-00			CONN,RCPT,ELEC:250V,6A		
.						
Q140	151-0774-00			TRANSISTOR:NPN,SI		
.						
R106	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
R108	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
.						
U120	119-0711-00			POWER SUPPLY:2KV AC P-P IN,10KV DC OUT	0000M	119-0711-00
.						
V100	154-0866-00			ELECTRON TUBE:FINISHED	80009	154-0866-00

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966 Drafting Practices.
Y14.2, 1973 Line Conventions and Lettering.
Y10.5, 1968 Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

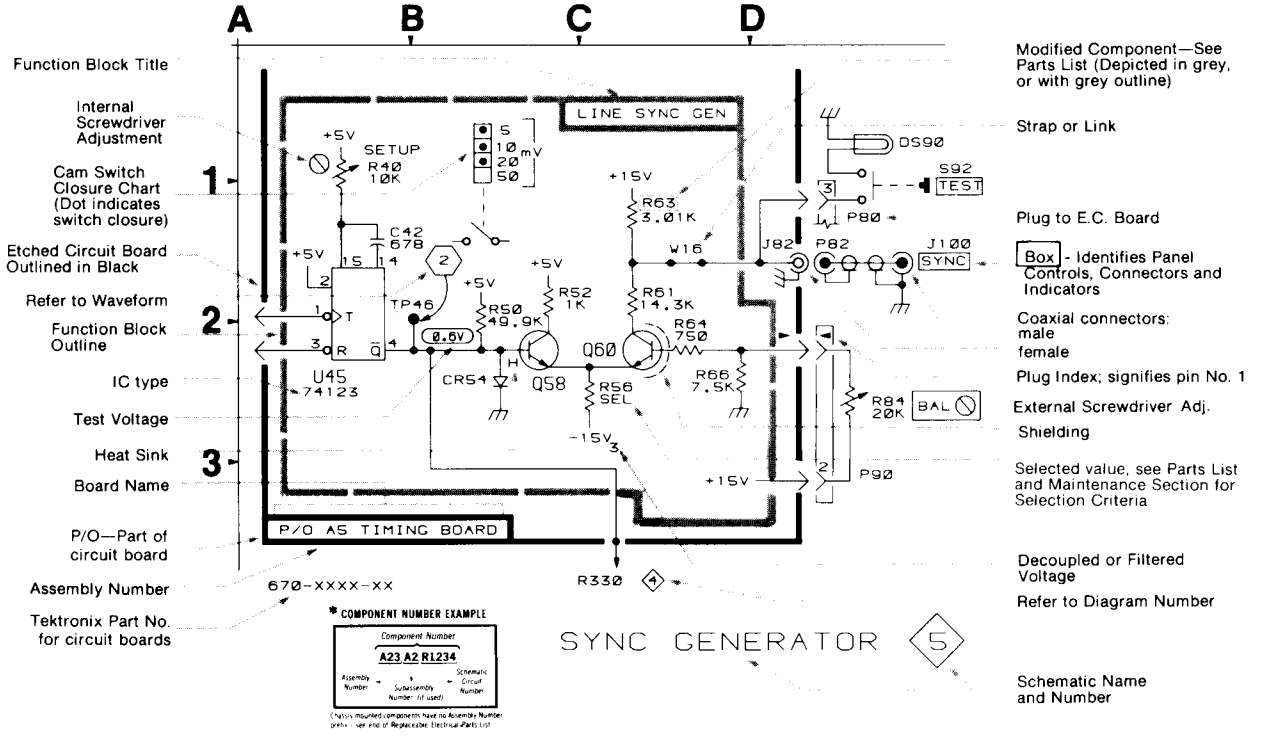
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

The information and special symbols below may appear in this manual.

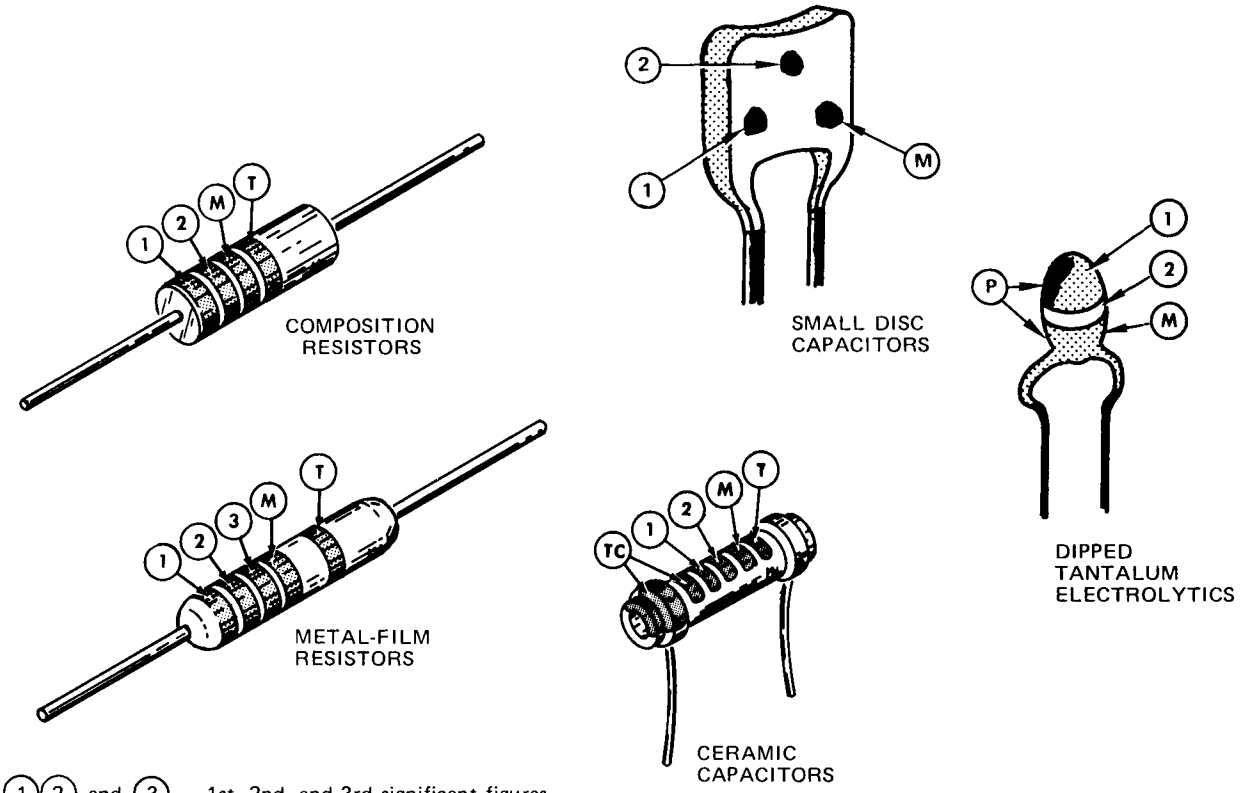
Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.



COLOR CODE



(1)(2) and (3) – 1st, 2nd, and 3rd significant figures

(M) –multiplier (T) –tolerance

(TC) –temperature coefficient

(P) –polarity and voltage rating

(T) and/or (TC) color code may not be present on some capacitors

COLOR	SIGNIFICANT FIGURES	RESISTORS		CAPACITORS			DIPPED TANTALUM VOLTAGE RATING
		MULTIPLIER	TOLERANCE	MULTIPLIER	TOLERANCE		
					over 10 pF	under 10 pF	
BLACK	0	1	---	1	±20%	±2 pF	4 VDC
BROWN	1	10	±1%	10	±1%	±0.1 pF	6 VDC
RED	2	10^2 or 100	±2%	10^2 or 100	±2%	---	10 VDC
ORANGE	3	10^3 or 1 K	±3%	10^3 or 1000	±3%	---	15 VDC
YELLOW	4	10^4 or 10 K	±4%	10^4 or 10,000	+100% –9%	---	20 VDC
GREEN	5	10^5 or 100 K	±½%	10^5 or 100,000	±5%	±0.5 pF	25 VDC
BLUE	6	10^6 or 1 M	±¼%	10^6 or 1,000,000	---	---	35 VDC
VIOLET	7	---	±1/10%	---	---	---	50 VDC
GRAY	8	---	---	10^{-2} or 0.01	+80% –20%	±0.25 pF	---
WHITE	9	---	---	10^{-1} or 0.1	±10%	±1 pF	3 VDC
GOLD	–	10^{-1} or 0.1	±5%	---	---	---	---
SILVER	–	10^{-2} or 0.01	±10%	---	---	---	---
NONE	–	---	±20%	---	±10%	±1 pF	---

(1861-20A) 2662-48

Figure 9-1. Color codes for resistors and capacitors.

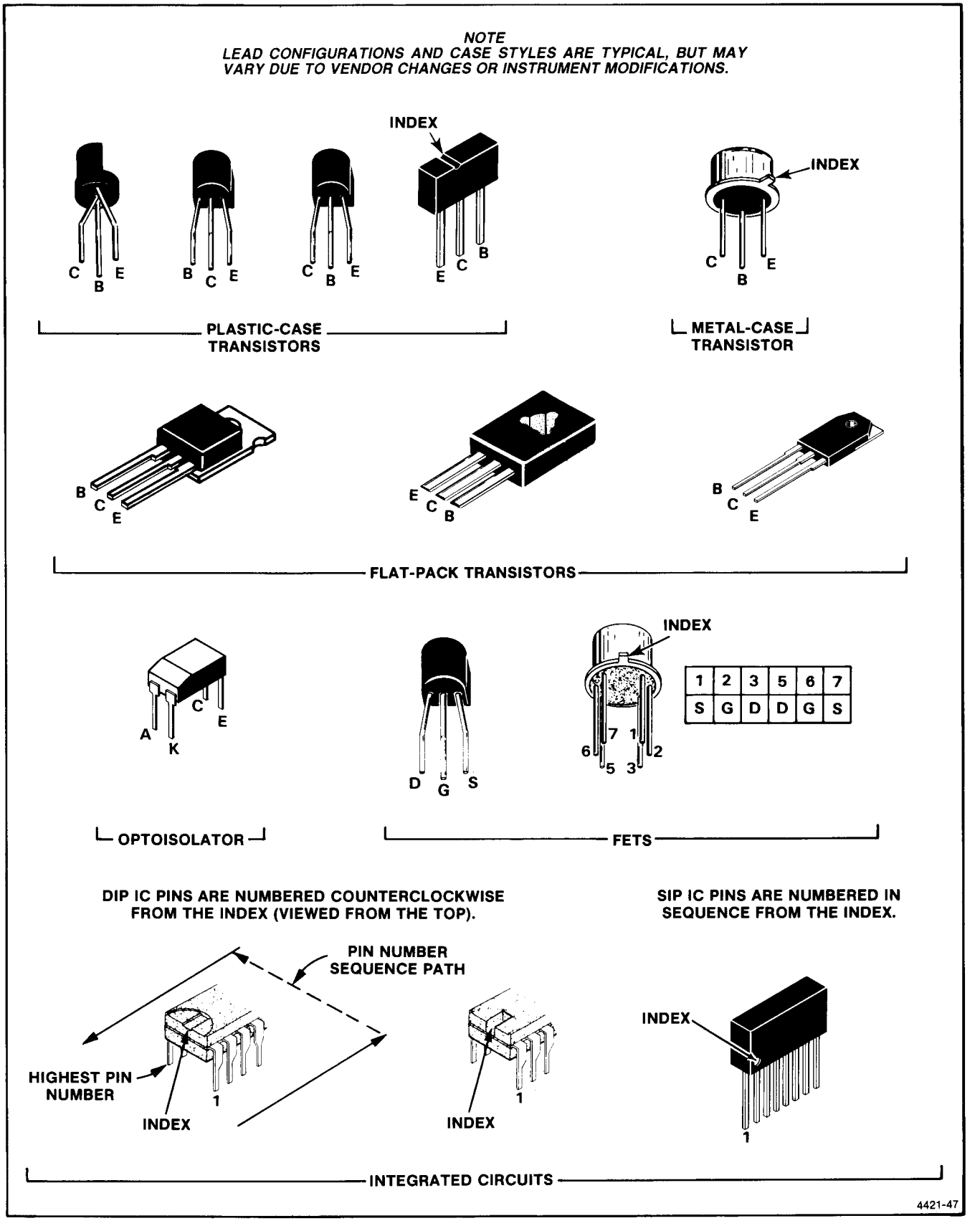


Figure 9-2. Semiconductor lead configurations.

336 Service

To identify any component mounted on a circuit board and to locate that component in the appropriate schematic diagram

1. Locate the Circuit Board Illustration

a. In the instrument identify the Assembly Number of the circuit board in question. The Assembly Number is usually printed on the upper left corner of the circuit board on the component side.

b. In the manual locate and pull out tabbed page whose title corresponds with the Assembly Number of the circuit board. Circuit board assembly numbers and board nomenclature are printed on the back side of the tabs (facing the rear of the manual).

2. Determine the Circuit Number

a. Compare the circuit board with its illustration and locate the desired component by area and shape on the illustration.

b. Scan the table adjacent to the Circuit Board Illustration and find the Circuit Number of the desired component.

c. Determine the Schematic Diagram Number in which the component is located.

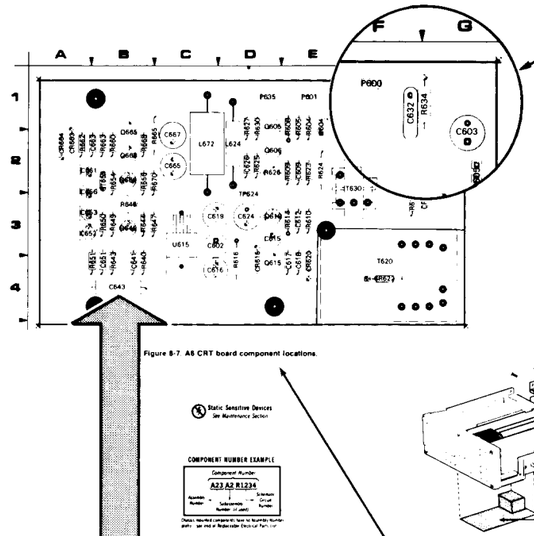
3. Lo

a.

b.

A6 CRT BOARD

A6 CRT BOARD



A6 CRT BOARD

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 10

C602	C632	Q668	R625
C603	C641		R626
C609	C643	R604	R627
C671	C651	R605	R630
C615		R608	R632
C616	Q606	R609	
C617	Q610	R610	
C618	Q615	R614	
C619	Q645	R616	
C624	Q656	R623	
C626	Q665	R624	

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 11

C670	Q670	R677	
C671	Q672	R679	
C673	Q673	R680	
C680			
C681	R671	U617	
P603	R673	U618	
P607	R674	U619	
Q669	R675		

COMPONENT LOCATION TABLE

CRT CIRCUIT DIAGRAM 10

CRT CIRCUIT DIAGRAM 10

A6 ASSEMBLY

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C602	2C	3C	Q656	2F	2B
C603	1C	1G	Q665	1G	1B
C609	4E	2E	Q668	2G	2B
C612	7C	3E			
C615	7C	3D	R604	4C	1E
C616	2C	3C	R605	5D	1E
C617	7D	3D	R608	4E	1D
C618	7E	3E	R609	4E	2D
C619	6E	3C	R610	7B	3E
C624	4F	3D	R614	7C	3D
C626	7G	2D	R616	1C	3D
C632	8G	1F	R623	4D	2E
C643	3D	4B	R625	7F	2D
C651	3E	3B	[illegible]	7F	2D
		3B	R627	7G	1D
			R630	4F	1D
Q606	4E	2D			
Q610	7C	3D	TP624	3B	2D
Q615	7D	3D			
Q645	3E	3B	U615	1D	3C

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
L635	5I	CHASSIS	V635	6J	CHASSIS

MANUAL BINDER

MANUAL BINDER

PULL OUT PAGE TABS FOR CIRCUIT BOARD ILLUSTRATION

ASSEMBLY NUMBER AND CIRCUIT BOARD NAME

ILLUSTRATION FOR INSTRUMENT CIRCUIT BOARD LOCATION

4. Determine the Circuit Board Illustration and Component Location

a. From the schematic diagram, determine the Assembly Number of the circuit board on which the component is mounted. This information is boxed and located in a corner of the heavy line that distinguishes the board outline.

b. Scan the Component Location Table for the Assembly Number just determined and find the Circuit Number of the desired component.

c. Under the BOARD LOCATION column, read the grid coordinates for the desired component.

5. Locate the Component on the Circuit Board

a. In the manual, locate and pull out the tabbed page whose title and Assembly Number correspond with the desired circuit board. This information is on the back side of the tabs.

b. Using the Circuit Number and grid coordinates, locate the component on the Circuit Board Illustration.

c. In the circuit board location illustration, determine the location of the circuit board in the instrument.

d. Find the circuit board in the instrument and compare it with its illustration in the manual to locate the desired component on the board.

Figure 9-3. Locating components on schematic diagrams and circuit board illustrations.

Determine the Circuit Number

Compare the circuit board with its illustration and locate the desired component by area and shape on the illustration.

Scan the table adjacent to the Circuit Board Illustration and find the Circuit Number of the desired component.

Determine the Schematic Diagram Number in which the component is located.

3. Locate the Component on the Schematic Diagram

a. Locate and pull out tabbed page whose number and title correspond with the Schematic Diagram Number just determined in the table. Schematic diagram nomenclature and numbers are printed on the front side of the tabs (facing the front of the manual).

b. Scan the Component Location Table adjacent to the schematic diagram and find the Circuit Number of the desired component.

c. Under the SCHEM LOCATION column, read the grid coordinates for the desired component.

d. Using the Circuit Number and grid coordinates, locate the component on the schematic diagram.

A6 CRT BOARD

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 10			
C602	C632	Q668	R625
C603	C641		R626
C609	C643	R604	R627
C671	C651	R605	R630
C615		R608	R632
C616	Q606	R609	
C617	Q610	R610	
C618	Q615	R614	
C619	Q645	R616	
C624	Q656	R623	
C626	Q665	R624	

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 11			
C670	Q670	R677	
C671	Q672	R679	
C673	Q673	R680	
C680			
C681	R671	U617	
P603	R673	U618	
P607	R674	U619	
Q669	R675		

CRT CIRCUIT DIAGRAM 10

COMPONENT LOCATION TABLE

A6 ASSEMBLY

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C602	2C	3C	Q656	2F	2B
C603	1C	1G	Q665	1G	1B
C609	4E	2E	Q668	2G	2B
C612	7C	3E			
C615	7C	3D	R604	4C	1E
C616	2C	3C	R605	5D	1E
C617	7D	3D	R608	4E	1D
C618	7E	3E	R609	4E	2D
C619	6E	3C	R610	7B	3E
C624	4F	3D	R614	7C	3D
C626	7G	2D	R616	1C	3D
C632	8G	1F	R623	4D	2E
C643	3D	4B	R625	7F	2D
C651	3E	3B	R626	7F	2D
		3B	R627	7G	1D
			R630	4F	1D
Q606	4E	2D			
Q610	7C	3D	TP624	3B	2D
Q615	7D	3D			
Q645	3E	3B	U615	1D	3C

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
L635	5I	CHASSIS	V635	6J	CHASSIS

PULL OUT PAGE TABS FOR SCHEMATIC DIAGRAMS

CRT CIRCUIT 10

SCHEMATIC DIAGRAM NAME AND NUMBER

PARTIAL A6 CRT CIRCUIT BOARD

CRT CIRCUIT 10

To identify any component in a schematic diagram and to locate that component on its respective circuit board.

MANUAL BINDER

ILLUSTRATION FOR INSTRUMENT CIRCUIT BOARD LOCATION

rd Illustration and Component

agram, determine the Assembly
oard on which the component is
on is boxed and located in a corner
istinguishes the board outline.

Location Table for the Assembly
l and find the Circuit Number of the

OCATION column, read the grid
red component.

on schematic diagrams and circuit board illustrations.

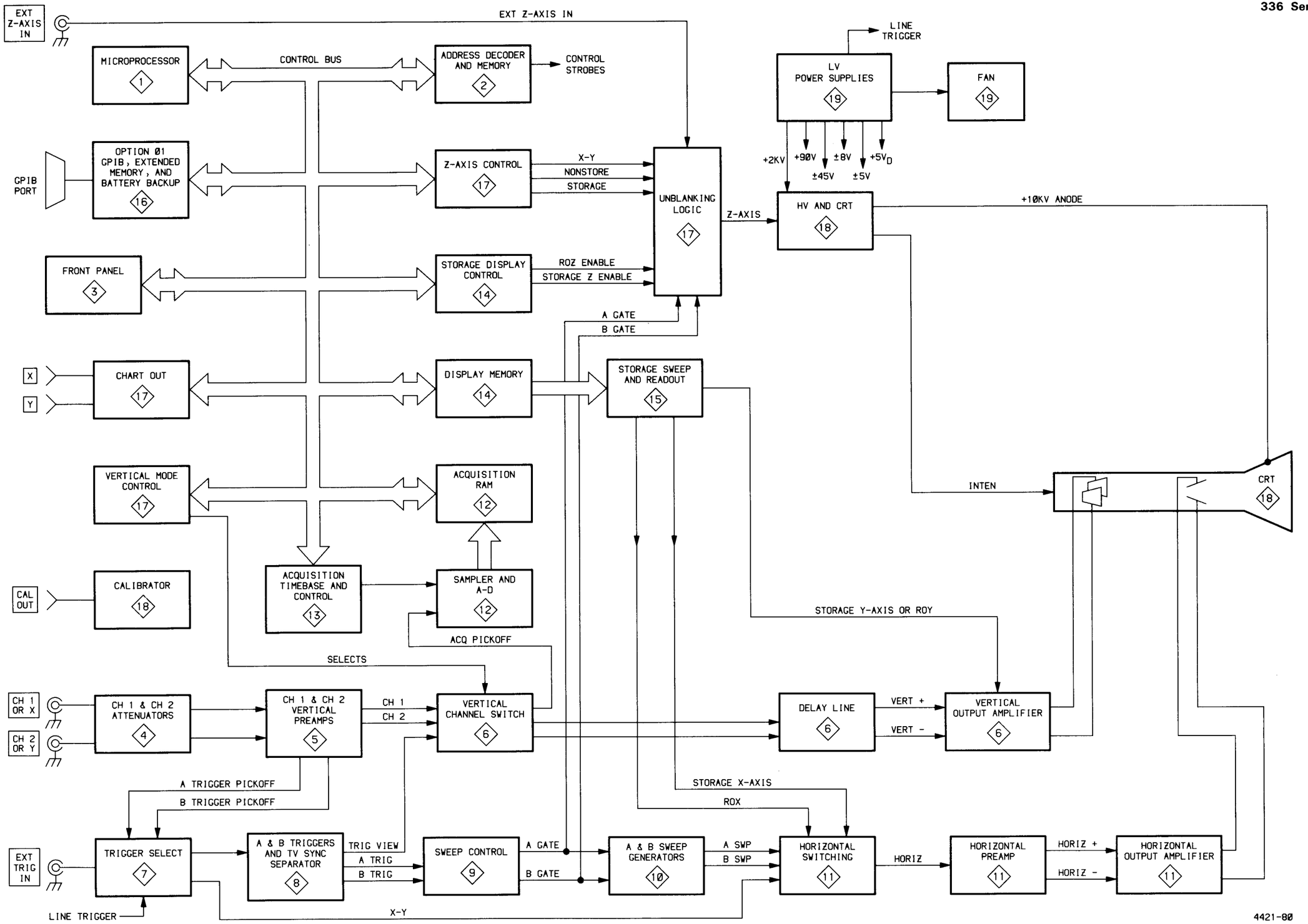


Figure 9-4. 336 block diagram.

A15 HIGH VOLTAGE REGULATOR BOARD

A12 HORIZONTAL OUTPUT BOARD

A4 CONTROL BOARD

A5 ACQUISITION BOARD

A6 DISPLAY BOARD

A7 CPU BOARD

A8 OPTION BOARD

A11 VERTICAL OUTPUT BOARD

A2 TRIGGER BOARD

A3 SWEEP BOARD

A14 PRIMARY BOARD

A13 DC/DC CONVERTER BOARD

A19 CH1 ATTENUATOR BD

A20 CH2 ATTENUATOR BD

A1 MAIN BOARD

A9 FRONT PANEL INTERFACE BOARD

A10 KEY BOARD

U100 H.V. MODULE

U120 X10

V100

L100

DELAY LINE

ANODE 10KV

(-) HORIZ

(+) HORIZ

(-) VERT

(+) VERT

EXT TRIG

GPIB

FAN B186

Q140

F10

P10

CH1 OR X

CH2 OR Y

EXT TRIG

X OUT

Y OUT

GND

CAL OUT 0.3V PK

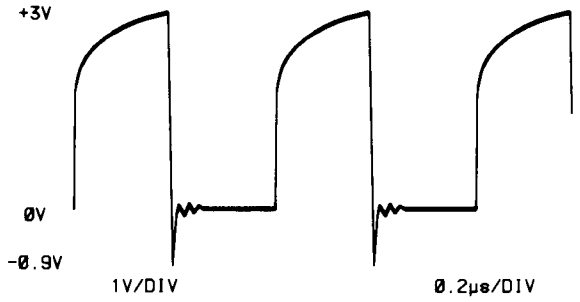
CIRCUIT BOARD INTERCONNECTIONS

4421-48

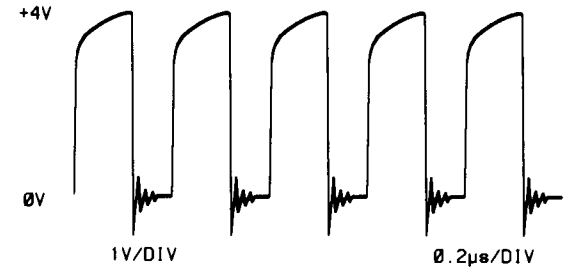
WAVEFORMS FOR DIAGRAM 1

TEST OSCILLOSCOPE TRIGGERED ON $\overline{\text{INT}}$ (WAVEFORM 4) FOR WAVEFORMS 6 THROUGH 12.

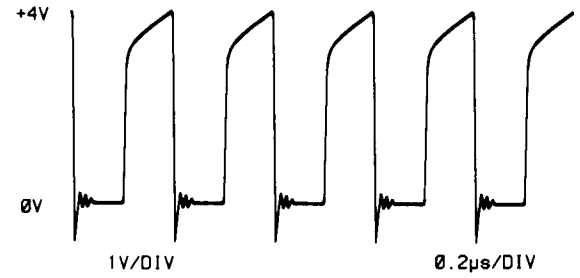
1



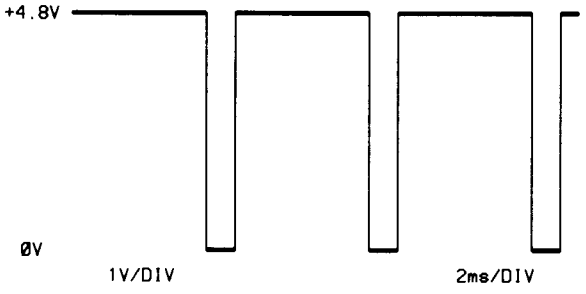
2



3



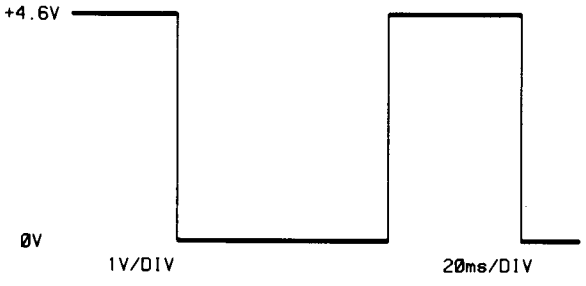
4



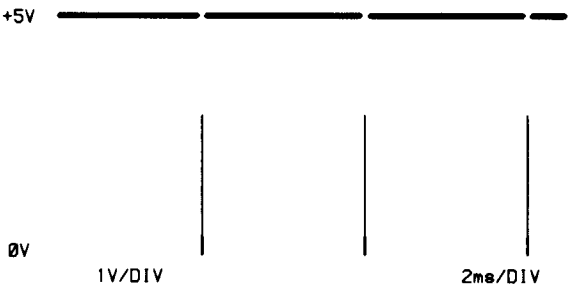
CHANGES TO 336 CONTROL SETTINGS:

VERT MODE.....CH1
HORIZONTAL DISPLAY.....A
DISPLAY MODE .....STORE

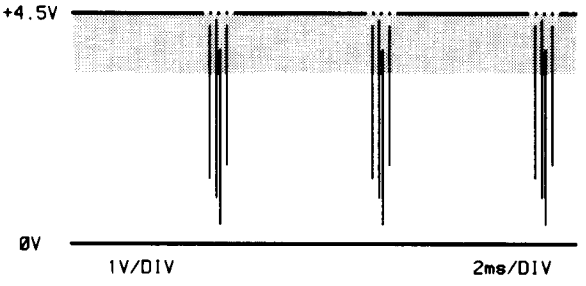
5



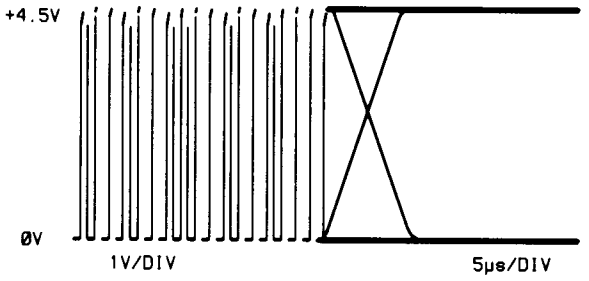
6



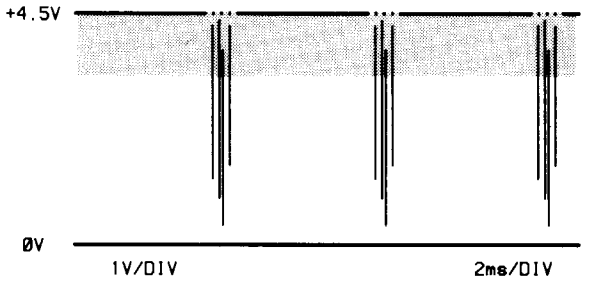
7



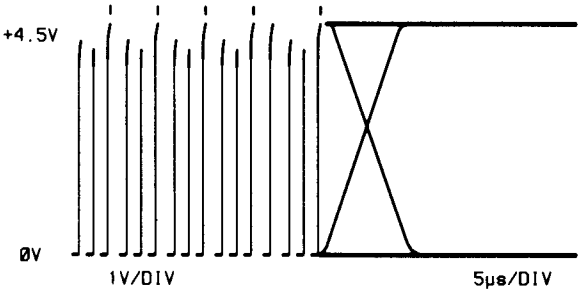
8



9



10



4421-68

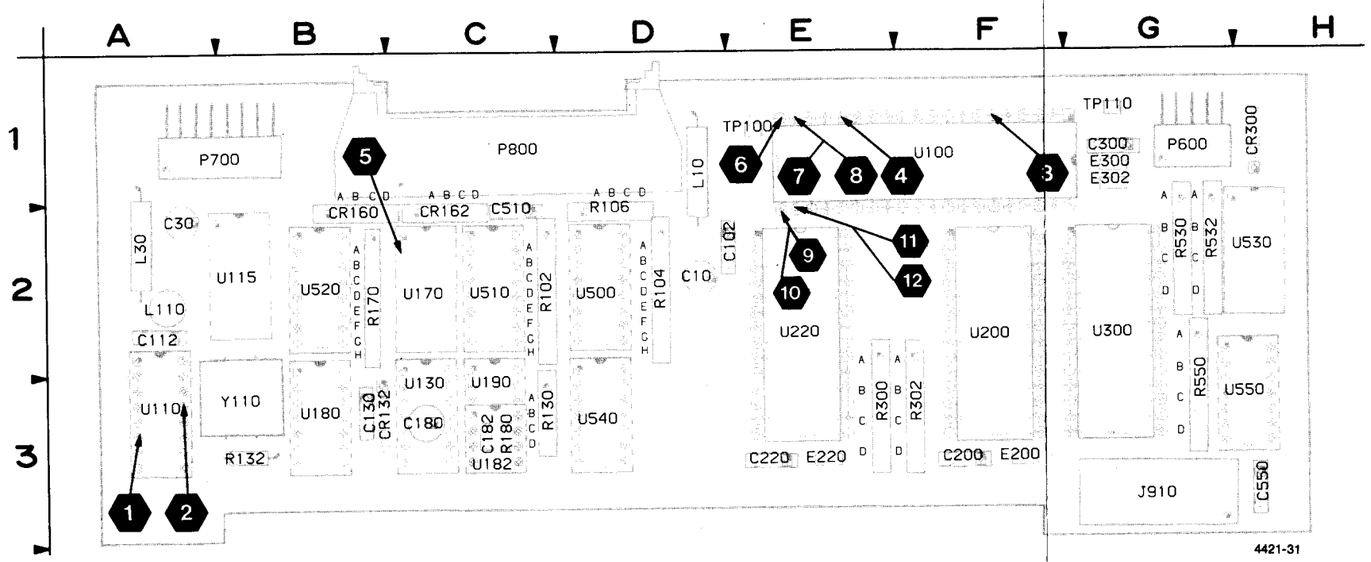
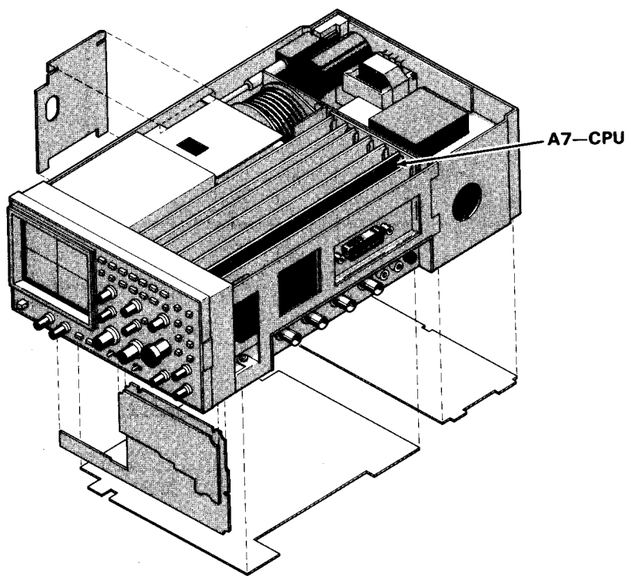
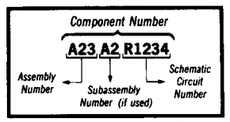


Figure 9-5. A7—CPU board.



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

A7—CPU BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C10	1	P800	1	TP110	1
C30	1	P800	2	U100	1
C102	1	R102	1	U110	1
C112	1	R104	1	U130A	1
C130	1	R106	1	U130B	1
C180	1	R130	1	U170	1
C182	1	R132	1	U180A	1
C200	1	R170A	1	U180B	1
C220	1	R170B	1	U180E	1
C300	2	R170C	1	U180F	1
C510	1	R170D	1	U182	1
C550	1	R170E	1	U190A	1
CR132	1	R170F	1	U190B	1
CR160	1	R170G	1	U190C	1
CR162	1	R180	1	U190D	1
CR300	2	R300A	2	U200	2
E200	1	R300B	2	U220	2
E220	1	R300C	2	U300	2
E300	2	R300D	2	U500A	2
E302	2	R302A	2	U500B	2
J910	1	R302B	2	U510	2
J910	1	R302C	2	U510A	2
J910	2	R302D	2	U520B	2
J910	2	R530A	2	U530	2
L10	1	R530B	2	U540A	1
L30	1	R530C	2	U540B	1
L110	1	R532A	2	U540C	1
P600	2	R532B	2	U540D	2
P700	1	R532C	2	U550	2
P700	1	R532D	2	Y110	1
P800	1	R550	2		
P800	1	TP100	1		

USE OF THE EXTENDER CIRCUIT BOARDS AND CABLES SUPPLIED IN THE SERVICE MAINTENANCE KIT PROVIDES EASE OF ACCESS TO THE WAVEFORM TEST POINTS.

TEST WAVEFORM AND VOLTAGE SETUPS

ON THE LEFT-HAND PAGES PRECEDING THE SCHEMATIC DIAGRAMS ARE ILLUSTRATIONS OF TEST WAVEFORMS THAT ARE INTENDED TO AID IN TROUBLESHOOTING THE INSTRUMENT. THE FOLLOWING INITIAL SETUP OF THE 336 ESTABLISHES CONDITIONS TO OBTAIN THOSE WAVEFORMS. CHANGES TO THESE SETUPS TO OBTAIN SPECIFIC WAFEFORMS ARE NOTED NEAR THOSE WAVEFORMS. VOLTS/DIV AND SEC/DIV SETTINGS FOR THE TEST OSCILLOSCOPE ARE NOTED ON THE ILLUSTRATIONS.

336 INITIAL CONTROL SETTINGS

VERTICAL
- VOLTS/DIV (both).....0.5V
- VAR VOLTS/DIV (both).....CAL (in detent)
- VERT MODE.....DUAL TRACE
- CH 2 INV.....Noninverted (no down arrow displayed with the CH 2 readout)
- POSITION (both).....Midrange

TRIGGER
- MODE.....AUTO
- SOURCE.....CH 1
- COUPLING.....AC
- A LEVEL.....For a stable triggered display
- B LEVEL.....RUNS AFTER DELAY

HORIZONTAL
- Display Mode.....ALT (SEC/DIV knob out)

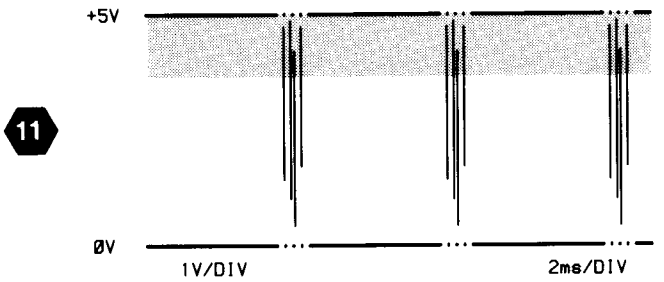
HORIZONTAL (CONT)
- A SEC/DIV.....0.5ms
- B SEC/DIV.....0.2ms
- Delay Time.....Minimum (press left DLY TIME/CURSOR position button until readout stops changing)
- VAR SWP/HOLDOFF.....CAL/NORM (in detent)
- X10 MAG.....Off
- POSITION.....Midrange
- DISPLAY MODE.....NON STORE

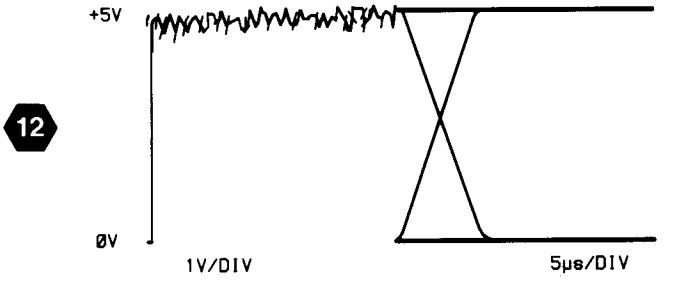
Main MENU Selections
- READOUT.....ON
- STORAGE DISPLAY.....TIME
- TIME OUT.....SLOW
- STORE MODE.....NORMAL

Display Signal.....Any triggerable signal

DC VOLTAGE MEASUREMENTS

TYPICAL VOLTAGE MEASUREMENTS WERE OBTAINED WITH THE 336 OPERATING UNDER NORMAL OPERATING CONDITIONS. THE VOLTAGES INDICATED ON THE SCHEMATIC DIAGRAMS ARE TAKEN WITH REFERENCE TO CHASSIS GROUND AND ROUNDED TO THE NEAREST ±5%.





MICROPROCESSOR 1

ASSEMBLY A1

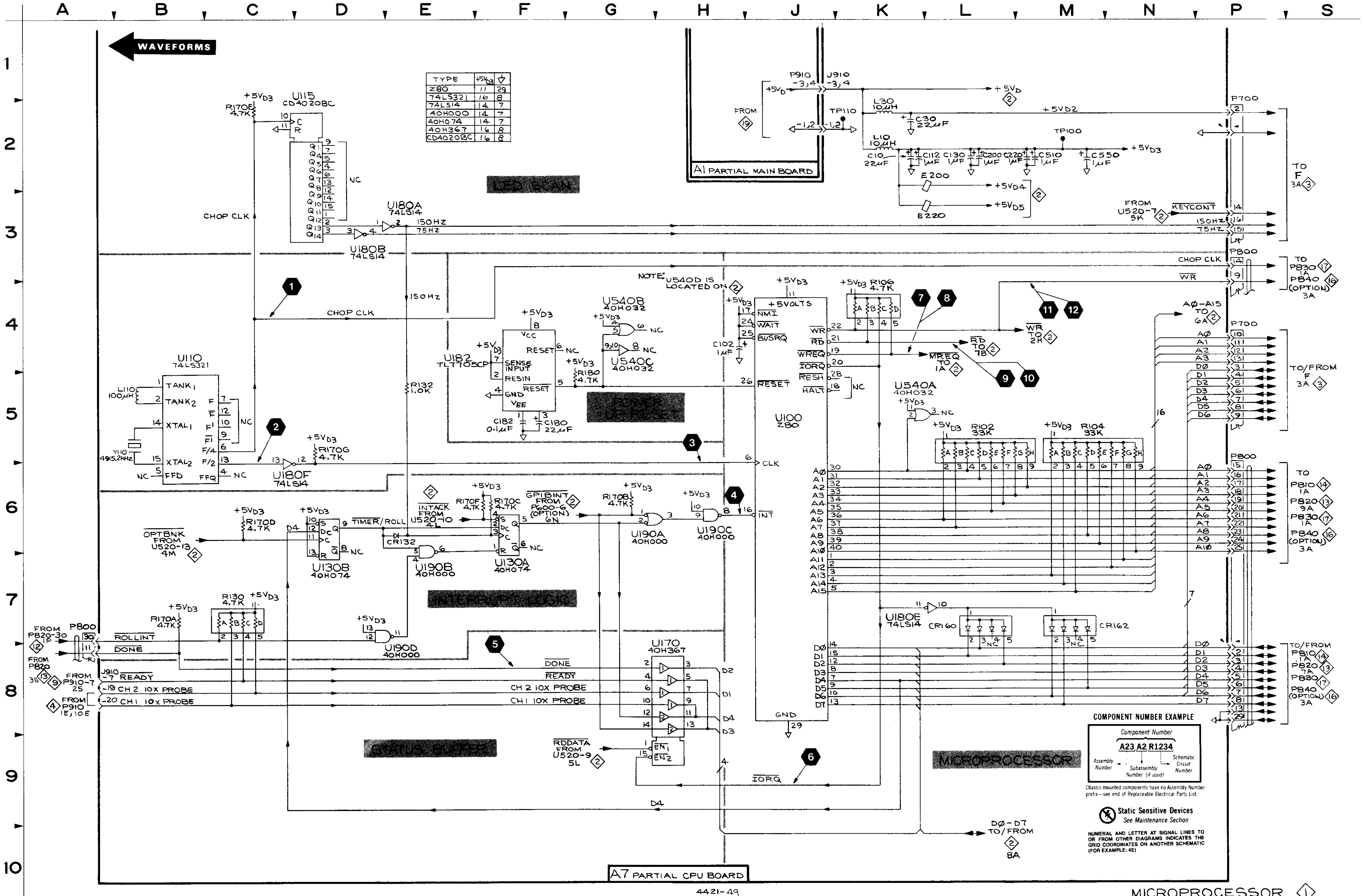
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P910	1J	2G			

Partial A1 also shown on diagrams 2, 3, 4, 5, 6, 7, 9, 11, 12, 13, 15, 17, 18 and 19.

ASSEMBLY A7

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C10	2K	2D	R106	4K	2D
C30	2K	2A	R130	7C	3C
C102	4H	2E	R132	5E	3B
C112	2L	2A	R170A	7B	2B
C130	2L	3B	R170B	6G	2B
C180	5F	3C	R170C	6F	2B
C182	5F	3C	R170D	6C	2B
C200	2L	3F	R170E	2C	2B
C220	2L	3E	R170F	6E	2B
C510	2M	2C	R170G	5D	2B
C550	2M	3H	R180	5G	3C
CR132	6E	3B	TP100	2M	1E
CR160	7L	2B	TP110	2J	1G
CR162	7M	2C			
			U100	5J	1F
E200	2L	3F	U110	4B	3A
E220	3K	3E	U130A	7F	3C
			U130B	7D	3C
J910	1J	3G	U170	8H	2C
J910	8A	3G	U180A	3E	3B
			U180B	3D	3B
L10	2K	1D	U180E	7L	3B
L30	2K	2A	U180F	6D	3B
L110	5B	2A	U182	4E	3C
			U190A	6G	3C
P700	1P	1B	U190B	7E	3C
P700	4P	1B	U190C	6H	3C
P800	3P	1C	U190D	8E	3C
P800	5P	1C	U540A	5K	3D
P800	7A	1C	U540B	4G	3D
			U540C	4G	3D
R102	5L	2C			
R104	5M	2D	Y110	5B	3B

Partial A7 also shown on diagram 2.


WAVEFORMS
TYPE | +5VD3 | GND
Z80 11 29
74LS321 16 8
74LS14 14 7
40H000 14 7
40H074 14 7
40H367 16 8
CD4020BC 16 8
LED SCAN
POWER UP RESET
INTERRUPT LOGIC
STATUS BUFFER
MICROPROCESSOR
A1 PARTIAL MAIN BOARD
A7 PARTIAL CPU BOARD
U115 CD4020BC
U110 74LS321
U180A 74LS14
U180B 74LS14
U180E 74LS14
U180F 74LS14
U182 TL7705CP
U540B 40H032
U540C 40H032
U540A 40H032
U100 Z80
U130A 40H074
U130B 40H074
U190A 40H000
U190B 40H000
U190C 40H000
U190D 40H000
U170 40H367
CHOP CLK
150HZ
75HZ
NOTE: U540D IS LOCATED ON 2
+5VD
+5VD2
+5VD3
+5VD4
+5VD5
P910 -3,4
J910 -3,4
FROM 19
TP110
TP100
L30 10µH
L10 10µH
C30 22µF
C10 22µF
C112 1µF
C130 1µF
C200 1µF
C220 1µF
C510 1µF
C550 1µF
E200
E220
FROM U520-7 5K 2
KEYCONT
P700
P800
TO F 3A 3
TO P830 1A 17 P840 16 (OPTION) 3A
WR
RD TO 7B 2
WR TO 2H 2
MREQ TO 1A 2
IORQ
A0-A15 TO 6A 2
TO/FROM F 3A 3
TO P810 14 1A P820 13 9A P830 17 1A P840 16 (OPTION) 3A
TO/FROM P810 14 1A P820 13 7A P830 17 P840 16 (OPTION) 3A
D0-D7 TO/FROM 2 8A
R170E 4.7K
R170G 4.7K
R170D 4.7K
R170F 4.7K
R170C 4.7K
R170B 4.7K
R170A 4.7K
R130 4.7K
R132 1.0K
R180 4.7K
R106 4.7K
R102 33K
R104 33K
CR132
CR160
CR162
C102 1µF
C182 0.1µF
C180 22µF
L110 100µH
Y110 4915.2kHz
TIMER/ROLL
INTACK FROM U520-10 4L
GPIBINT FROM P600-6 (OPTION) 6N
OPTBNK FROM U520-13 4M 2
RDDATA FROM U520-9 5L 2
ROLLINT
DONE
READY
CH 2 10X PROBE
CH 1 10X PROBE
FROM P820-30 1P 12
FROM P820 3S 13
FROM P910-7 2S 9
FROM P910 1E, 10E 4
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)
4421-49
MICROPROCESSOR 1

ADDRESS DECODER & MEMORY

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P910	2N	2G	P960	2N	4G
P950	3P	4G			

Partial A1 also shown on diagrams 1, 3, 4, 5, 6, 7, 9, 11, 12, 13, 15, 17, 18 and 19.

ASSEMBLY A7

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C300	8M	1G	R530C	3K	2G
			R532A	3L	2G
CR300	7M	1H	R532B	3K	2G
			R532C	4L	2G
E300	7M	1G	R532D	3L	2G
E302	7M	1G	R550A	8M	3G
			R550B	9M	3G
J910	2N	3G	R550C	10M	3G
J910	8M	3G			
			U200	9D	2F
P600	6N	1G	U220	9F	2E
P800	4N	1C	U300	9H	2G
			U500A	1D	2D
R300A	9B	3E	U500B	1B	2D
R300B	8B	3E	U510A	2G	2C
R300C	8B	3E	U510B	1E	2C
R300D	8B	3E	U520	4J	2B
R302A	9B	3F	U530	2J	2H
R302B	9B	3F	U540D	7C	3D
R302C	9B	3F	U550A	10L	3H
R302D	8B	3F	U550B	9L	3H
R530A	2K	2G	U550C	10L	3H
R530B	3K	2G	U550D	8L	3H

Partial A7 also shown on diagram 1.

ASSEMBLY A8

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
W600	6P	1G			

Partial A8 also shown on diagram 16.

TYPE	+5V$_{D2}$	+5V$_{D4}$	+5V$_{D5}$	+5V$_{I3}$	▽
40H032	14				7
40H138	16				8
40H139	16				8
HN613128P			1,28		14
HN613256		1,28			14
TC5565P				1	14

U500B 40H139 · U500A 40H139 · U510B 40H139 · U510A 40H139 · U530 40H138 · U520 40H138

MREQ FROM U100-19 4L ◇1

WR FROM U100-22 4M ◇1

RD FROM U100-21 4L ◇1

A0-A15 FROM 4N ◇1

D0-D7 TO/FROM 10L ◇1

+5VD3 → +5VD3 · +5VD4 → +5VD4 · +5VD5 → +5VD5 FROM ◇1

ROM2 · SYS · OPTRAM · MREQ · WRDISP

NOTE: U540A,B & C ARE LOCATED ON ◇1

U540D 40H032 · U200 HN613256 · U220 HN613128P · U300 TC5565P

R300B 1.0K · R300C 1.0K · R300D 1.0K · R302D 1.0K · R302C 1.0K · R302B 1.0K · R302A 1.0K · R300A 1.0K

R530A 1K · R530B 1K · R530C 1K · R532B 1K · R532D 1K · R532A 1K · R532C 1K

TSOURCE · TCOUPLE · SWP HD LATCH · PREAMP · SWP CONTROL LATCH · TIMING CURRENT LATCH · ATT

A1 PARTIAL MAIN BOARD

J910 P910 P960

TO J960-9 4A ◇7 · TO J960-10 4A ◇7 · TO J950-20 8A ◇10 · TO U430-14 4A ◇5 · TO J950-17 1A ◇10 · TO J950-19 2A ◇10 · TO U50-14 2B ◇4

P800

RDACQ · WPMCTRL · OPTBNK · H-VMODE CONT · TALKCONT · INTACK · RDDATA · KEYCONT

TO U130-11 6B ◇1 · TO U130-4 6E ◇1 · TO U170-1 9G ◇1 · TO P700-14 3N ◇1

TO P820-26 ◇13 · TO P810-28 5A ◇14 & P820-28 9A ◇13 · TO P830-12 5A ◇17 · TO P810-27 2A ◇14

OPTBNK · TALKCONT · OPTRAM · GPIBINT TO U190-1 6F ◇1 · RD · SYS · SYSB · +5V13 · J604 · +5VD · E302 E300 CR300 · C300 1μF · J602 · FROM ◇1

P600 W600

-3 OPTBNK TO U140-9 3H · -4 TALKCONT TO U400-8 9F · -2 OPTRAM TO U130-2 2H · -6 GPIBINT FROM U400-11 9F · -5 RD TO U400-9 8F · -8 SYS TO U130-14 2H · -7 SYSB FROM U130-13 2K · -9 +5V11 · -10 +5VD ◇10

A8 PARTIAL OPTION BOARD

OPTION

NOTE: J602 & J604 ARE USED WHEN OPTION IS NOT PRESENT.

U550D 40H032 · U550B 40H032 · U550A 40H032 · U550C 40H032

R550A 1.0K · R550B 1.0K · R550D 1.0K · R550C 1.0K

TO P910 3A ◇4

ADDRESS DECODER · MEMORY

A7 PARTIAL CPU BOARD

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234 (Assembly Number · Subassembly Number (if used) · Schematic Circuit Number)

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices — See Maintenance Section

NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)

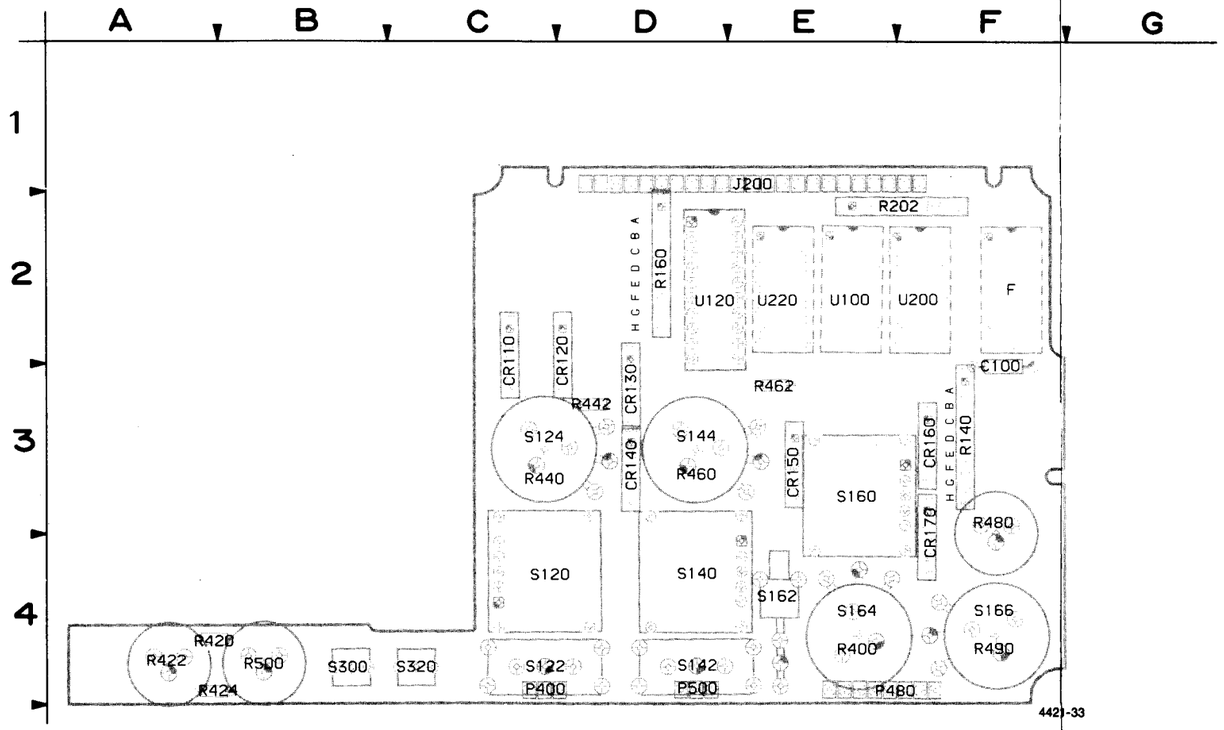
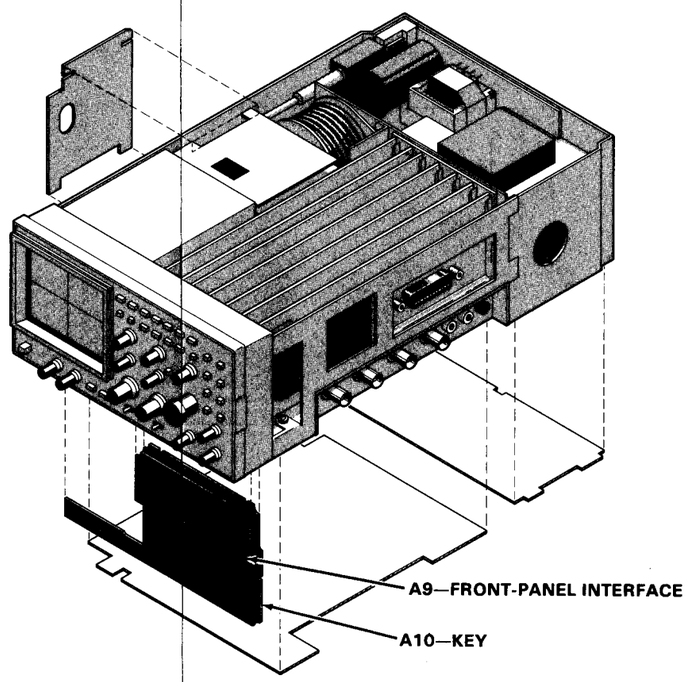


Figure 9-6. A9—Front Panel Interface board.

A9—FRONT PANEL INTERFACE BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C100	3	R420	3
CR110	3	R422	3
CR130	3	R424	3
CR140	3	R440	3
CR150	3	R442	3
CR160	3	R460	3
CR170	3	R462	3
F	3	R480	3
J200	3	R490	3
J200	3	R500	3
P400	3	S120	3
P400	3	S122	3
P480	3	S124	3
P480	3	S140	3
P500	3	S142	3
P500	3	S144	3
R140	3	S160	3
R160A	3	S162	3
R160B	3	S164	3
R160C	3	S166	3
R160D	3	S300	3
R160E	3	S320	3
R160F	3	U100	3
R160G	3	U100	3
R160H	3	U120	3
R202	3	U200	3
R400	3	U220	3



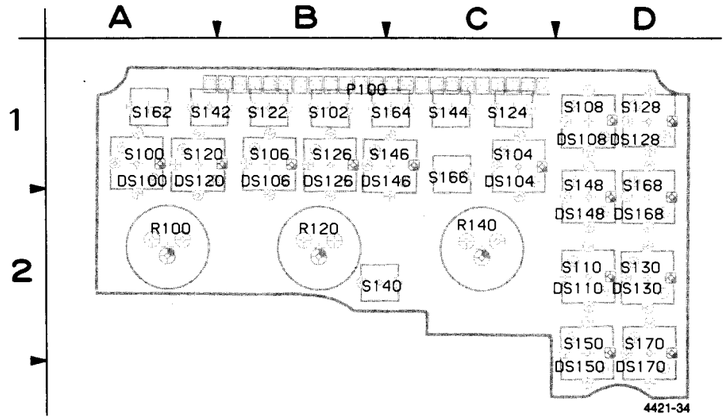
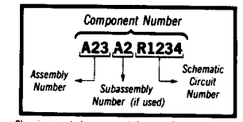


Figure 9-7. A10—Key board.

A10—KEY BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
DS100	3	S104	3
DS104	3	S106	3
DS106	3	S108	3
DS108	3	S110	3
DS110	3	S120	3
DS120	3	S122	3
DS126	3	S124	3
DS128	3	S126	3
DS130	3	S128	3
DS146	3	S130	3
DS148	3	S140	3
DS150	3	S142	3
DS168	3	S144	3
DS170	3	S146	3
P100	3	S148	3
P100	3	S150	3
R100	3	S162	3
R120	3	S164	3
R140	3	S166	3
S100	3	S168	3
S102	3	S170	3

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

KEYBOARD & INTERFACE

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
ME	2J	5A	MG MG8	1C 3C	5A 4A	P962	1B	4A			

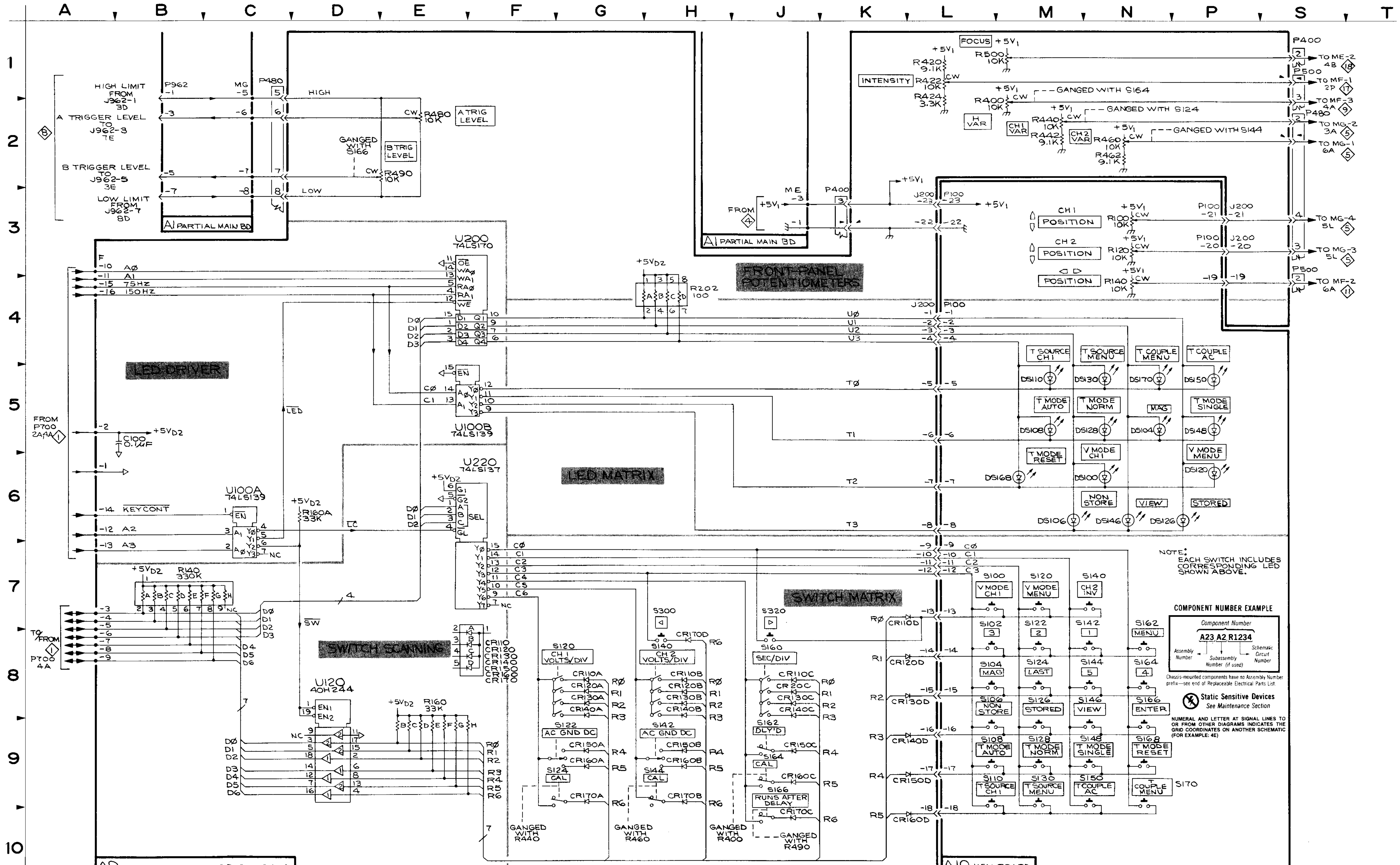
Partial A1 also shown on diagrams 1, 2, 4, 5, 6, 7, 9, 11, 12, 13, 15, 17, 18 and 19.

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	5B	2F	CR150D	9K	3E	R140	7B	3F	S120	8G	4C
			CR160A	9G	3F	R160A	6D	2D	S122	9G	4C
CR110A	8G	2C	CR160B	9H	3F	R160B	8E	2D	S124	9G	3C
CR110B	8H	2C	CR160C	9J	3F	R160C	8E	2D	S140	8H	4D
CR110C	8J	2C	CR160D	10K	3F	R160D	8E	2D	S142	9H	4D
CR110D	7K	2C	CR170A	9G	3F	R160E	8E	2D	S144	9H	3D
CR120A	8G	3D	CR170B	9H	3F	R160F	8E	2D	S160	8J	3E
CR120B	8H	3D	CR170C	9J	3F	R160G	8E	2D	S162	9J	4E
CR120C	8J	3D	CR170D	8H	3F	R160H	8E	2D	S164	9J	4E
CR120D	8K	3D				R202	4H	2E	S166	9J	4F
CR130A	8G	3D	F	4A	2F	R400	1L	4E	S300	7H	4B
CR130B	8H	3D				R420	1L	4A	S320	7J	4C
CR130C	8J	3D	J200	3P	1E	R422	1L	4A			
CR130D	8K	3D	J200	4L	1E	R424	1L	4A	U100A	6C	2E
CR140A	8G	3D				R440	2M	3C	U100B	5E	2E
CR140B	8H	3D	P400	1S	4C	R442	2M	3D	U120	8D	2D
CR140C	8J	3D	P400	2K	4C	R460	2N	3D	U200	3F	2F
CR140D	9K	3D	P480	1C	4E	R462	2N	3E	U220	6F	2E
CR150A	9G	3E	P480	2S	4E	R480	2E	3F			
CR150B	9H	3E	P500	1S	4D	R490	2E	4F			
CR150C	9J	3E	P500	3S	4D	R500	1L	4B			

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
DS100	6M	1A	DS168	6M	2D	S104	8L	1C	S144	8N	1C
DS104	5N	1C	DS170	5N	2D	S106	8L	1B	S146	8N	1B
DS106	6M	1B				S108	9L	1D	S148	9N	1D
DS108	5M	1D	P100	3P	1B	S110	9L	2D	S150	9N	2D
DS110	5M	2D	P100	4L	1B	S120	7M	1A	S162	7N	1A
DS120	6P	1A				S122	7M	1B	S164	8N	1B
DS126	6N	1B	R100	3N	2A	S124	8M	1C	S166	8N	1C
DS128	5N	1D	R120	3N	2B	S126	8M	1B	S168	9N	1D
DS130	5N	2D	R140	3N	2C	S128	9M	1D	S170	9N	2D
DS146	6N	1B				S130	9M	2D			
DS148	5N	2D	S100	7L	1A	S140	7N	2B			
DS150	5N	2D	S102	7L	1B	S142	7N	1A			



4421-51

KEYBOARD & INTERFACE 3

A1—MAIN, A19 & A20—ATTENUATOR BOARDS FIG. 9-8

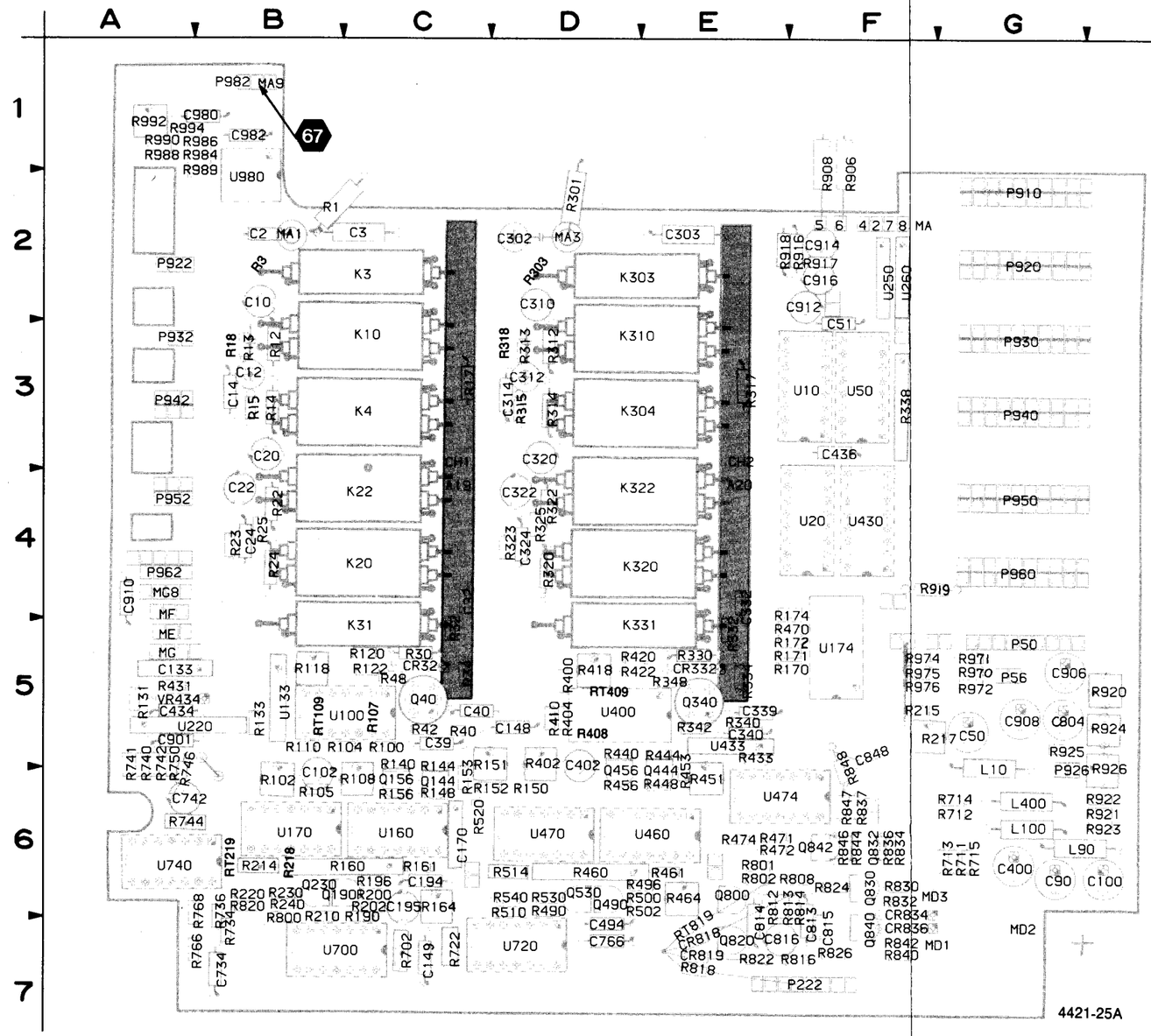


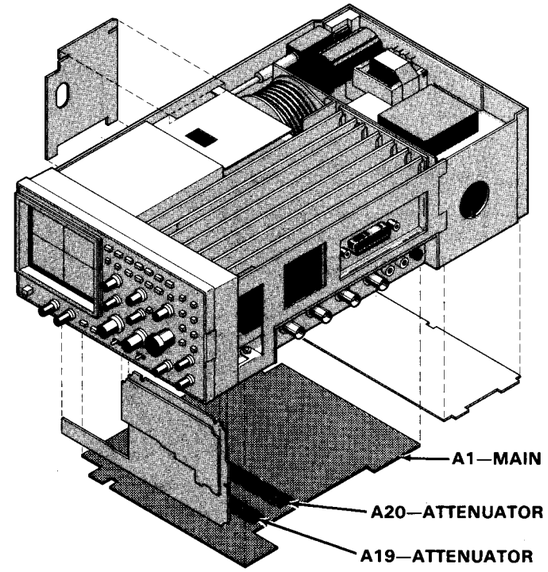
Figure 9-8. A1—Main board, A19 & A20—Attenuator boards.

A19—ATTENUATOR BOARD

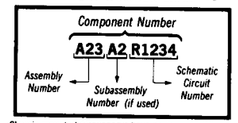
CIRCUIT NUMBER	SCHEM NUMBER
C32	4
R17	4
R32	4
R34	4

A20—ATTENUATOR BOARD

CIRCUIT NUMBER	SCHEM NUMBER
C332	4
R317	4
R332	4
R334	4



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

A1—MAIN BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C2	4	MA	17	R30	4	R456	5	R986	18
C3	4	MA	18	R40	4	R460A	5	R988	18
C10	4	MA1	4	R42	4	R460B	5	R990	18
C12	4	MA3	4	R48	4	R460C	5	R992	18
C14	4	MA9	18	R100	5	R460D	5	R994	18
C20	4	MD1	6	R102	5	R460E	5	RT109	5
C22	4	MD2	6	R104	5	R460F	5	RT218	5
C24	4	MD3	6	R105	5	R460G	5	RT409	5
C39	4	ME	3	R107	5	R461	5	U10	4
C40	4	ME	18	R108	5	R464	5	U20	4
C50	4	MF	9	R110	5	R470	5	U50	4
C51	4	MF	11	R118	5	R471	5	U100A	5
C90	4	MF	17	R120	5	R472	5	U100B	5
C100	4	MG	3	R122	5	R474	5	U100C	5
C102	5	MG	5	R131	5	R490	5	U100D	5
C133A	5	MG8	3	R133	5	R496	5	U100E	5
C133B	5	P50	19	R140	5	R500	5	U100F	5
C133C	5	P50	19	R144	5	R502	5	U133A	5
C133D	5	P56	7	R148	5	R510	5	U133B	5
C144	4	P56	19	R150	5	R514	5	U160A	5
C148	4	P222	15	R151	5	R520	5	U160B	5
C149	4	P222	17	R152	5	R530	5	U160C	5
C170	5	P910	1	R153	5	R540	5	U160D	5
C194	5	P910	2	R156	5	R711	6	U170A	5
C195	5	P910	4	R160A	5	R712	6	U170B	5
C302	4	P910	9	R160B	5	R713	6	U170C	5
C303	4	P920	11	R160C	5	R714	6	U170D	5
C310	4	P920	15	R160D	5	R715	6	U174	5
C312	4	P922	17	R160E	5	R722	6	U220A	5
C314	4	P922	18	R160F	5	R734	6	U220B	5
C320	4	P926	18	R160G	5	R736	6	U250	4
C322	4	P930	6	R161	5	R740	6	U260	4
C324	4	P930	12	R164	5	R741	6	U400A	5
C339	4	P930	13	R170	5	R742	6	U400B	5
C340	4	P932	17	R171	5	R744	6	U400C	5
C400	4	P940	6	R172	5	R746	6	U400D	5
C402	5	P940	11	R174	5	R750	6	U400E	5
C434	4	P940	13	R190	5	R766	6	U400F	5
C436	4	P940	17	R196	5	R768	6	U430	5
C494	5	P942	11	R200	5	R800	6	U433A	5
C700	6	P942	17	R202	5	R801	6	U433B	5
C720	6	P942	17	R210	5	R802	6	U460A	5
C734	6	P950	2	R214	5	R808	6	U460B	5
C744	6	P950	5	R215	5	R812	6	U460C	5
C766	6	P950	9	R217	5	R813	6	U460D	5
C813	6	P950	13	R218	5	R814	6	U470A	5
C814	6	P952	9	R220	5	R816	6	U470B	5
C815	6	P952	17	R230	5	R820	6	U470C	5
C816	6	P960	2	R240	5	R822	6	U470D	5
C848	6	P960	5	R301	4	R824	6	U474	5
C901	18	P960	7	R312	4	R826	6	U700A	6
C906	4	P960	17	R313	4	R830	6	U700B	6
C908	4	P962	3	R314	4	R832	6	U700C	6
C910	4	P962	6	R315	4	R834	6	U700D	6
C912	7	P962	9	R322	4	R836	6	U700E	6
C914	7	P982	4	R323	4	R837	6	U700F	6
C916	7	Q40	4	R324	4	R840	6	U720A	6
C980	18	Q144	5	R325	4	R842	6	U720B	6
C982	18	Q156	5	R330	4	R844	6	U720C	6
CR32	4	Q190	5	R338A	4	R846	6	U720D	6
CR332	4	Q230	5	R338B	4	R847	6	U720E	6
CR818	6	Q340	4	R338C	4	R848	6	U720F	6
CR819	6	Q444	5	R338D	4	R906	17	U740A	6
CR834	6	Q456	5	R338E	4	R908	7	U740B	6
CR836	6	Q490	5	R338F	5	R916	7	U740C	6
K3	4	Q530	5	R340	4	R917	7	U740D	6
K4	4	Q800	6	R342	4	R918	7	U740E	6
K10	4	Q820	6	R348	4	R919	7	U740F	6
K20	4	Q830	6	R400	5	R920	17	U980	18
K22	4	Q832	6	R402	5	R921	17	VR434	4
K31	4	Q840	6	R404	5	R922	17		
K303	4	Q842	6	R408	5	R923	17		
K304	4	R1	4	R410	5	R924	17		
K310	4	R3	4	R418	5	R925	17		
K320	4	R12	4	R420	5	R926	18		
K322	4	R13	4	R422	5	R970	5		
K331	4	R14	4	R431	5	R971	5		
L10	4	R15	4	R433	5	R972	5		
L90	4	R18	4	R440	5	R974	5		
L100	4	R22	4	R444	5	R975	5		
L400	4	R23	4	R448	5	R976	5		
MA0	4	R24	4	R451	5	R982	18		
MA0	17	R25	4	R453	5	R984	18		

CH 1 & CH 2 ATTENUATORS

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C2	3F	2B	C434	7B	5A	MA	9C	2F	R312	8G	3D
C3	2E	2C	C436	7B	3F	MA1	1B	2B	R313	8H	3D
C10	3G	2B	C906	6A	5G	MA3	8B	2D	R314	8G	3D
C12	3G	3B	C908	7B	5G				R315	7H	3D
C14	4H	3B	C910	8A	4A	P910	1E	2G	R318	8H	3D
C20	3K	3B				P910	2A	2G	R322	8K	4D
C22	3K	4B	CR32	1N	5C	P910	9E	2G	R323	8L	4D
C24	3L	4B	CR332	9N	5E	P982	1B	1B	R324	8K	4D
C39	7C	5C							R325	8K	4D
C40	1P	5C	K3	3F	2C	Q40A	2P	5C	R330	9M	5E
C50	7B	5G	K4	3H	3C	Q40B	2P	5C	R338A	2B	3F
C51	3E	2F	K10	3F	3C	Q340A	9P	5E	R338B	2B	3F
C90	6B	6G	K20	3L	4C	Q340B	9P	5E	R338C	2B	3F
C100	7B	6H	K22	3J	4C	R1	2B	2B	R338D	2B	3F
C144	6B	7C	K31	3N	5C	R3	3F	2B	R338E	2C	3F
C148	8B	5D	K303	7F	2D	R12	3G	3B	R340	8P	5E
C149	6C	7C	K304	7H	3D	R13	3H	3B	R342	9P	5E
C302	8F	2D	K310	7F	3D	R14	3H	3B	R348	10P	5E
C303	9E	2E	K320	7L	4E	R15	3H	3B			
C310	8G	2D	K322	7J	4E	R18	4H	3B	U10	3D	3F
C312	7G	3D	K331	7M	5E	R22	3K	4B	U20	5D	4E
C314	8H	3D				R23	4L	4B	U50	3D	3F
C320	8K	3D	L10	7B	6G	R24	4L	4B	U250	1D	2F
C322	7J	4D	L90	6B	6H	R25	3L	4B	U260	9D	2F
C324	8L	4D	L100	7B	6G	R30	2M	5C			
C339	7C	5E	L400	8B	6G	R40	1P	5C	VR434	6C	5A
C340	8P	5E				R42	2P	5C			
C400	8B	6G	MA	1C	2F	R48	3P	5C			
						R301	9B	2D			
						R303	7F	2D			

Partial A1 also shown on diagrams 1, 2, 3, 5, 6, 7, 9, 11, 12, 13, 15, 17, 18 and 19.

ASSEMBLY A19

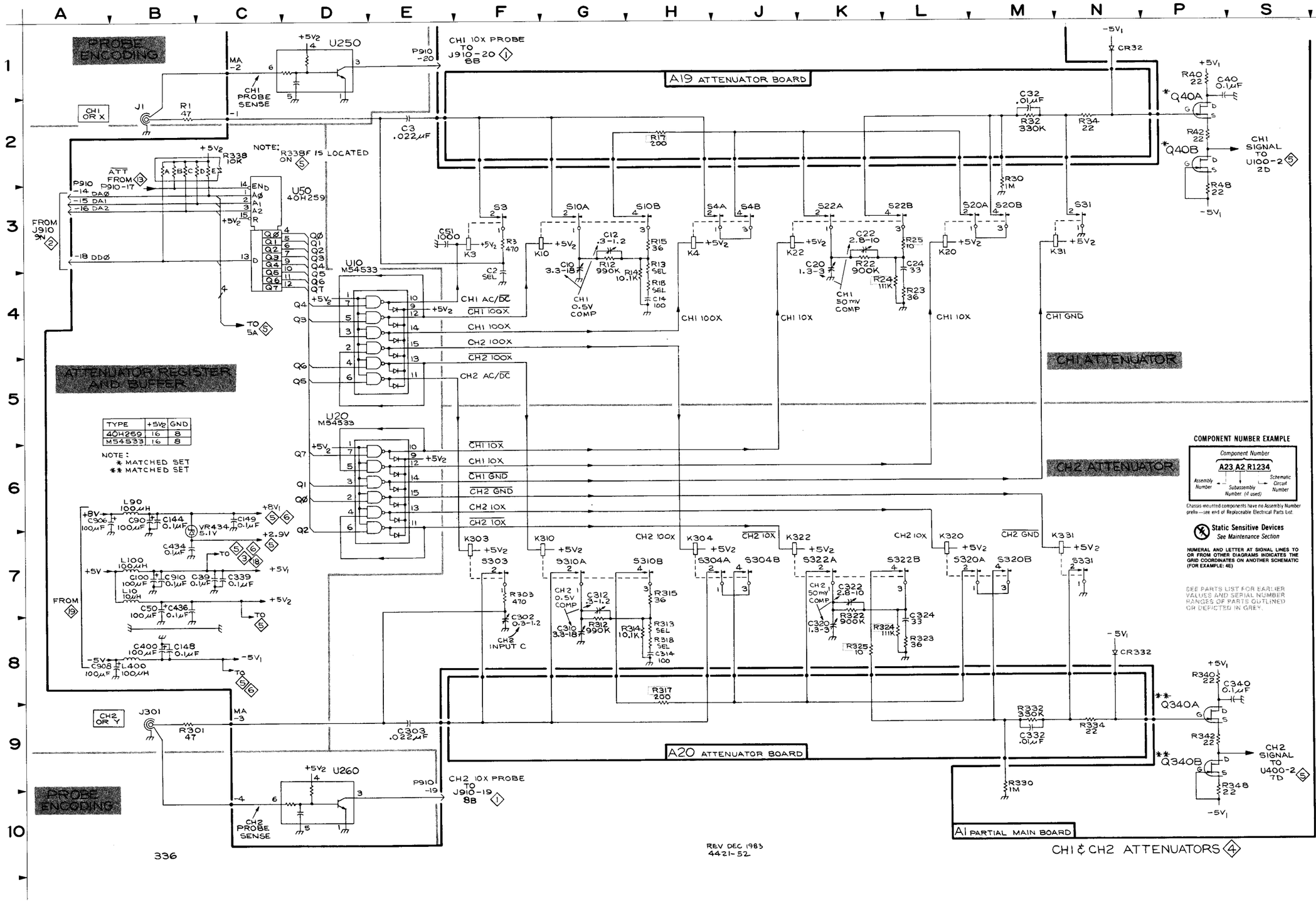
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C32	2M	4C	R17	2H	3C	R34	2N	5C			
			R32	2M	4C						

ASSEMBLY A20

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C332	9M	4E	R317	8H	3E	R334	9N	5E			
			R332	9M	4E						

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1	2B	CHASSIS	J301	9B	CHASSIS						



CH1 & CH2 ATTENUATORS ◇4

REV DEC 1983
4421-52

CH1 & CH2 ATTENUATORS ◇4

CH 1 & CH 2 VERTICAL PREAMPS 5

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C102	3F	6B	R133	4C	5B	R420	8F	5E	U100A	2F	5C
C133A	6B	5A	R140	4H	5C	R422	8F	5E	U100B	2F	5C
C133B	4B	5A	R144	2H	5C	R431	6B	5A	U100C	2G	5C
C133C	6L	5A	R148	2J	6C	R433	6C	5E	U100D	4F	5C
C133D	5L	5A	R150	5H	6D	R440	9H	5D	U100E	3F	5C
C170	5J	6C	R151	2J	5C	R444	7H	5E	U100F	3F	5C
C194	3M	6C	R152	5H	6C	R448	7H	6E	U133A	2G	5B
C195	3M	6C	R153	2J	6C	R451	8J	6E	U133B	3D	5B
C402	8F	5D	R156	4J	6C	R453	8J	6E	U160A	1K	6C
C494	8M	7D	R160A	1M	6C	R456	9H	6D	U160B	2L	6C
			R160B	1L	6C	R460A	6M	6D	U160C	2K	6C
MG1	6A	5A	R160C	2L	6C	R460B	6L	6D	U160D	2P	6C
MG2	3A	5A	R160D	3L	6C	R460C	7L	6D	U170A	4K	6B
MG3	5L	5A	R160E	3L	6C	R460D	8L	6D	U170B	4L	6B
MG4	5L	5A	R160F	4L	6C	R460E	9L	6D	U170C	3K	6B
P950	2C	4G	R160G	5M	6C	R460F	9L	6D	U170D	3P	6B
P960	2C	4G	R161	2M	6C	R460G	10M	6D	U174	5D	5F
P960	2S	4G	R164	2M	6C	R461	7M	6E	U220A	5M	5A
P960	7S	4G	R170	5F	5F	R464	7M	6E	U220B	5M	5A
			R171	5H	5F	R470	5G	5F	U400A	7F	5D
Q144	2H	6C	R172	5G	5F	R471	6H	6F	U400B	7F	5D
Q156	4H	6C	R174	4C	5F	R472	6G	6F	U400C	7F	5D
Q190	1M	6B	R190	1N	7C	R474	4C	6E	U400D	9F	5D
Q230	4M	6B	R196	2N	6C	R490	6N	6D	U400E	8F	5D
Q444	7H	6E	R200	3N	6C	R496	7N	6E	U400F	8F	5D
Q456	9H	6D	R202	3N	6C	R500	8N	6E	U430	4B	4E
Q490	6M	6D	R210	1N	7B	R502	8N	6E	U433A	7G	5E
Q530	9N	6D	R214	3N	6B	R510	6N	6D	U433B	8D	5E
			R215	1P	5F	R514	8N	6D	U460A	6K	6E
R100	2E	5C	R217	1P	5G	R520	6M	6C	U460B	7L	6E
R102	3F	6B	R218*	3N	6C	R530	10M	6D	U460C	8K	6E
R104	3F	5C	R220	5M	6B	R540	10M	6D	U460D	7P	6E
R105	3F	6B	R230	5N	6B	R970	3P	5G	U470A	9K	6D
R107*	3E	5C	R240	4N	6B	R971	2P	5G	U470B	9L	6D
R108	3F	6C	R338F	4B	3F	R972	3P	5G	U470C	8K	6D
R110	3E	5B	R400	8E	5D	R974	7P	5F	U470D	8P	6D
R118	3E	5B	R402	8F	5D	R975	9P	5F	U474	5D	6F
R120	3F	5C	R404	8F	5D	R976	8P	5F			
R122	3F	5C	R408*	8F	5D	RT109*	3F	5C			
R131	3C	5A	R410	8E	5D	RT219*	3N	6B			
			R418	8E	5D	RT409*	8F	5D			

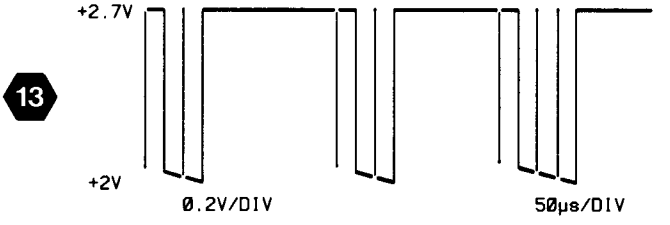
Partial A1 also shown on diagrams 1, 2, 3, 4, 6, 7, 9, 11, 12, 13, 15, 17, 18 and 19.

***See Parts List for serial number ranges.**

WAVEFORMS FOR DIAGRAM 6

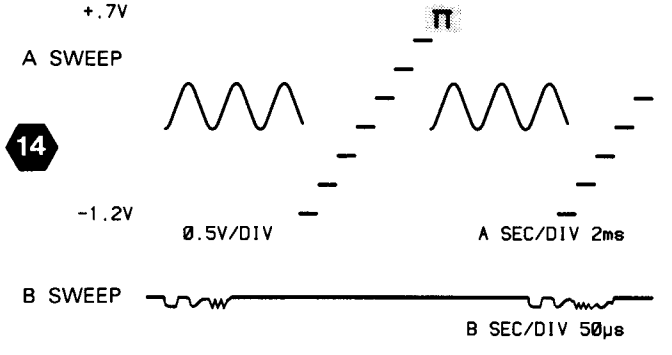
SEE TEST WAVEFORM SETUP ADJACENT TO DIAGRAM 1

TEST SCOPE AC COUPLED

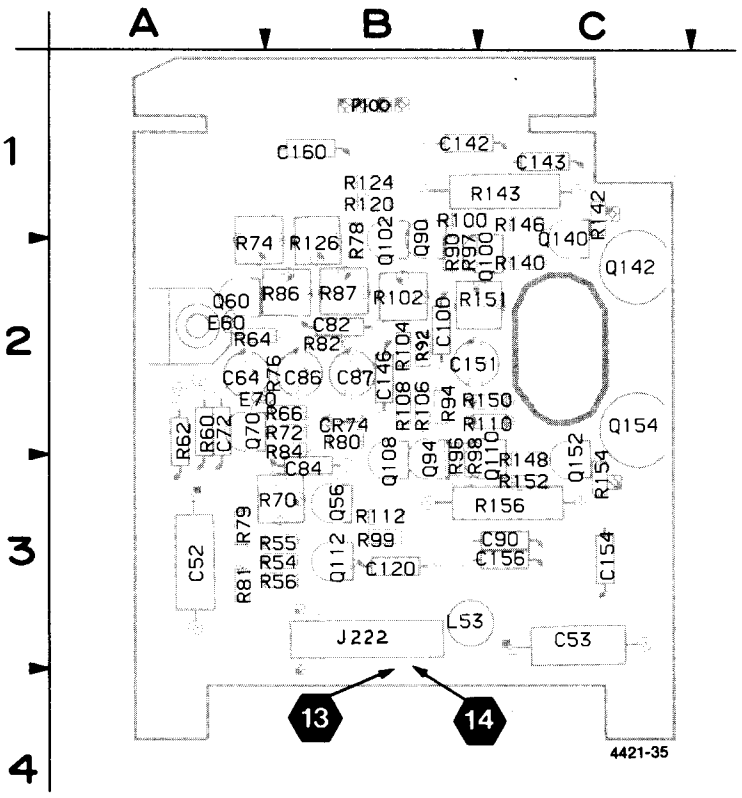


CHANGES TO 336 CONTROL SETTINGS:

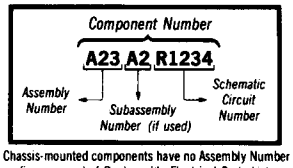
HORIZONTAL DISPLAY .....A
VERT MODE CH1
DISPLAY MODE .....STORE
2-DIV SINE-WAVE SIGNAL INPUT ON CH1
TEST SCOPE HORIZONTAL DISPLAY SET TO ALT



4421-69



COMPONENT NUMBER EXAMPLE



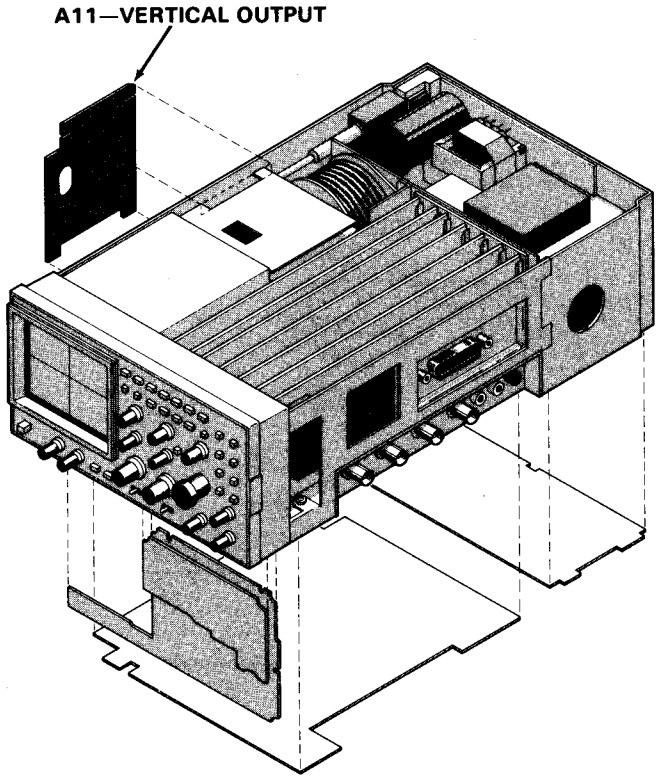
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

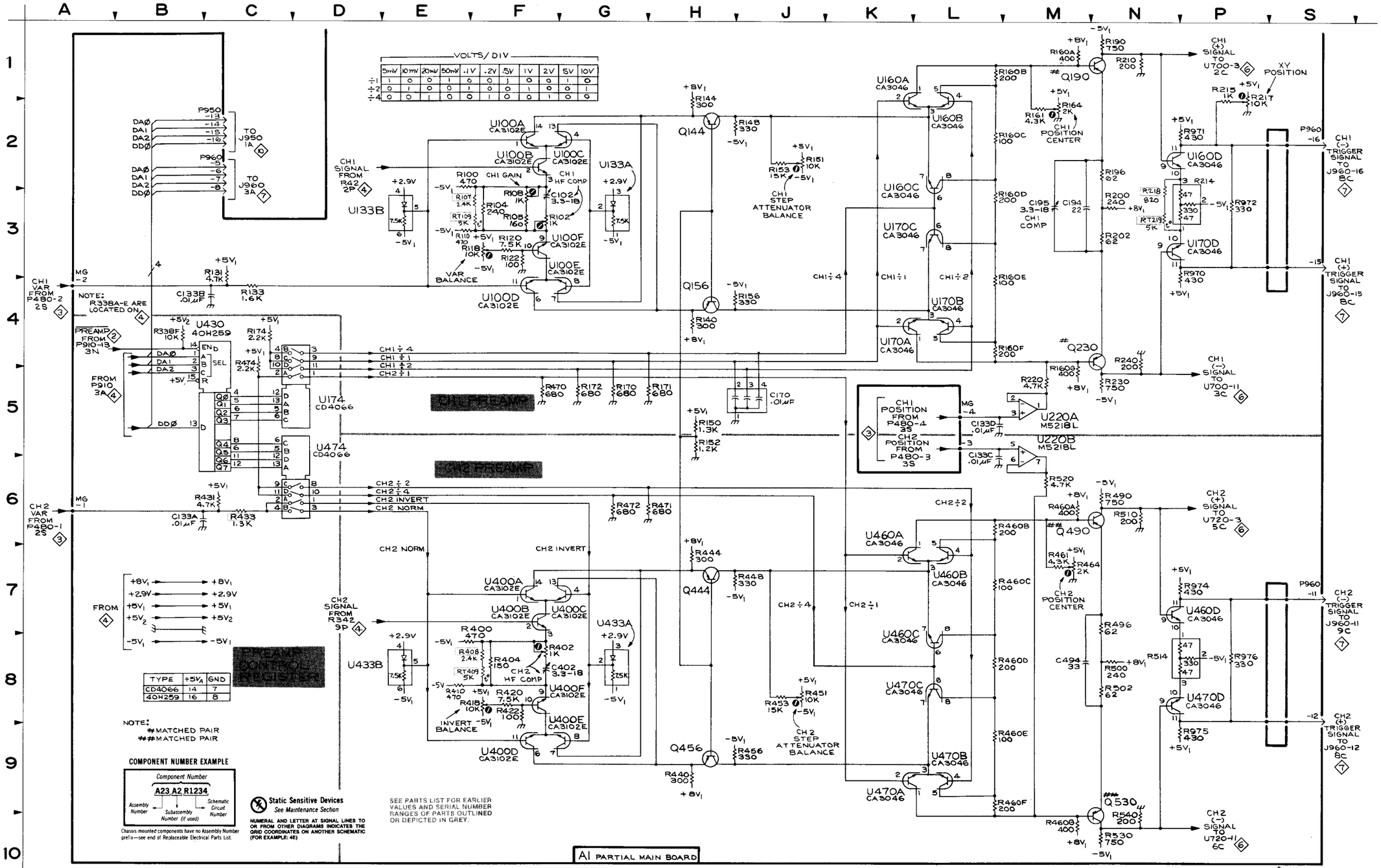
Static Sensitive Devices
See Maintenance Section

Figure 9-9. A11—Vertical Output board.

A11—VERTICAL OUTPUT BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C52	6	Q70	6	R86	6
C53	6	Q90	6	R87	6
C64	6	Q94	6	R90	6
C72	6	Q100	6	R92	6
C82	6	Q102	6	R94	6
C84	6	Q108	6	R96	6
C86	6	Q110	6	R97	6
C87	6	Q112	6	R98	6
C90	6	Q140	6	R99	6
C100	6	Q142	6	R100	6
C120	6	Q152	6	R102	6
C142	6	Q154	6	R104	6
C143	6	R54	6	R106	6
C146	6	R55	6	R108	6
C151	6	R56	6	R110	6
C154	6	R60	6	R112	6
C156	6	R62	6	R120	6
C160	18	R64	6	R124	6
CR74	6	R66	6	R126	6
E60	6	R70	6	R140	6
E70	6	R72	6	R142	6
J222	6	R74	6	R143	6
J222	6	R76	6	R146	6
J222	18	R78	6	R150	6
L53	6	R79	6	R151	6
P100	6	R80	6	R152	6
P100	18	R81	6	R154	6
Q56	6	R82	6	R156	6
Q60	6	R84	6		





4421-53

CH1 & CH2 PREAMPS ⑤ CH1 & CH2 VERTICAL PREAMPS

VERTICAL SWITCHING & OUTPUT AMPLIFIER 6

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C700	3C	7B	P962	8A	4A	R766	9E	7B	R847	3H	6F
C720	6C	7D				R768	1E	6B	R848	3J	5E
C734	6F	7B	Q800	7G	6E	R800	7F	7B			
C744	8C	6A	Q820	3G	7E	R801	10B	6E	U700A	1D	7C
C766	9E	7D	Q830	7G	6F	R802	7G	6E	U700B	2D	7C
C813	5G	7F	Q832	8H	6F	R808	7G	6F	U700C	3D	7C
C814	4G	7E	Q840	3G	7F	R812	5G	6F	U700D	3D	7C
C815	5F	7F	Q842	2H	6F	R813	5G	6F	U700E	3D	7C
C816	5G	7F				R814	5F	6F	U700F	1D	7C
C848	2J	5F	R711	2B	6G	R816	3G	7F	U720A	4C	7D
			R712	1B	6G	R820	3F	6B	U720B	5D	7D
CR818	6F	7E	R713	5B	6G	R822	4G	7E	U720C	6C	7D
CR819	4F	7E	R714	4B	6G	R824	7G	6F	U720D	6D	7D
CR834	5G	7F	R715	7B	6G	R826	3G	7F	U720E	6D	7D
CR836	5H	7F	R722	5C	7C	R830	7H	6F	U720F	4C	7D
			R734	7F	7B	R832	7H	6F	U740A	7C	6A
MD1	3H	7G	R736	4F	6B	R834	8H	6F	U740B	8D	6A
MD2	5H	7G	R740	8B	5A	R836	8H	6F	U740C	9C	6A
MD3	7H	6F	R741	9B	5A	R837	8H	6F	U740D	9D	6A
			R742	8B	5A	R840	4H	7F	U740E	9D	6A
P930	2J	3G	R744	8D	6A	R842	3H	7F	U740F	7D	6A
P940	10A	3G	R746	9C	5A	R844	2H	6F			
P940	1A	3G	R750	9B	5A	R846	3H	6F			

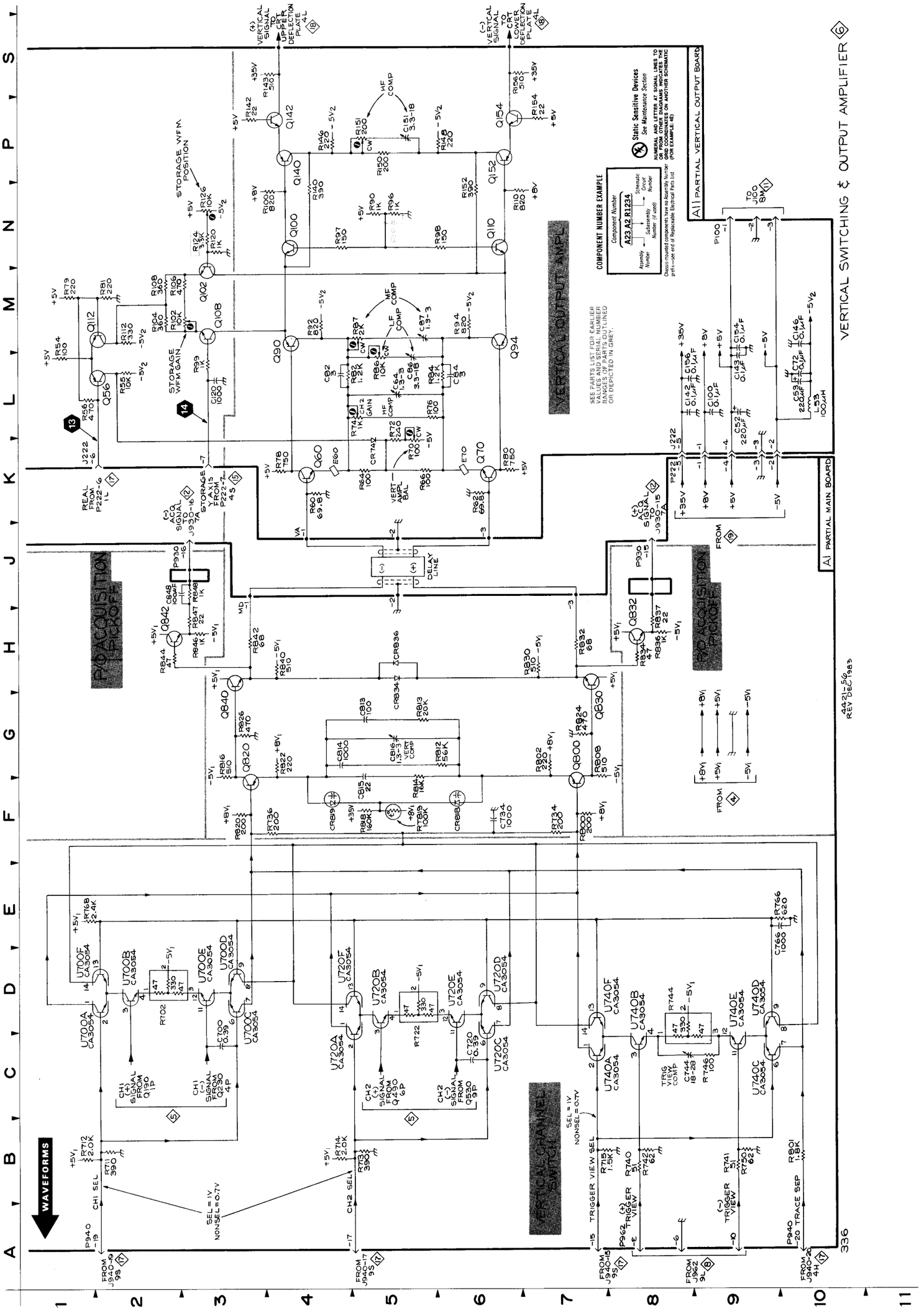
Partial A1 also shown on diagrams 1, 2, 3, 4, 5, 7, 9, 11, 12, 13, 15, 17, 18 and 19.

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C52	9L	3A	J222	1K	3B	R55	2L	3B	R98	6N	2C
C53	10L	3C	J222	8K	3B	R56	1L	3B	R99	3L	3B
C64	5L	2A				R60	4K	2A	R100	4N	1B
C72	10L	2A	L53	10L	3B	R62	6K	2A	R102	2M	2B
C82	4L	2B				R64	5K	2A	R104	2M	2B
C84	6L	3B	P100	9N	1B	R66	5K	2B	R106	2M	2B
C86	5L	2B				R70	5K	3B	R108	2M	2B
C87	5M	2B	Q56	2L	3B	R72	5L	2B	R110	6N	2C
C90*	5N	3C	Q60	4K	2A	R74	5L	2A	R112	2M	3B
C100	9L	2B	Q70	6K	2A	R76	5L	2B	R120	3N	1B
C120	3L	3B	Q90	4M	1B	R78	4K	1B	R124	3N	1B
C142	8L	1B	Q94	6M	2B	R79	1M	3A	R126	3N	1B
C143	9L	1C	Q100	4N	2C	R80	6K	2B	R140	4N	2C
C146	10M	2B	Q102	3M	1B	R81	2M	3A	R142	3P	1C
C151	5P	2B	Q108	3M	2B	R82	5L	2B	R143	4S	1C
C154	9M	3C	Q110	6N	2C	R84	5L	2B	R146	4P	1C
C156	8L	3C	Q112	1M	3B	R86	5L	2B	R150	5P	2C
			Q140	4P	1C	R87	5M	2B	R151	5P	2B
CR74	5K	2B	Q142	4P	2C	R90	5N	2B	R152	6N	3C
			Q152	6P	3C	R92	4M	2B	R154	7P	3C
E60	4K	2A	Q154	6P	2C	R94	6M	2B	R156	6S	3C
E70	6K	2A				R96	5N	2B			
			R54	1M	3B	R97	4N	2B			

Partial A11 also shown on diagram 18.

***See Parts List for serial number ranges.**


VERTICAL SWITCHING & OUTPUT AMPLIFIER 6
A1 PARTIAL VERTICAL OUTPUT BOARD
A1 PARTIAL MAIN BOARD
VERTICAL OUTPUT AMPL
P/O ACQUISITION PC BOARD
P/O ACQUISITION PC BOARD
VERTICAL CHANNEL SWITCH
WAVEFORMS
COMPONENT NUMBER EXAMPLE
Static Sensitive Devices
See Maintenance Section
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR REPORTED ON GREY.
4421-56 REV DEC 1983
336

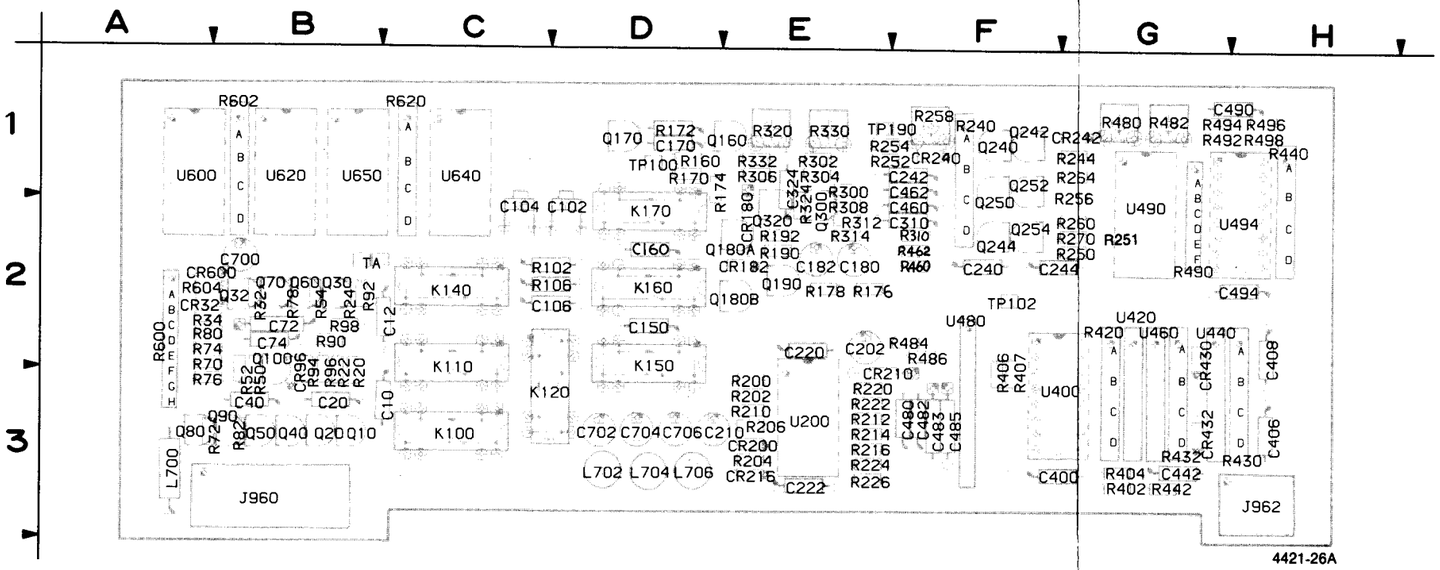
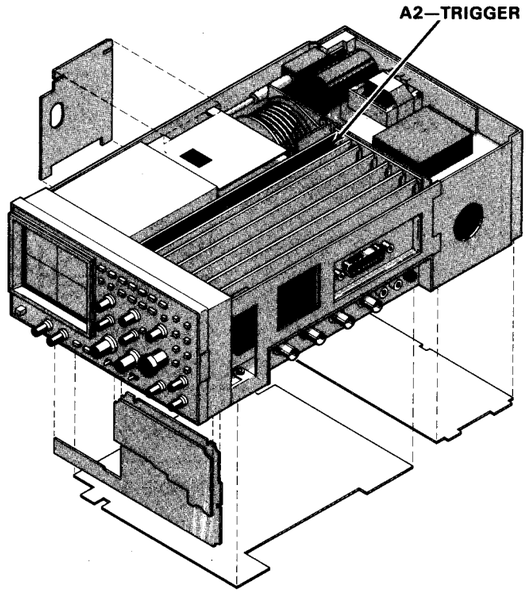


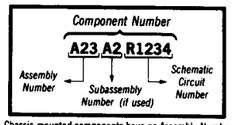
Figure 9-10. A2—Trigger board.



A2—TRIGGER BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C10	7	K100	7	R174	7	R440C	8
C20	7	K110	7	R176	7	R440D	8
C40	7	K120	7	R178	7	R442	8
C72	7	K140	7	R190	7	R460	8
C74	7	K150	7	R192	7	R462	8
C102	7	K160	7	R200	8	R480	8
C104	7	K170	7	R202	8	R482	8
C106	7	L700	7	R204	8	R484	8
C150	7	L702	7	R206	8	R486	8
C160	7	L704	7	R210	8	R490A	8
C170	7	L706	7	R212	8	R490B	8
C180	7	Q10	7	R214	8	R490C	8
		Q20	7	R216	8	R490D	8
C182	7	Q30	7	R220	8	R490E	8
C202	8	Q32	7	R222	8	R490F	8
C210	8	Q40	7	R224	8	R492	8
C220	7	Q50	7	R226	8	R494	8
C222	8	Q60	7	R240A	8	R496	8
C242	8	Q70	7	R240B	8	R498	8
C244	8	Q80	7	R240C	8	R600	7
C310	8	Q90	7	R240D	8	R602	7
C324	8	Q100	7	R244	8	R602	7
C400	7	Q160	7	R250	8	R602	7
C406	8	Q170	7	R251	8	R604	7
C408	8	Q180A	7	R252	8	R620	7
C442	8	Q180B	7	R254	8	R620	7
C460	8	Q190	7	R256	8	R620	7
C462	8	Q240	8	R258	8	R620	7
C480	8	Q242	8	R260	8	R620	7
C482	8	Q244	8	R264	8	TA	7
C483	8	Q250	8	R270	8	TP100	7
C485	8	Q252	8	R300	8	TP102	7
C490	7	Q254	8	R302	8	TP190	7
C494	7	Q300	8	R304	8	U200A	8
C700	7	Q320	8	R306	8	U200B	8
C702	7	R20	7	R308	8	U400A	8
C704	7	R22	7	R310	8	U400B	8
C706	7	R24	7	R312	8	U400C	8
CR32	7	R32	7	R314	8	U420A	8
CR96	7	R34	7	R320	8	U420B	8
CR182	7	R50	7	R324	8	U440A	8
CR200	8	R52	7	R330	8	U440B	8
CR210	8	R54	7	R332	8	U460A	8
CR216	8	R70	7	R402	8	U460B	8
CR240	8	R72	7	R404	8	U480	8
CR242	8	R74	7	R406	8	U490A	8
CR430	8	R76	7	R407	8	U490B	8
CR432	8	R78	7	R420A	8	U490C	8
CR600	7	R80	7	R420B	8	U490D	8
J960	7	R82	7	R420C	8	U494A	8
J960	7	R90	7	R420D	8	U494B	8
J960	7	R92	7	R430A	8	U494C	8
J960	7	R94	7	R430B	8	U494D	8
J960	7	R96	7	R430C	8	U600	7
J962	8	R98	7	R430D	8	U620	7
J962	8	R102	7	R432A	8	U640	7
J962	8	R106	7	R432B	8	U650A	7
J962	8	R160	7	R432C	8	U650B	7
J962	8	R170	7	R432D	8	U650C	8
		R172	7	R440A	8		
				R440B	8		

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

TRIGGER SELECT 

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C912	2B	2F	P56	9A	5G	R908	2A	2F	R919	2D	4G
C914	2B	2F	P960	2D	4G	R916	2B	2F			
C916	2B	2F	P960	7M	4G	R917	2C	2F			
			P960	9B	4G	R918	2C	2F			

Partial A1 also shown on diagrams 1, 2, 3, 4, 5, 6, 9, 11, 12, 13, 15, 17, 18 and 19.

ASSEMBLY A2

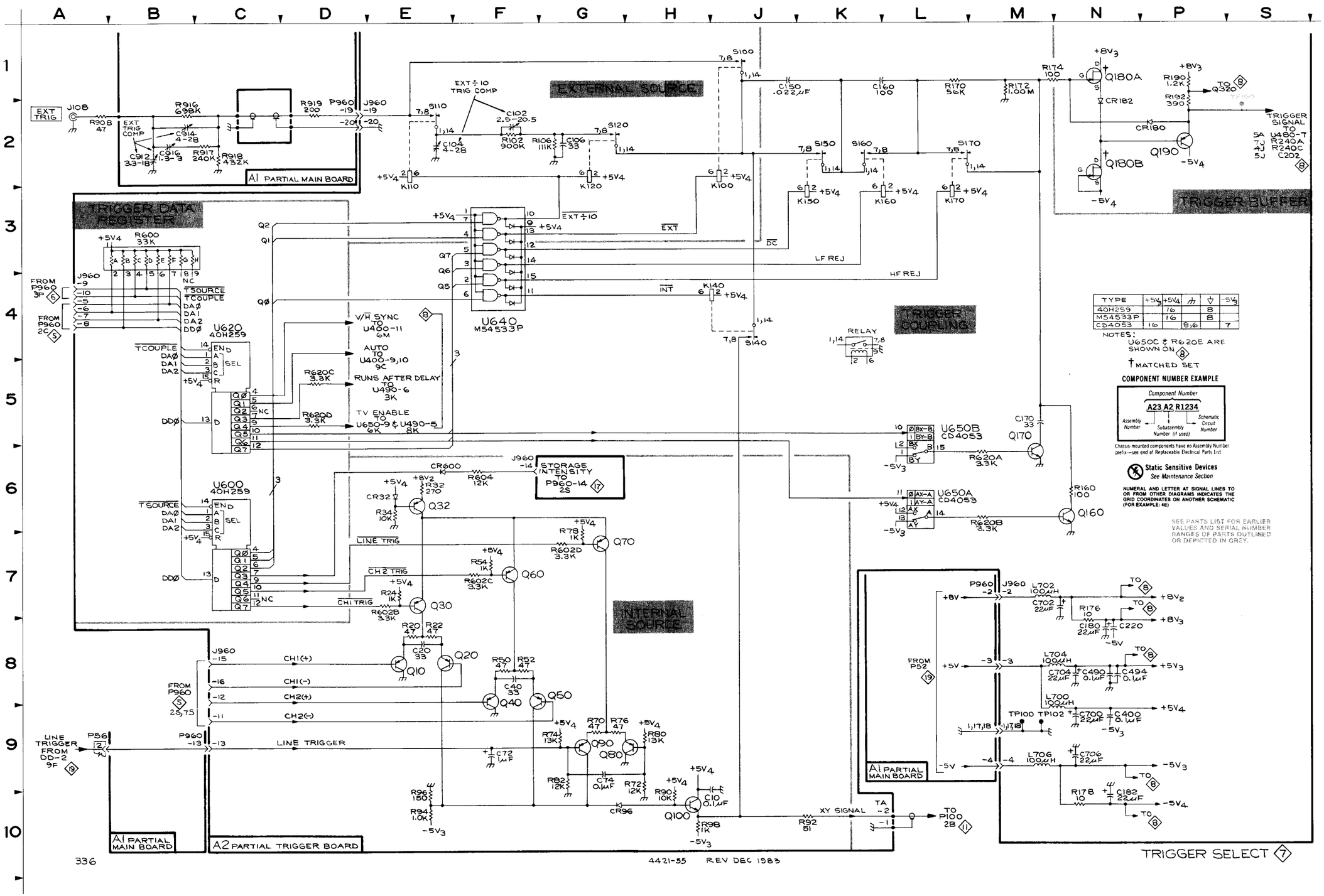
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C10	10H	3C	J960	4A	3B	Q160	6N	1E	R170	1L	1D
C20	8E	3B	J960	6F	3B	Q170	5M	1D	R172	1M	1D
C40	8F	3B	J960	7M	3B	Q180A	1N	2E	R174	1N	2E
C72	9F	2D	J960	8C	3B	Q180B	2N	2E	R176	7N	2E
C74	9G	2B				Q190	2P	2E	R178	10N	2E
C102	2F	2D	K100	2J	3C				R190	1P	2E
C104	2F	2C	K110	2E	2C	R20	8E	3B	R192	2P	2E
C106	2G	2D	K120	2G	3D	R22	8E	3B	R600	3B	2A
C150	1J	2D	K140	4J	2C	R24	7E	2B	R602B	7E	1B
C160	1K	2D	K150	3K	2D	R32	6E	2B	R602C	7F	1B
C170	5M	1D	K160	3L	2D	R34	6E	2A	R602D	7G	1B
			K170	3L	2D	R50	8F	3B	R604	6F	2A
C180	8N	2E				R52	8F	3B	R620A	6M	1C
C182	10N	2E	L700	9N	3A	R54	7F	2B	R620B	6M	1C
C220	8N	2E	L702	7M	3D	R70	9G	2A	R620C	5D	1C
C400	9N	3G	L704	8N	3D	R72	9H	3B	R620D	5D	1C
C490	8N	1G	L706	9M	3D	R74	9G	2A			
C494	8N	2H				R76	9G	3A	TA	10L	2C
C700	9N	2B	Q10	8E	3B	R78	7G	2B			
C702	7M	3D	Q20	8F	3B	R80	9H	2A	TP100	9M	1D
C704	8N	3D	Q30	7E	2B	R82	9G	3B	TP102	9M	2F
C706	9N	3D	Q32	6E	2B	R90	10H	2B	TP190*	2S	1E
			Q40	9F	3B	R92	10K	2B			
CR32	6E	2A	Q50	8G	3B	R94	10E	3B	U600	6C	1A
CR96	10G	3B	Q60	7F	2B	R96	10E	3B	U620	4C	1B
CR180	2P	2E	Q70	7G	2B	R98	10H	2B	U640	4F	1C
CR182	2N	2E	Q80	9G	3A	R102	2F	2D	U650A	6L	1B
CR600	6E	2A	Q90	9G	3B	R106	2G	2D	U650B	5L	1B
J960	2E	3B	Q100	10H	2B	R160	6N	1D			

Partial A2 also shown on diagram 8.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J108	2A	CHASSIS									

***See Parts List for serial number ranges.**



4421-55 REV DEC 1983

TRIGGER SELECT 7

A & B SWEEP TRIGGERS & TV SYNC SEPARATOR

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C202	5J	2E	Q250	3H	1F	R308	9G	2E	R490A	8L	2G
C210	5K	3E	Q252	3H	1F	R310	8F	2F	R490B	3L	2G
C222	5L	3E	Q254	4H	2F	R312	9J	2E	R490C	8P	2G
C242*	6G	1F	Q300	9J	2E	R314	10J	2E	R490D	3P	2G
C244	5H	2F	Q320	10J	2E	R320	9H	1E	R490E	8P	2G
C310	9G	2F				R324	9H	1E	R490F	3P	2G
C324	9H	1E	R200	5L	3E	R330	9J	1E	R492	7P	1G
C406	7E	3H	R202	5J	3E	R332	9H	1E	R494	7N	1G
C408	3E	2H	R204	5K	3E	R402	2D	3G	R496	3N	1H
C442	7G	3G	R206	5K	3E	R404	8D	3G	R498	3P	1H
C460	4G	2F	R210	5K	3E	R406	2C	3F	R620E	6J	1C
C462	7G	1F	R212	4K	3E	R407	8B	3F			
C480	1B	3F	R214	5L	3E	R420A	2C	2G	U200A	5K	3E
C482	9B	3F	R216	5L	3E	R420B	8B	2G	U200B	5L	3E
C483	1B	3F	R220	5L	3E	R420C	3E	2G	U400A	5M	3G
C485	9B	3F	R222	5L	3E	R420D	8E	2G	U400B	2C	3G
			R224	5L	3E	R430A	3F	3H	U400C	8B	3G
CR200	6K	3E	R226	5L	3E	R430B	3E	3H	U420A	2D	2G
CR210	5L	3E	R240A	7J	1F	R430C	7F	3H	U420B	8D	2G
CR216	6K	3E	R240B	7H	1F	R430D	7E	3H	U440A	4F	2G
CR240	6H	1F	R240C	4J	1F	R432A	4G	3G	U440B	7F	2G
CR242	3J	1G	R240D	4H	1F	R432B	4F	3G	U460A	3G	2G
CR430	3F	2G	R244	7H	1G	R432C	8F	3G	U460B	7G	2G
CR432	7F	3G	R250	5H	2G	R432D	7G	3G	U480	3B	2F
			R251*	5H	2G	R440A	6F	1H	U490A	7K	2G
J962	3D	3H	R252	6H	1E	R440B	7F	1H	U490B	3K	2G
J962	3E	3H	R254	6G	1E	R440C	3F	1H	U490C	4M	2G
J962	3S	3H	R256	4H	1G	R440D	3F	1H	U490D	5N	2G
J962	7S	3H	R258	6H	1F	R442	7G	3G	U494A	7P	2H
J962	8D	3H	R260	5H	2G	R460	4G	2F	U494B	8P	2H
J962	9L	3H	R264	3H	1G	R462	7G	2F	U494C	3P	2H
			R270	5H	2G	R480	7N	1G	U494D	3P	2H
Q240	7H	1F	R300	9H	1E	R482	3N	1G	U650C	6K	1B
Q242	7H	1F	R302	9J	1E	R484	1B	2F			
Q244	6H	2F	R304	9J	1E	R486	9B	2F			
			R306	9J	1E						

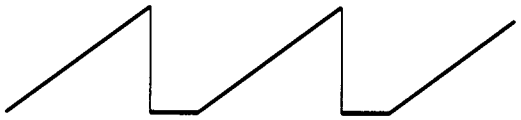
Partial A2 also shown on diagram 7.

***See Parts List for serial number ranges.**

SEE TEST WAVEFORM SETUP ADJACENT TO DIAGRAM 1

WAVEFORMS FOR DIAGRAM 9

A SWP



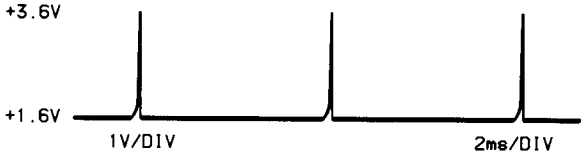
B SWP

15

23

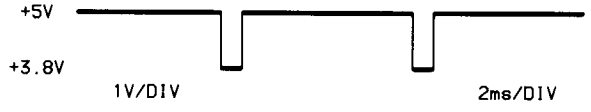
16

24

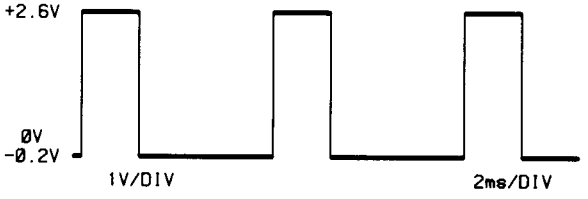


SET 336 AC-GND-DC TO GND

17



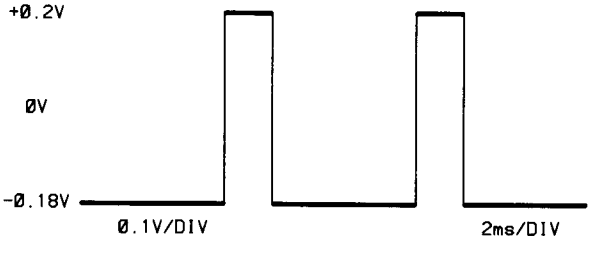
25



4421-70

18

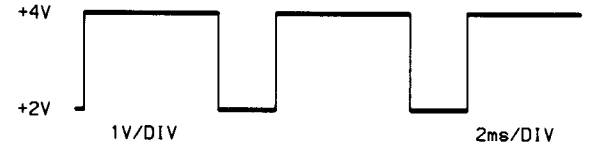
19



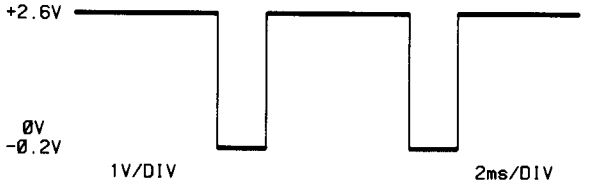
USE OF THE EXTENDER CIRCUIT BOARDS AND CABLES SUPPLIED IN THE SERVICE MAINTENANCE KIT PROVIDES EASE OF ACCESS TO THE WAVEFORM TEST POINTS.

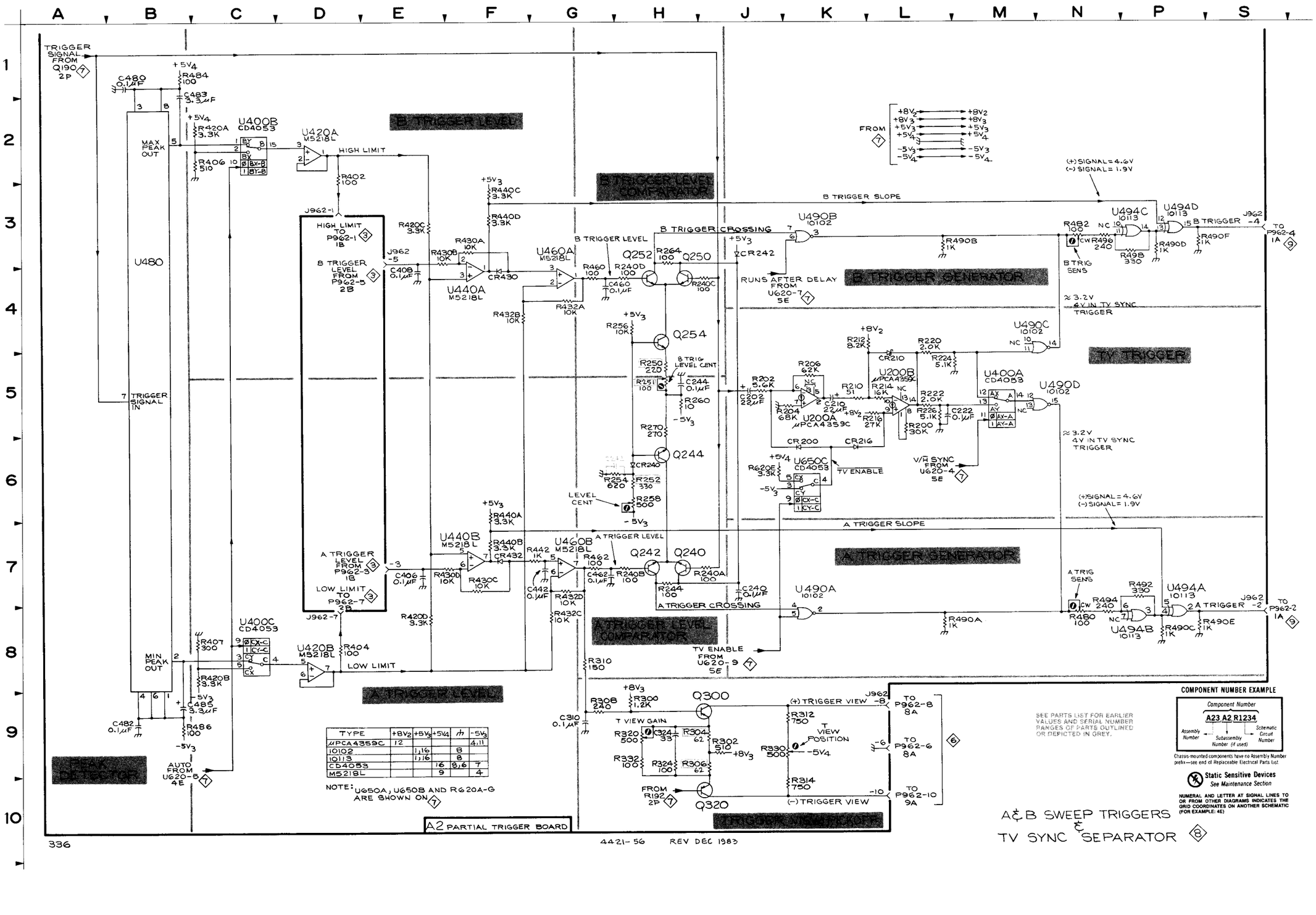
20

21



22





4421-56 REV DEC 1983

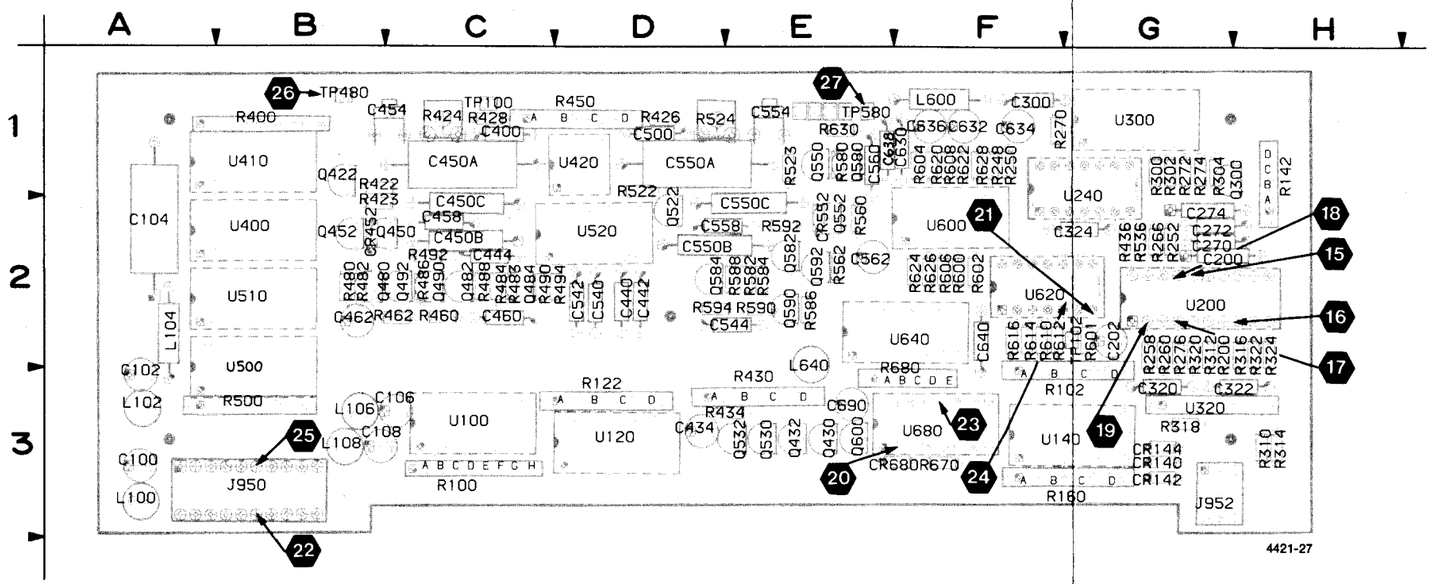
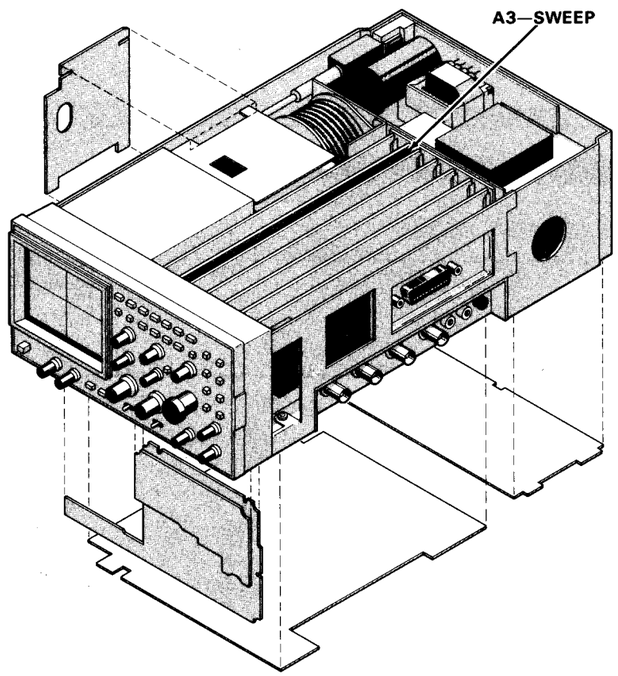


Figure 9-11. A3—Sweep board.

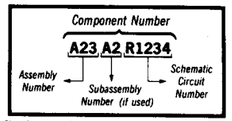


A3—SWEEP BOARD & WAVEFORMS FIG. 9-11

A3—SWEEP BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C100	9	L104	9	R270	9	R606	9
C102	9	L106	9	R272	9	R608	9
C104	9	L108	9	R276	9	R610	9
C106	9	L600	9	R300	9	R612	9
C108	9	L640	9	R302	9	R614	9
C200	9	Q300	9	R304	9	R616	9
C202	9	Q422	10	R310	9	R620	9
C270	9	Q430	9	R312	9	R624	9
C270	9	Q432	9	R314	10	R626	9
C272	9	Q450	10	R316	10	R628	9
C274	9	Q452	10	R318	10	R630	9
C300	9	Q480	10	R320	9	R670	9
C320	9	Q482	10	R322	10	R680A	9
C322	10	Q484	10	R324	10	R680B	9
C324	9	Q490	10	R400	10	R680C	9
C400	10	Q492	10	R422	10	R680D	9
C434	9	Q522	10	R423	10	R680E	9
C440	10	Q530	9	R424	10	TP100	9
C442	10	Q532	9	R426	10	TP102	9
C444	10	Q550	10	R428	10	TP480	10
C450A	10	Q552	10	R430	9	TP580	10
C450B	10	Q580	10	R430	9	U100	10
C450C	10	Q582	10	R434	9	U120	10
C454	10	Q584	10	R436	9	U140	10
C458	10	Q590	10	R450A	10	U200	9
C460	9	Q592	10	R450B	10	U240A	9
C462	9	Q600	9	R450C	10	U240B	9
C500	10	R100A	9	R450D	10	U240C	9
C540	10	R100B	10	R460	9	U240D	9
C542	10	R100C	10	R462	9	U300A	9
C544	10	R100D	10	R480	10	U300C	9
C550A	10	R100E	10	R482	10	U300	10
C550B	10	R100F	10	R483	10	U320	9
C550C	10	R100G	10	R484	10	U320	10
C554	10	R100H	10	R486	10	U400	10
C558	10	R102A	10	R488	10	U410	10
C560	9	R102B	10	R490	10	U420A	10
C562	9	R102C	10	R492	10	U420B	10
C630	9	R102D	10	R494	10	U500	10
C632	9	R122A	10	R500	10	U510	10
C636	9	R122B	10	R522	10	U520A	10
C638	9	R122C	10	R523	10	U520B	10
C640	9	R122D	10	R524	10	U520C	10
C690	9	R142A	9	R536	9	U520D	10
CR140	10	R142B	10	R560	9	U520E	10
CR142	10	R142C	10	R562	9	U600A	9
CR144	10	R142D	10	R580	10	U600B	9
CR452	10	R160A	10	R582	10	U600C	9
CR552	10	R160B	10	R584	10	U600D	9
CR680	9	R160C	10	R586	10	U600E	9
J950	9	R160D	10	R588	10	U620A	9
J950	10	R200	9	R590	10	U620B	9
J950	10	R248	9	R592	10	U620C	9
J950	10	R250	9	R594	10	U620D	9
J952	9	R252	9	R600	9	U620E	9
J952	9	R258	9	R601	9	U640	9
L100	9	R260	9	R602	9	U680	9
L102	9	R266	9	R604	9		

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

SWEEP CONTROL 9

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
MF	4A	4A	P910	2S	2G	P950	6A	4G	P962	1A	4A
			P950	2S	4G	P952	1A	4A			

Partial A1 also shown on diagrams 1, 2, 3, 4, 5, 6, 7, 11, 12, 13, 15, 17, 18 and 19.

ASSEMBLY A3

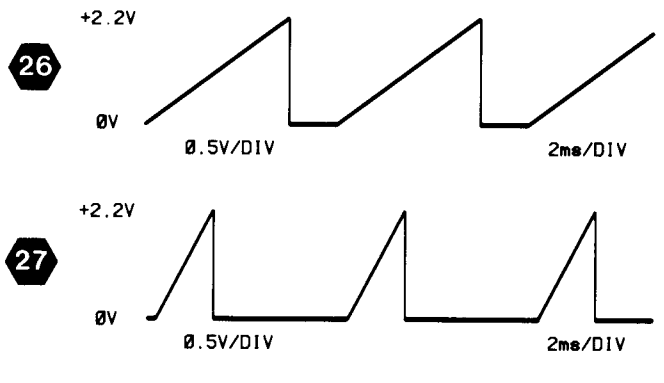
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	8B	3A	J952	1B	3G	R302	3F	1G	R680A	7N	2F
C102	6B	3A				R304	4E	1G	R680B	9M	2F
C104	8B	2A	L100	8B	3A	R310	4C	3H	R680C	6M	2F
C106	7B	3C	L102	6B	3A	R312	5C	2G	R680D	9K	2F
C108	8B	3B	L104	8B	2A	R320	4C	2G	R680E	8H	2F
C200	6H	2G	L106	7B	3B	R430A	9N	3E			
C202	2J	2G	L108	8B	3B	R430B	9N	3E	TP100	8B	1C
C270	5G	2G	L600	10G	1F	R434	6C	3D	TP102	8B	2G
C270	5G	2G	L640	8B	2E	R436	7N	2G			
C272	5F	2G				R460	7C	2C	U200	4J	2G
C274	5G	2G	Q300	4F	1G	R462	9C	2B	U240A	5G	1G
C300	6B	1F	Q430	6N	3E	R536	7N	2G	U240B	5F	1G
C320	5C	3G	Q432	6N	3E	R560	7C	2E	U240C	4M	1G
C324	6C	2G	Q530	9N	3E	R562	9C	2E	U240D	6K	1G
C434	6C	3D	Q532	9N	3E	R600	9E	2F	U300A	3F	1G
C460	7C	2C	Q600	4L	3E	R601	8G	2G	U300C	4E	1G
C462	9C	2B				R602	9E	2F	U320A	4C	3G
C560	7C	1E	R100G	2M	3C	R604	9G	1F	U600A	8F	2F
C562	9C	2E	R142A	4E	1H	R606	8G	2F	U600B	8G	2F
C630	8F	1F	R200	5H	2G	R608	8G	1F	U600C	6F	2F
C632	10G	1F	R248	6G	1F	R610	9J	2F	U600D	6G	2F
C636	7C	1F	R250	6G	1F	R612	9J	2F	U600E	9G	2F
C638	9E	1E	R252	6G	2G	R614	9H	2F	U620A	9H	2F
C640	8B	2F	R258	7M	2G	R616	9J	2F	U620B	9J	2F
C690	8C	3E	R260	7M	2G	R620	9E	1F	U620C	8H	2F
			R266	6K	2G	R624	8F	2F	U620D	7N	2F
CR680	5M	3E	R270	6K	1F	R626	8G	2F	U620E	9E	2F
			R272	6K	1G	R628	9C	1F	U640	8K	2F
J950	2S	3B	R276	4M	2G	R630	8F	1E	U680	5L	3F
J952	10B	3G	R300	3F	1G	R670	5M	3F			

Partial A3 also shown on diagram 10.

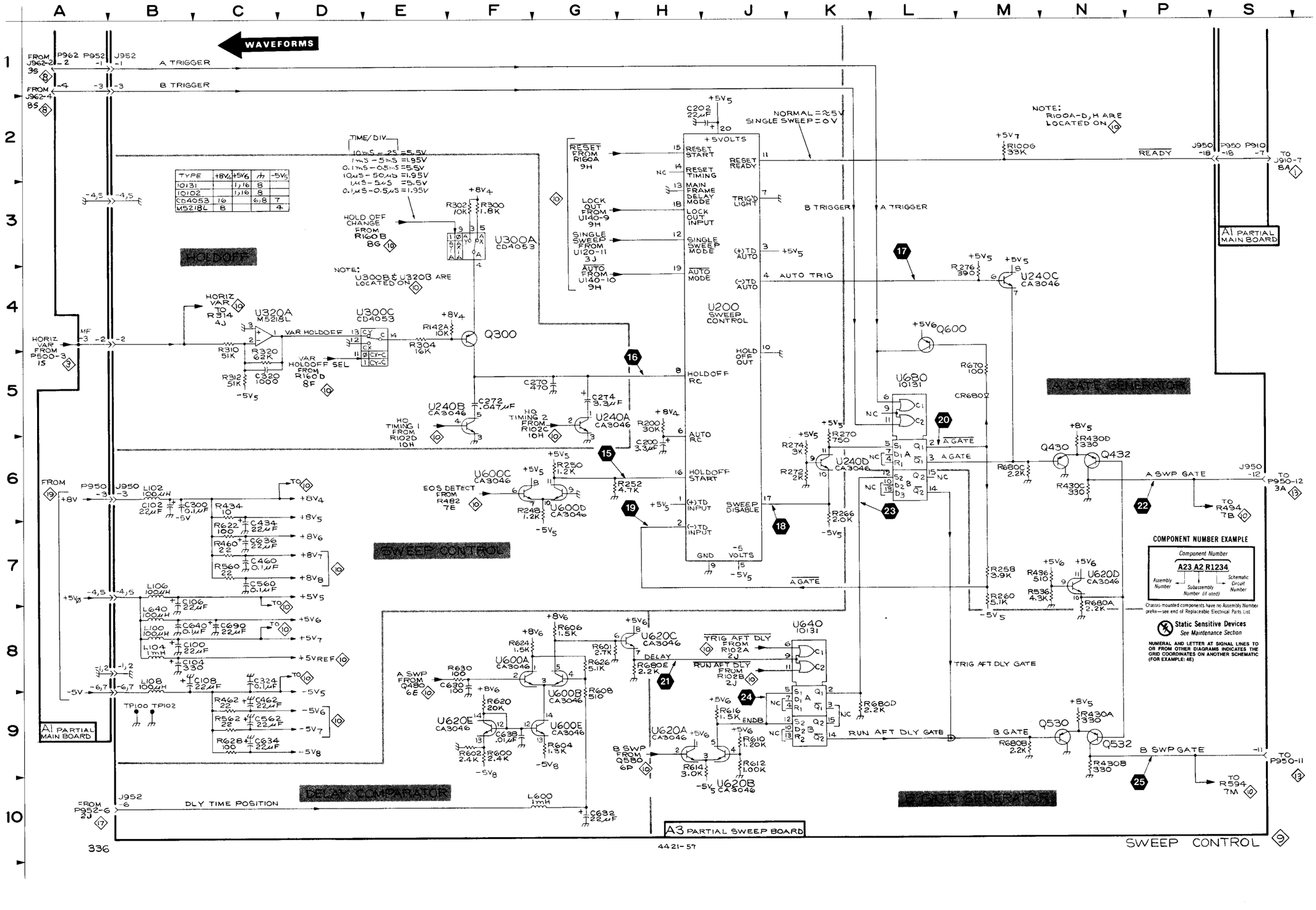
USE OF THE EXTENDER CIRCUIT BOARDS AND CABLES SUPPLIED IN THE SERVICE MAINTENANCE KIT PROVIDES EASE OF ACCESS TO THE WAVEFORM TEST POINTS.

WAVEFORMS FOR DIAGRAM 10

SEE TEST WAVEFORM SETUP ADJACENT TO DIAGRAM 1



4421-46


WAVEFORMS
A TRIGGER
B TRIGGER
HOLDOFF
SWEEP CONTROL
DELAY COMPARATOR
TRIGGER GENERATOR
A1 PARTIAL MAIN BOARD
A3 PARTIAL SWEEP BOARD
U200 SWEEP CONTROL
U300A CD4053
U300C CD4053
U320A M5218L
U240B CA3046
U240A CA3046
U600C CA3046
U600D CA3046
U600A CA3046
U600B CA3046
U620C CA3046
U620E CA3046
U620A CA3046
U620B CA3046
U240C CA3046
U240D CA3046
U620D CA3046
U640 10131
U680 10131
Q300
Q600
Q430
Q432
Q530
Q532
NORMAL = ≈5V
SINGLE SWEEP = 0V
TIME/DIV
HOLD OFF CHANGE FROM R160B 8G
HORIZ VAR FROM P500-3 1S
VAR HOLDOFF
VAR HOLDOFF SEL FROM R160D 8F
HO TIMING 1 FROM R102D 10H
HO TIMING 2 FROM R102C 10H
EOS DETECT FROM R482 7E
A SWP FROM Q480 6E
B SWP FROM Q580 6P
TRIG AFT DLY FROM R102A 2J
RUN AFT DLY FROM R102B 2J
DLY TIME POSITION
FROM P952-6 2J
READY
A GATE
B GATE
TRIG AFT DLY GATE
RUN AFT DLY GATE
A SWP GATE
B SWP GATE
AUTO TRIG
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)
NOTE: R100A-D, H ARE LOCATED ON 1G
NOTE: U300B & U320B ARE LOCATED ON 10
TO J910-7 8A
TO P950-12 3A
TO P950-11 3A
TO R494 7B
TO R594 7M
SWEEP CONTROL 9
4421-57
336

A & B SWEEP GENERATORS

ASSEMBLY A3

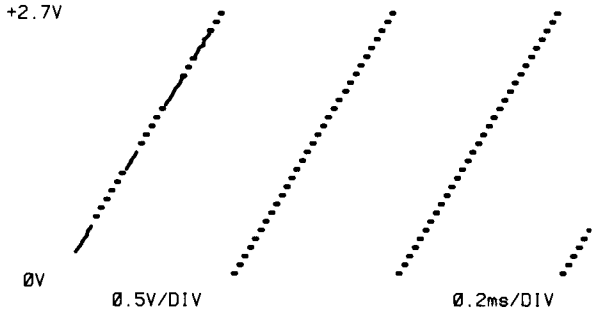
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C322	4J	3G	Q452	7D	2B	R142D	8G	1H	R524	6J	1D
C400	6G	1C	Q480	6E	2B	R160A	9G	3F	R580	8P	1E
C440	6B	2D	Q482	7C	2C	R160B	8F	3F	R582	9P	2E
C442	7B	2D	Q484	7C	2C	R160C	8G	3F	R584	9P	2E
C444	7D	2C	Q490	7E	2C	R160D	9G	3F	R586	9S	2E
C450A	7C	2C	Q492	7E	2C	R314	4J	3H	R588	9N	2E
C450B	6C	2C	Q522	5N	2D	R316	4J	2H	R590	9M	2E
C450C	5G	2C	Q550	7P	1E	R318	4J	3G	R592	8N	2E
C454	7C	1B	Q552	8P	2D	R322	4J	2H	R594	9M	2D
C458	6C	2C	Q580	7P	1E	R324	4J	2H			
C500	6L	1D	Q582	9N	2E	R400	4E	1B	TP480	6E	1B
C540	8K	2D	Q584	9N	2D	R422	5E	1B	TP580	7S	1E
C542	7K	2D	Q590	9P	2E	R423	6D	2B			
C544	9P	2E	Q592	9S	2E	R424	6J	1C	U100	2B	3C
C550A	7N	1D				R426	6J	1D	U120	1G	3D
C550B	8N	1D	R100A	1D	3C	R428	5J	1C	U140	8F	3F
C550C	5L	1D	R100B	1C	3C	R450A	5G	1D	U300B	5H	1G
C554	8N	1E	R100C	1C	3C	R450B	6G	1D	U320B	4J	3G
C558	7N	2D	R100D	2B	3C	R450C	5L	1D	U400	4D	2B
			R100E	1B	3C	R450D	6K	1D	U410	4G	1B
CR140	10G	3G	R100F	8E	3C	R480	7E	2B	U420A	6F	1D
CR142	10F	3G	R100H	1D	3C	R482	7E	2B	U420B	6L	1D
CR144	10F	3G	R102A	2H	3F	R483	7D	2C	U500	3K	3B
CR452	7D	2B	R102B	2H	3F	R484	7D	2C	U510	3N	2B
CR552	8P	2E	R102C	10G	3F	R486	7E	2C	U520A	6C	2D
			R102D	10G	3F	R488	8C	2C	U520B	7C	2D
J950	1A	3B	R122A	7K	3D	R490	7C	2C	U520C	8M	2D
J950	6S	3B	R122B	8K	3D	R492	7C	2C	U520D	7M	2D
J950	7S	3B	R122C	6B	3D	R494	7C	2C	U520E	7M	2D
			R122D	7B	3D	R500	4M	3B			
Q422	5C	1B	R142B	8F	1H	R522	6M	1D			
Q450	6D	2C	R142C	8G	1H	R523	7N	1E			

Partial A3 also shown on diagram 9.

SEE TEST WAVEFORM SETUP ADJACENT TO DIAGRAM 1

WAVEFORMS FOR DIAGRAM 11

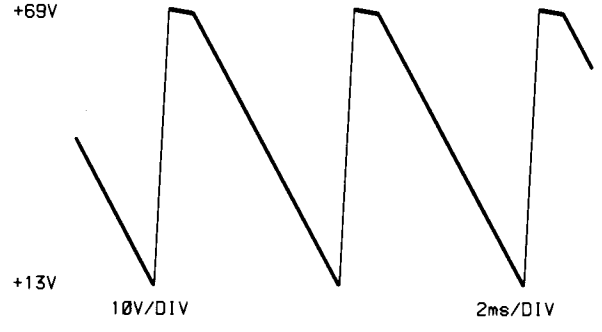
28



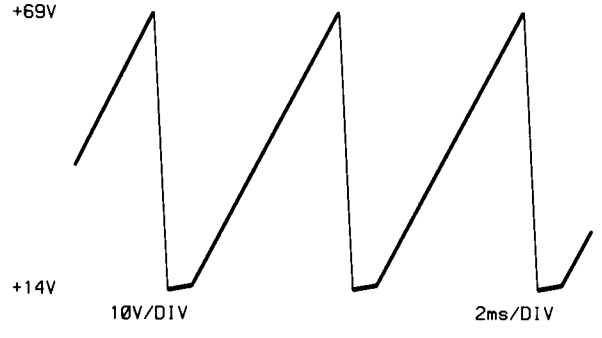
WAVEFORMS 29 & 30 HAVE THE FOLLOWING 336 CONTROL SETTINGS:

HORIZONTAL DISPLAY
MODE.....A
READOUT .....OFF (menu selection)

29

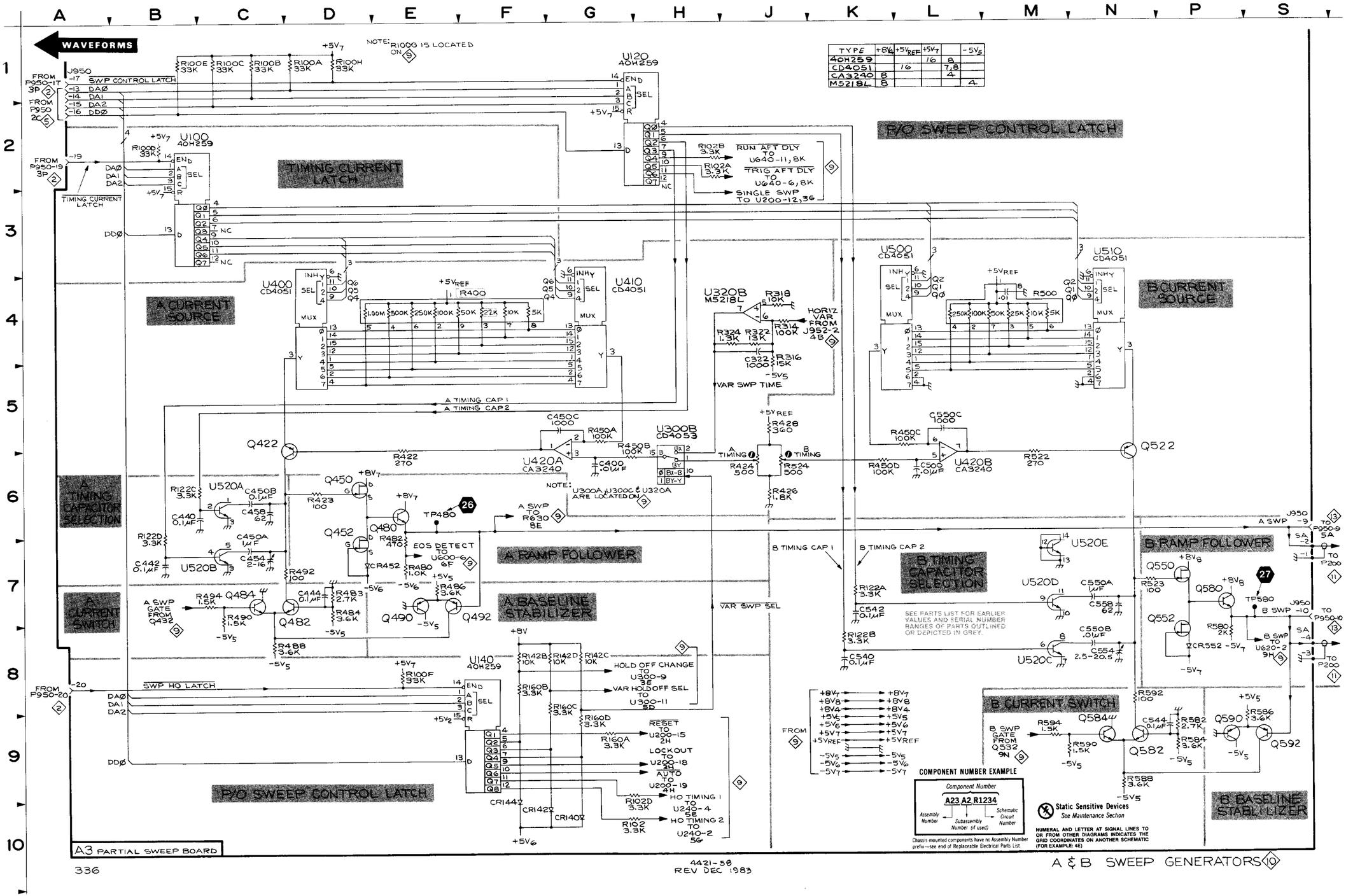


30



4421-71

USE OF THE EXTENDER CIRCUIT BOARDS AND CABLES SUPPLIED IN THE SERVICE MAINTENANCE KIT PROVIDES EASE OF ACCESS TO THE WAVEFORM TEST POINTS.



TYPE	+8V	+5V REF	+5V		-5V
40H259		16	16	8	
CD4051				7,8	
CA3240	8			4	
M5218L	8				4

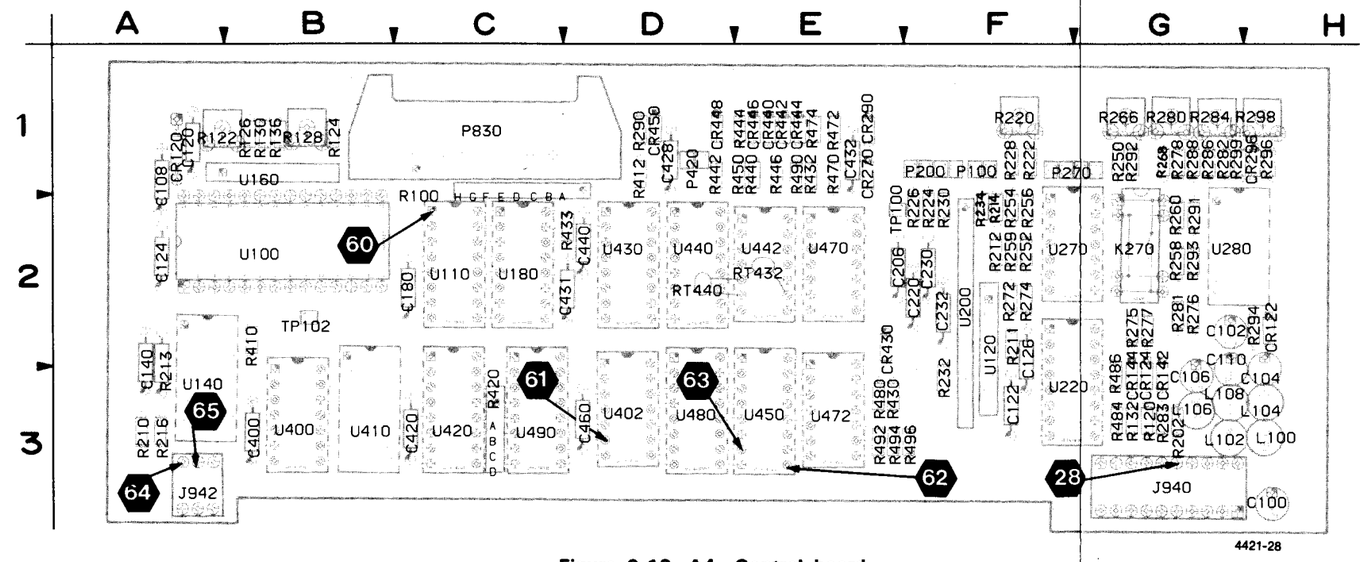


Figure 9-12. A4—Control board.

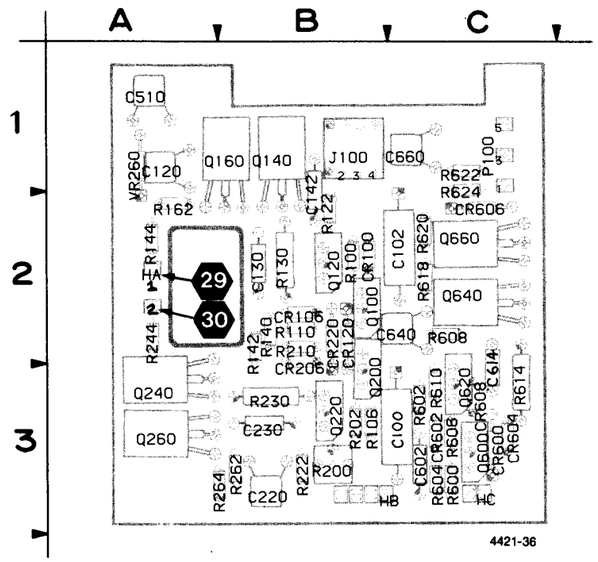


Figure 9-13. A12—Horizontal Output board.

A12—HORIZONTAL OUTPUT BOARD

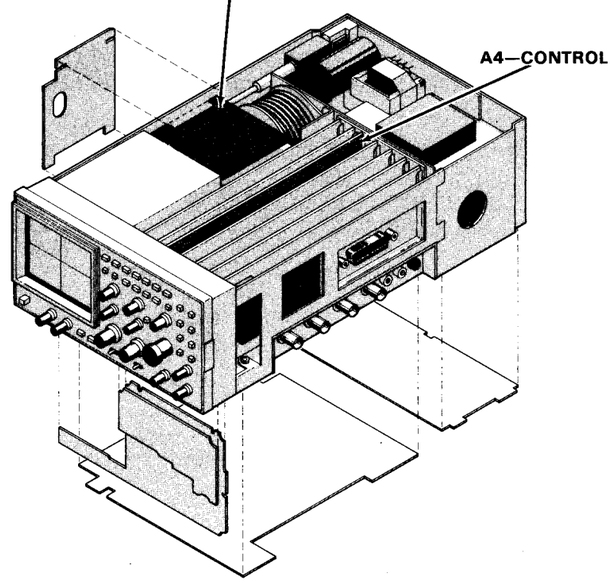
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C100	11	Q260	11
C102	11	Q600	18
C120	11	Q620	18
C130	11	Q640	18
C220	11	Q660	18
C230	11	R100	11
C510	18	R106	11
C602	18	R110	11
C614	18	R122	11
C640	18	R130	11
C660	18	R140	11
CR100	11	R142	11
CR106	11	R144	11
CR120	11	R162	11
CR206	11	R200	11
CR220	11	R202	11
CR600	18	R210	11
CR602	18	R222	11
CR604	18	R230	11
CR606	18	R244	11
CR608	18	R262	11
HA	11	R264	11
HA	11	R600	18
HB	11	R602	18
HC	18	R604	18
J100	11	R606	18
J100	18	R608	18
P100	18	R610	18
Q100	11	R614	18
Q120	11	R618	18
Q140	11	R620	18
Q160	11	R622	18
Q200	11	R624	18
Q220	11	VR260	11
Q240	11		

A4—CONTROL BOARD

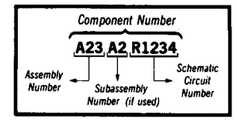
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C100	11	J942	17	R256	11	TP100	11
C102	11	J942	17	R258	11	TP102	11
C104	11	J942	17	R259	11	U100	17
C106	11	K270	11	R260	11	U110A	17
C108	11	L100	11	R266	11	U110B	17
C110	11	L102	11	R268	11	U120A	11
C120	17	L104	11	R272	11	U120B	17
C122	11	L106	11	R274	11	U140	17
C124	11	L108	11	R275	11	U160A	17
C126	11	P100	11	R276	11	U160B	17
C140	17	P200	11	R277	11	U180	17
C180	11	P270	11	R278	11	U200	11
C206	11	P420	17	R280	11	U220B	11
C220	11	P830	17	R281	11	U220C	11
C230	11	P830	17	R282	11	U220A	17
C232	11	P830	17	R283	11	U270A	11
C400	11	R100A	17	R284	11	U270B	11
C420	11	R100B	17	R286	11	U270C	11
C428	17	R100C	17	R288	11	U270D	11
C431	17	R100D	17	R290	11	U270E	11
C432	17	R100E	17	R291	11	U280A	11
C440	11	R100F	17	R292	11	U280B	11
C460	11	R100G	17	R293	11	U280C	11
CR120	17	R100H	17	R294	11	U280D	11
CR122	17	R120	17	R296	11	U280E	11
CR124	17	R122	17	R298	11	U400	17
CR142	17	R124	17	R299	11	U402A	17
CR144	17	R126	17	R410	17	U402B	17
CR270	11	R128	17	R412	17	U402C	17
CR290	11	R130	17	R420	17	U410	17
CR296	11	R132	17	R430	17	U420	17
CR430	17	R136	17	R432	17	U430	17
CR440	17	R202	11	R433	17	U440	17
CR442	17	R210	11	R440	17	U442A	17
CR444	17	R211	11	R442	17	U442B	17
CR446	17	R212	11	R444	17	U442C	17
CR448	17	R213	11	R446	17	U442D	17
CR450	17	R214	11	R450	17	U442E	17
J940	11	R216	11	R470	17	U450	17
J940	11	R220	11	R472	17	U470A	17
J940	17	R222	11	R474	17	U470B	17
J940	17	R224	11	R480	17	U470C	17
J940	17	R226	11	R484	17	U472A	17
J940	17	R228	11	R486	17	U472B	17
J940	17	R230	11	R490	17	U472C	17
J940	17	R232	11	R492	17	U480	17
J940	17	R234	11	R494	17	U490	17
J940	17	R250	11	R496	17		
J942	11	R252	11	RT432	17		
J942	17	R254	11	RT440	17		

A12—HORIZONTAL OUTPUT

A4—CONTROL



COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

HORIZONTAL PREAMP & OUTPUT AMPLIFIER

11

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
MF	6B	4A	P920	4B	2G	P940	4B	3G	P942	6B	3A
			P920	7B	2G	P940	7B	3G			

Partial A1 also shown on diagrams 1, 2, 3, 4, 5, 6, 7, 9, 12, 13, 15, 17, 18 and 19.

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	8C	3H	K270	3J	2G	R234	2D	2F	R293	3G	2G
C102	7C	2G				R250	4G	1G	R294	4G	2H
C104	8C	3H	L100	8C	3H	R252	6F	2F	R296	4G	1H
C106	9C	3G	L102	7C	3G	R254	2F	2F	R298	4G	1H
C108	8C	1A	L104	8C	3H	R256	2F	2F	R299	4G	1G
C110	9C	2G	L106	9C	3G	R258	4H	2G			
C122	9C	3F	L108	9C	3G	R259	6E	2F	TP100	8B	2D
C124	9C	2A				R260	3H	1G	TP102	9B	2B
C126	8D	2F	P100	2B	1F	R266	3J	1G			
C180	8C	2B	P200	3B	1F	R268	4H	1G	U120A	6E	2F
C206	4D	2E	P270	2L	1F	R272	6F	2F	U200	2E	2F
C220	6E	2F				R274	2F	2F	U220B	6D	3F
C230	1E	2F	R202	4C	3G	R275	2H	2G	U220C	5D	3F
C232	3E	2F	R210	6C	3A	R276	4K	2G	U270A	2F	2G
C400	8D	3B	R211	6D	2F	R277	6H	2G	U270B	6F	2G
C420	8D	3C	R212	6E	2F	R278	4K	1G	U270C	6H	2G
C440	8D	2C	R213	6C	3A	R280	5K	1G	U270D	2H	2G
C460	8D	3D	R214	2E	2F	R281	6K	2G	U270E	4G	2G
			R216	6D	3A	R282	5L	1G	U280A	3H	2G
CR270	4H	1E	R220	2C	1F	R283	6K	3G	U280B	5H	2G
CR290	5G	1E	R222	2C	1F	R284	5L	1G	U280C	6K	2G
CR296	4G	1H	R224	3C	2F	R286	5K	1G	U280D	4L	2G
			R226	3C	2F	R288	5K	1G	U280E	4G	2G
J940	4B	3G	R228	2C	1F	R290	5G	1D			
J940	7B	3G	R230	1E	2F	R291	3G	2G			
J942	6B	3A	R232	3E	2F	R292	5G	1G			

Partial A4 also shown on diagram 17.

ASSEMBLY A12

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	9M	3C	HA	2S	2A	Q220	6M	3B	R162	1P	2A
C102	9M	2C	HA	7S	2A	Q240	6N	3A	R200	5N	3B
C120	1N	1A				Q260	7P	3A	R202	5N	3B
C130	2P	2B	HB	2L	3C				R210	6M	2B
C220	7N	3B				R100	4N	2B	R222	7N	3B
C230	7N	3B	J100	8M	1B	R106	4M	3B	R230	7N	3B
						R110	2N	2B	R244	7P	2A
CR100	4M	2B	Q100	2M	2B	R122	1N	2B	R262	7P	3B
CR106	2N	2B	Q120	2N	2B	R130	2P	2B	R264	4S	3A
CR120	4N	2B	Q140	2P	1B	R140	4P	2B			
CR206	6M	2B	Q160	1P	1A	R142	4P	2B	VR260	4S	1A
CR220	4M	2B	Q200	6M	3B	R144	2P	2A			

Partial A12 also shown on diagram 18.

SEE TEST WAVEFORM SETUP ADJACENT TO DIAGRAM 1

WAVEFORMS FOR DIAGRAM 12

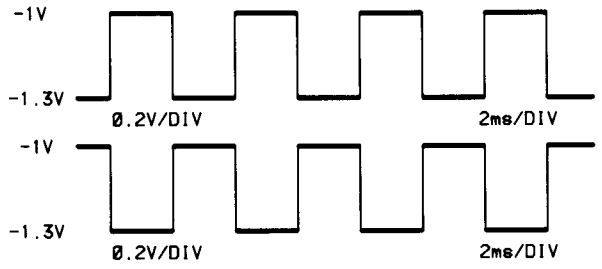
WAVEFORMS 31 THROUGH 35 HAVE THE FOLLOWING 336 CONTROL SETTINGS:

AC-GND-DC .....GND
CH1 POSITION .....FULLY CW
CH2 POSITION .....FULLY CCW
A SEC/DIV.....0.5 S ROLL

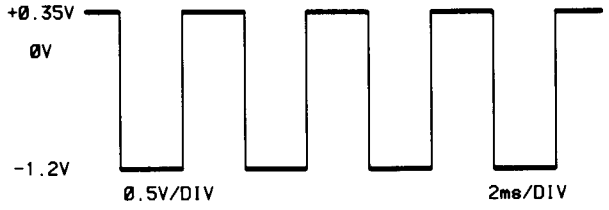
WAVEFORMS 36 THROUGH 40 HAVE THE FOLLOWING 336 CONTROL SETTINGS:

AC-GND-DC .....DC
VERT MODE.....CH1
A SEC/DIV.....0.1 μs/DIV
DISPLAY MODE .....STORE
DISPLAY CENTERED AND 336 TRIGGERED ON 1 MHz SQUARE-WAVE SIGNAL INPUT.

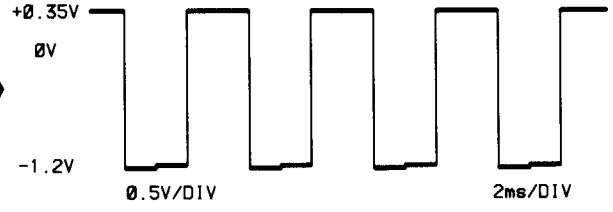
31



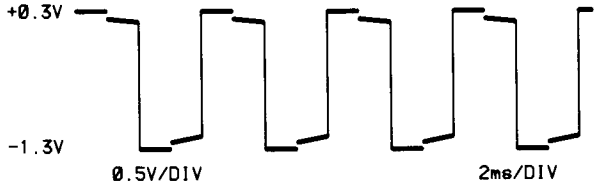
32



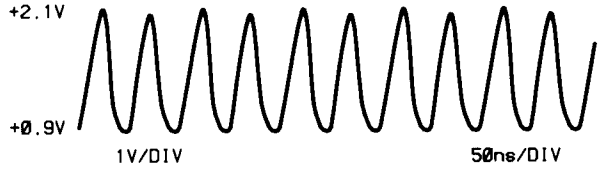
33



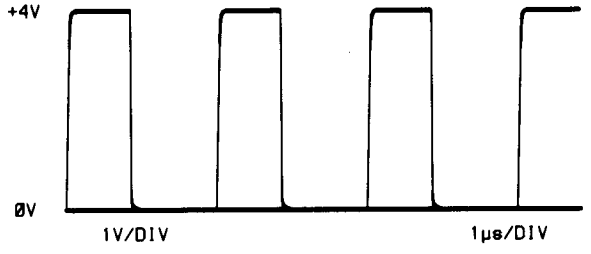
34



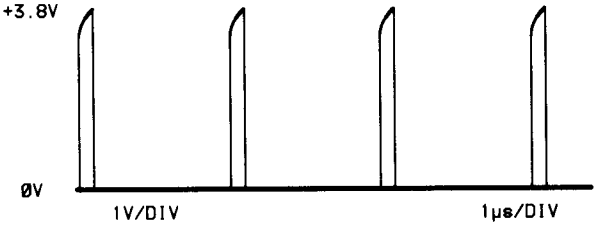
35



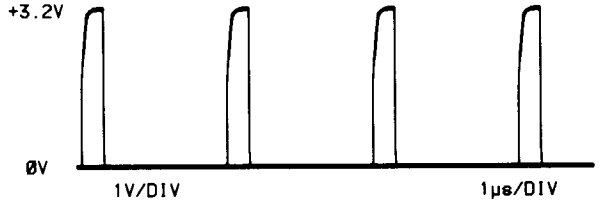
36



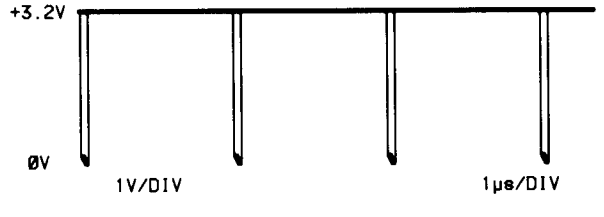
37



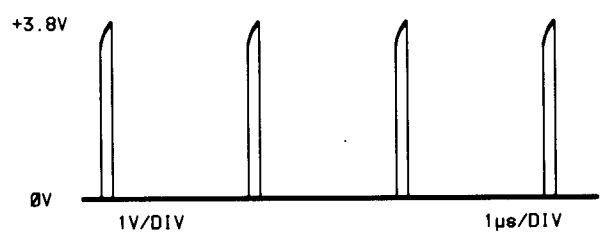
38



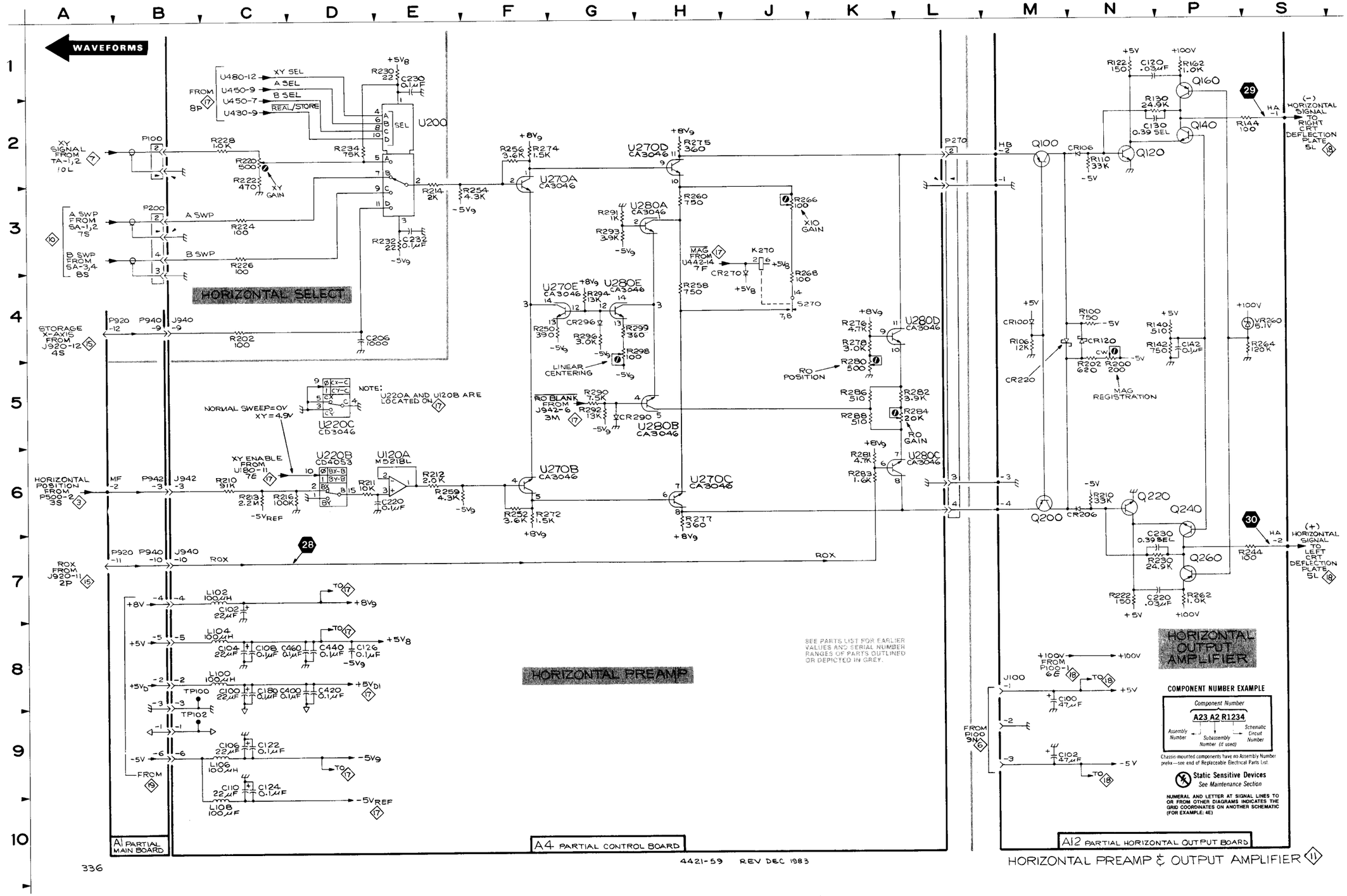
39



40



4421-72


WAVEFORMS
HORIZONTAL SELECT
HORIZONTAL PREAMP
HORIZONTAL OUTPUT AMPLIFIER
A1 PARTIAL MAIN BOARD
A4 PARTIAL CONTROL BOARD
A12 PARTIAL HORIZONTAL OUTPUT BOARD
HORIZONTAL PREAMP & OUTPUT AMPLIFIER 11
4421-59 REV DEC 1983
336
XY SEL
A SEL
B SEL
REAL/STORE
SEL
U200
XY GAIN
A SWP
B SWP
U270A CA3046
U270D CA3046
U280A CA3046
U270E CA3046
U280E CA3046
U280B CA3046
U270B CA3046
U270C CA3046
U280D CA3046
U280C CA3046
U220C CD3046
U220B CD4053
U120A M5218L
XIO GAIN
LINEAR CENTERING
RO POSITION
RO GAIN
RO BLANK
XY ENABLE
NORMAL SWEEP=0V
XY=4.9V
NOTE: U220A AND U120B ARE LOCATED ON 17
HORIZONTAL POSITION
STORAGE X-AXIS
ROX
Q100
Q120
Q140
Q160
Q200
Q220
Q240
Q260
CR106
CR220
MAG REGISTRATION
(-) HORIZONTAL SIGNAL TO RIGHT CRT DEFLECTION PLATE 5L
(+) HORIZONTAL SIGNAL TO LEFT CRT DEFLECTION PLATE 5L
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)

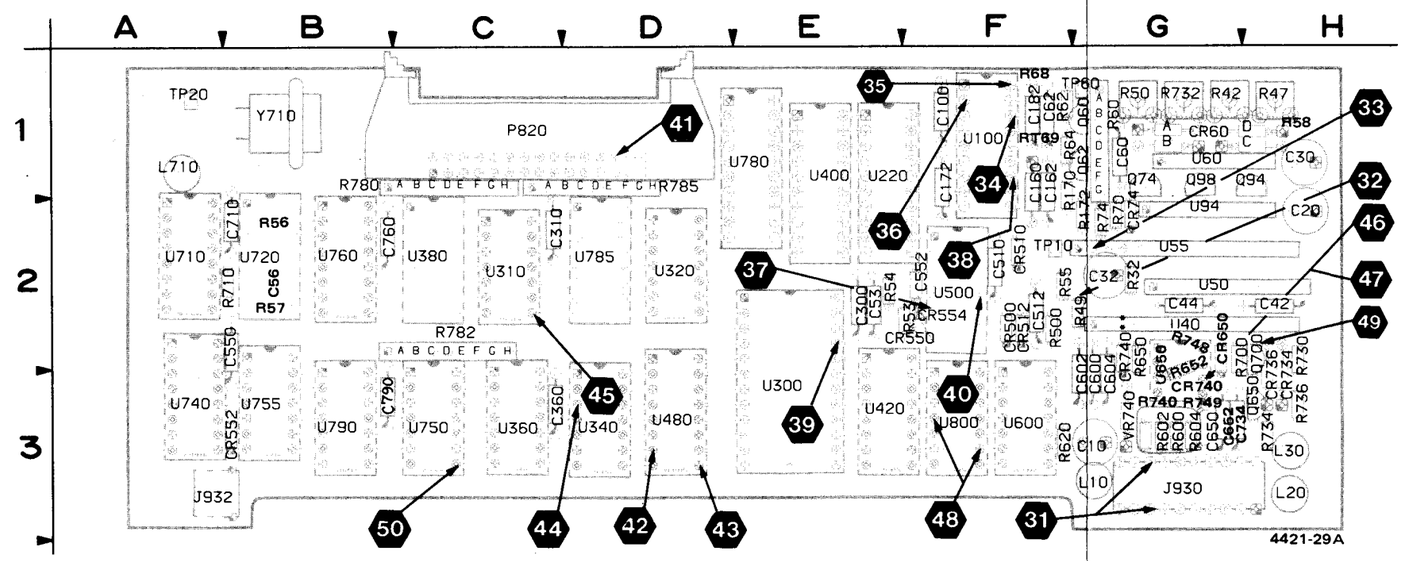


Figure 9-14. A5—Acquisition board.

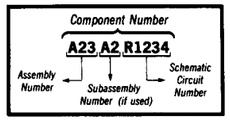
**Earlier location.

USE OF THE EXTENDER CIRCUIT BOARDS AND CABLES SUPPLIED IN THE SERVICE MAINTENANCE KIT PROVIDES EASE OF ACCESS TO THE WAVEFORM TEST POINTS.

A5—ACQUISITION BOARD

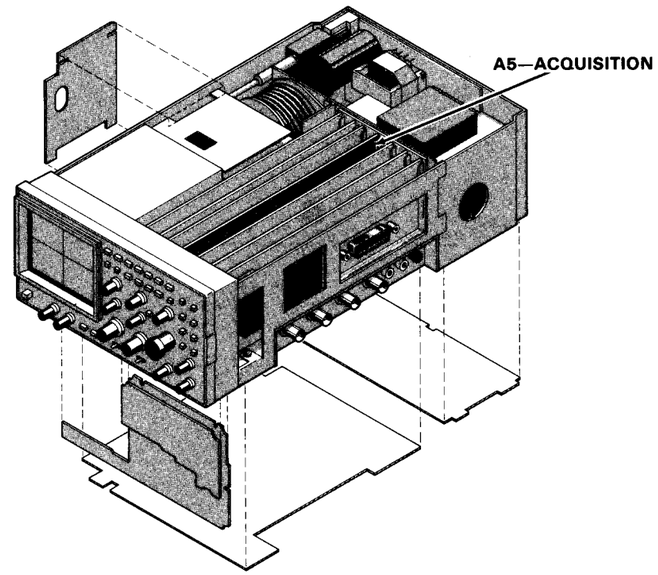
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C10	12	CR650	13	R600	13	U310A	13
C20	12	CR734	13	R602	13	U310B	13
C30	12	CR736	13	R604	13	U320	13
C32	12	CR740	13	R620	13	U340A	13
C42	12	J930	12	R650	13	U340B	13
C44	12	J930	13	R652	13	U360A	13
C53	12	J932	12	R700	13	U360B	13
C56	12	L10	12	R710	13	U380	13
C60	12	L20	12	R730	13	U400	12
C62	12	L30	12	R732	13	U420A	12
C100	12	L710	13	R734	13	U420B	13
C160	12	P820	13	R736	13	U420C	13
C162	12	Q60	12	R740	13	U420D	13
C172	12	Q62	12	R748	13	U420E	13
C182	12	Q74	12	R749	13	U480	13
C300	12	Q94	12	R780	13	U500	12
C310	12	Q98	12	R782A	13	U600	13
C360	12	Q650	13	R782B	13	U650	13
C510	12	Q700	13	R782C	13	U710	13
C512	12	R32	12	R782D	13	U720	13
C550	12	R42	12	R782F	13	U740A	13
C552	12	R47	12	R782G	13	U740B	13
C600	13	R49	12	R785A	13	U750A	13
C602	13	R50	12	R785B	13	U750B	13
C604	13	R53	12	R785C	13	U755A	13
C650	13	R54	12	R785D	13	U755B	13
C652	13	R55	12	R785E	13	U755C	13
C710	12	R56	12	R785F	13	U755D	13
C734	13	R57	12	R785H	13	U760	13
C760	12	R58	12	RT69	12	U780	13
C790	12	R60	12	TP10	12	U785A	13
CR60	12	R62	12	TP20	12	U785B	13
CR74	12	R64	12	TP60	12	U790A	13
CR500	12	R68	12	U40	12	U790B	13
CR510	12	R70	12	U50	12	U800A	12
CR512	12	R74	12	U55	12	U800B	13
CR550	12	R170	12	U60	12	U800C	13
CR552	12	R172	12	U94	12	U800D	13
CR554	12	R500	12	U100	12	VR740	13
				U220	12	Y710	13
				U300	12		

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



REV DEC 1983

ACQUISITION (12)

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P930	1B	3G						

Partial A1 also shown on diagrams 1, 2, 3, 4, 5, 6, 7, 9, 11, 13, 15, 17, 18 and 19.

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C10	2B	3G	CR500	3G	2F	R56*	9E	2B
C20	2C	2H	CR510	3G	2F	R57*	10F	2B
C30	3C	1H	CR512	3H	2F	R58*	9F	1H
C32	1B	2G	CR550	2N	2F	R60A	7J	1G
C42	7B	2H	CR552	2N	3B	R60B	8H	1G
C44	8B	2G	CR554	2M	2F	R60C	8H	1G
C53	9C	2E				R62	8J	1F
C56*	10E	2B	J930	1B	3G	R64	8J	1F
C60	8H	1G	J930	7B	3G	R68*	9J	1F
C62	7J	1F	J932	2P	3A	R70	5G	2G
C100	2K	1F				R74	6G	2G
C160	5J	1F	L10	2B	3G	R170	6J	1F
C162	5J	1F	L20	2B	3H	R172	6J	2G
C172	6J	1F	L30	3B	3H	R500	3H	2F
C182	9K	1F				RT69*	9J	1F
C300	2C	2E	P820	1P	1C	TP10	3B	2F
C310	2C	2C				TP20	2B	1A
C360	2C	3C	Q60	7J	1G	TP60	8J	1F
C510	4E	2F	Q62	8J	1G			
C512	2J	2F	Q74	6G	1G	U40	8B	2G
C550	2N	2B	Q94	6F	1H	U50	7D	2G
C552	2M	2F	Q98	6H	1G	U55	7F	2G
C710	2D	2B				U60	6G	1G
C760	2D	2B	R32	1B	2G	U94	5G	2G
C790	2D	3C	R42	7C	1G	U100	4K	1F
CR60A	8F	1G	R47	8C	1H	U220	5N	1E
CR60B	8F	1G	R49	8C	2G	U300	3N	3E
CR60C	8F	1G	R50	8H	1G	U400	4P	1E
CR60D	8F	1G	R53	9C	2F	U420A	4G	3E
CR74	5G	2G	R54	9C	2E	U500	3F	2F
			R55	9D	2F	U800A	9C	3F

Partial A5 also shown on diagram 13.

***See Parts List for serial number ranges.**

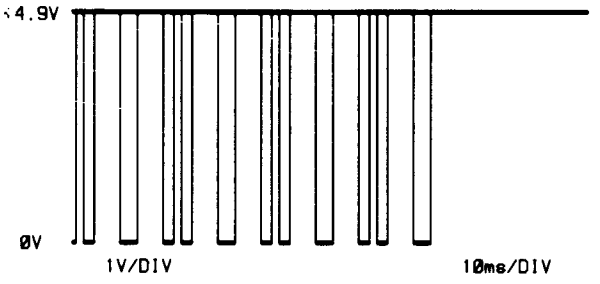
SEE TEST WAVEFORM SETUP ADJACENT TO DIAGRAM 1

WAVEFORMS FOR DIAGRAM 13

WAVEFORMS 41 THROUGH 42 HAVE THE FOLLOWING 336 CONTROL SETTINGS:

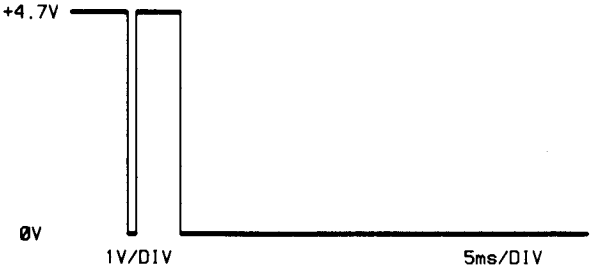
VERT MODE.....CH1
SEC/DIV .....1 ms
HORIZONTAL
DISPLAY MODE .....A
DISPLAY SIGNAL.....1 kHz SQUARE WAVE
TEST SCOPE TRIGGERED ON WAVEFORM 34 (RDACQ).

41



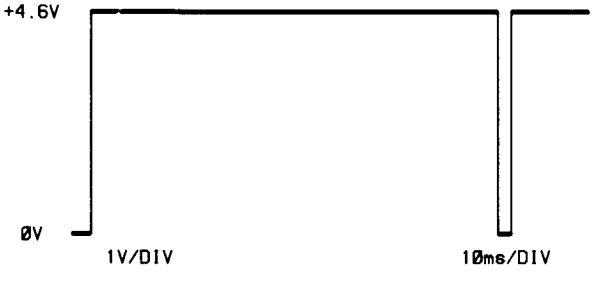
42

43

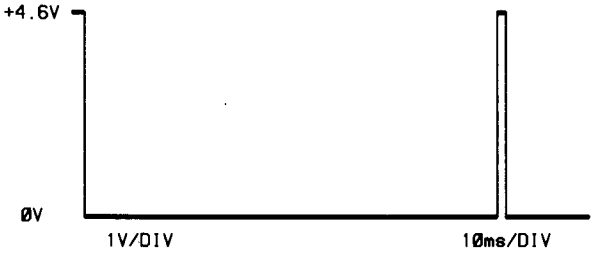


SET 336 A SEC/DIV TO 0.1 ms
FOR WAVEFORMS 44 THROUGH 46.

44

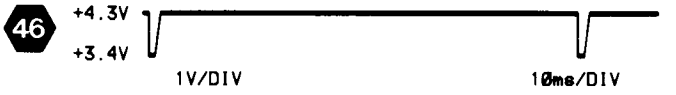


45



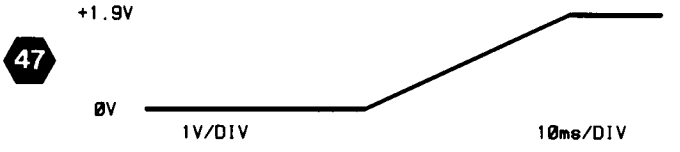
USE OF THE EXTENDER CIRCUIT BOARDS AND CABLES SUPPLIED IN THE SERVICE MAINTENANCE KIT PROVIDES EASE OF ACCESS TO THE WAVEFORM TEST POINTS.

46

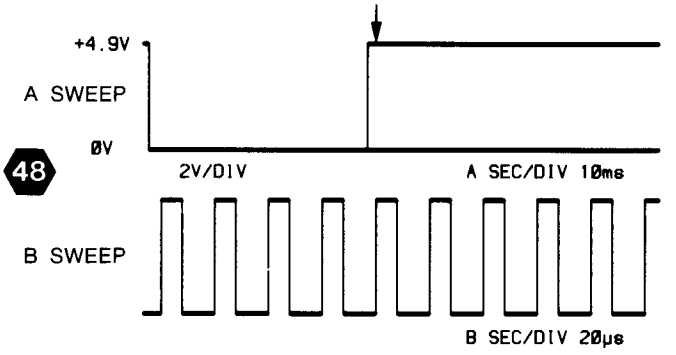


SET 336 A SEC/DIV TO 1 μs AND DISPLAY SIGNAL TO 1 MHz FOR WAVEFORMS 47 & 48.

47

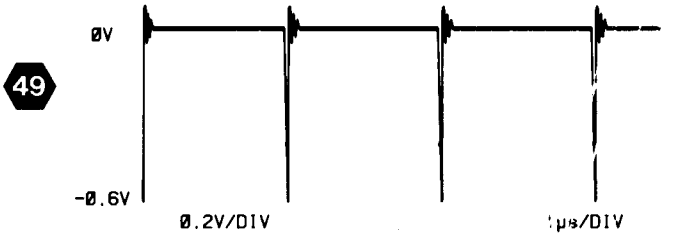


48



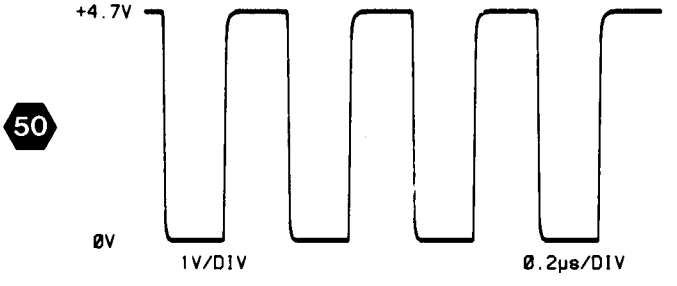
SET 336 A SEC/DIV TO 0.1 μs.

49



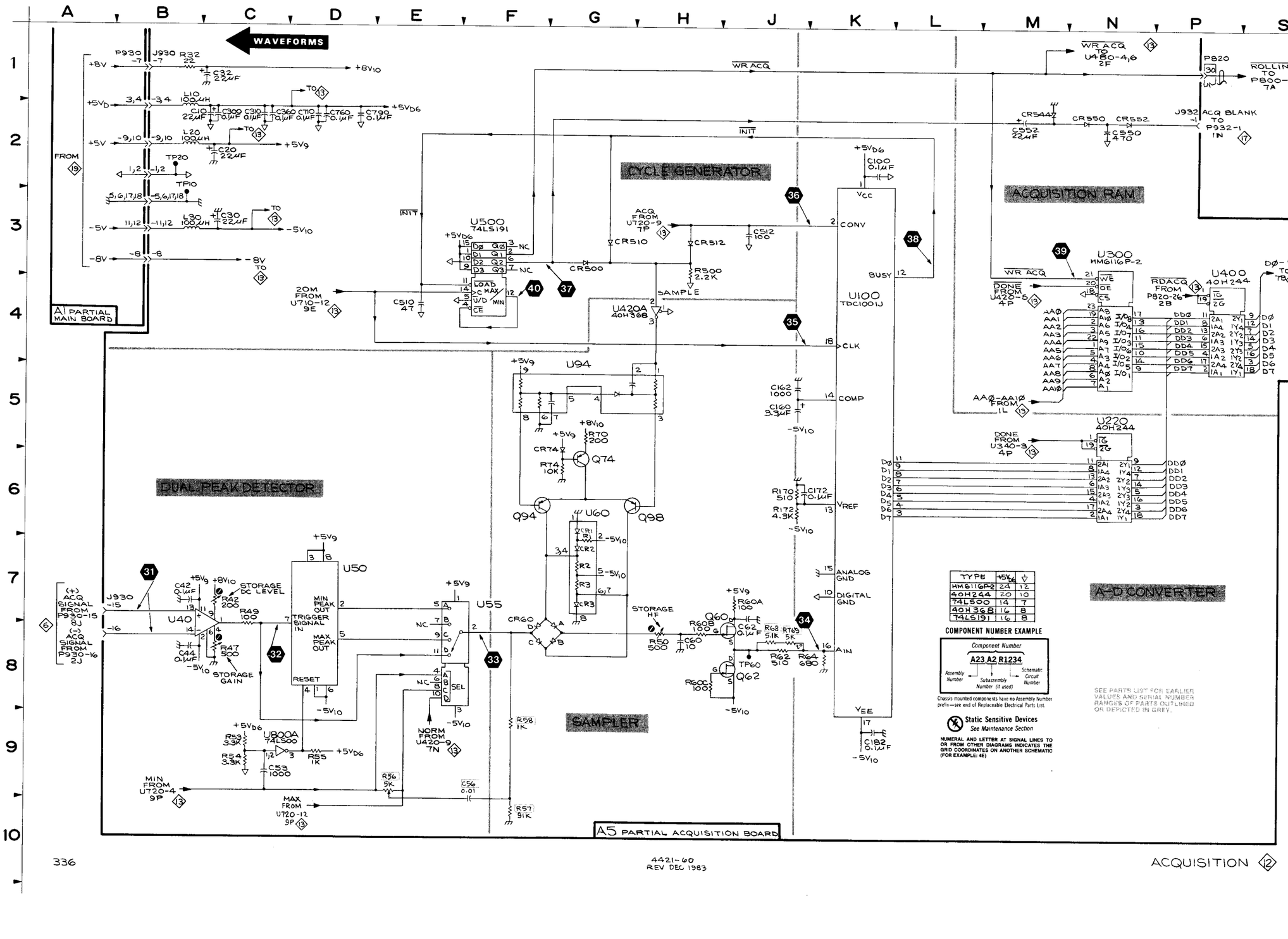
SET 336 A SEC/DIV TO 0.1 ms.

50



4421-73

TIME BASE & ACQUISITION CONTROL WAVEFORMS


WAVEFORMS
CYCLE GENERATOR
ACQUISITION RAM
DUAL PEAK DETECTOR
SAMPLER
A-D CONVERTER
A1 PARTIAL MAIN BOARD
A5 PARTIAL ACQUISITION BOARD
U500 74LS191
U100 TDC1001J
U300 HM6116P-2
U400 40H244
U220 40H244
U94
U60
U50
U40
U55
U800A 74LS00
U420A 40H36B
WR ACQ
INIT
ROLLINT
ACQ BLANK
SAMPLE
BUSY
CONV
CLK
COMP
VREF
VEE
AIN
ANALOG GND
DIGITAL GND
STORAGE DC LEVEL
STORAGE GAIN
STORAGE HF
TRIGGER SIGNAL IN
MIN PEAK OUT
MAX PEAK OUT
RESET
NORM
SEL
TYPE | +5V | 0V
HM6116P-2 | 24 | 12
40H244 | 20 | 10
74LS00 | 14 | 7
40H36B | 16 | 8
74LS191 | 16 | 8
COMPONENT NUMBER EXAMPLE
Component Number
A23,A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

TIME BASE & ACQUISITION CONTROL 13

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P930	3B	3G	P950	3A	4G			
P940	3A	3G	P950	5A	4G			

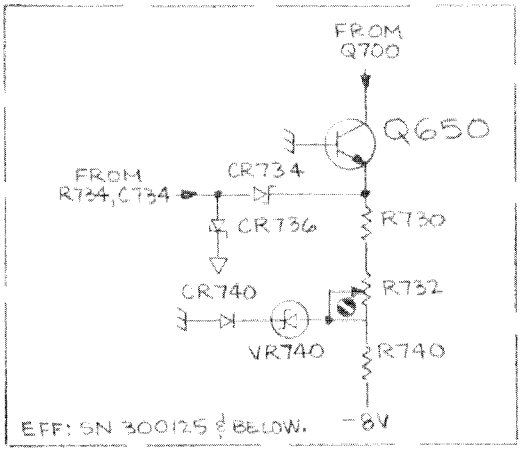
Partial A1 also shown on diagrams 1, 2, 3, 4, 5, 6, 7, 9, 11, 12, 15, 17, 18 and 19.

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C600	5C	3G	R710	10E	2B	U420B	3P	3E
C602	5C	3G	R730	7D	3H	U420C	2G	3E
C604	5C	3G	R732	7D	1G	U420D	8M	3E
C650	6D	3G	R734	6B	3H	U420E	6J	3E
C652	6D	3G	R736	7B	3H	U480	3F	3D
C734	6B	3G	R740	6C	3G	U600	5D	3F
			R748*	6C	3G	U650	6D	3G
CR650	6D	2G	R749*	6C	3G	U710	9D	2A
CR734	7C	3H	R780	7B	1B	U720	8P	2B
CR736	7C	3H	R782A	4M	2C	U740A	9F	3A
CR740	6C	3G	R782B	4M	2C	U740B	9H	3A
			R782C	9J	2C	U750A	7K	3C
J930	3B	3G	R782D	5H	2C	U750B	7L	3C
			R782F	2F	2C	U755A	8N	3B
L710	9D	1A	R782G	2F	2C	U755B	4K	3B
			R785A	3S	1D	U755C	9K	3B
P820	2B	1C	R785B	9P	1D	U755D	5H	3B
P820	3S	1C	R785C	9B	1D	U760	7G	2B
P820	7A	1C	R785D	9B	1D	U780	7D	1E
			R785E	2C	1D	U785A	9C	2D
Q650	6C	3H	R785F	9B	1D	U785B	4G	2D
Q700	6C	2H	R785H	2E	1D	U790A	7J	3B
						U790B	7G	3B
R600	5C	3G	U310A	2L	2C	U800B	5D	3F
R602	5C	3G	U310B	2M	2C	U800C	5G	3F
R604	6C	3G	U320A	1H	2D	U800D	5G	3F
R620	5F	3F	U320B	1J	2B			
R650	6D	2G	U340A	3M	3D	VR740*		3G
R652	6D	3G	U340B	1K	3D			
R700	6C	2H	U360A	4K	3C	Y710	10D	1B
			U360B	4J	3C			
			U380	3M	2C			

Partial A5 also shown on diagram 12.

***See Parts List for serial number ranges.**



SEE TEST WAVEFORM SETUP ADJACENT TO DIAGRAM 1

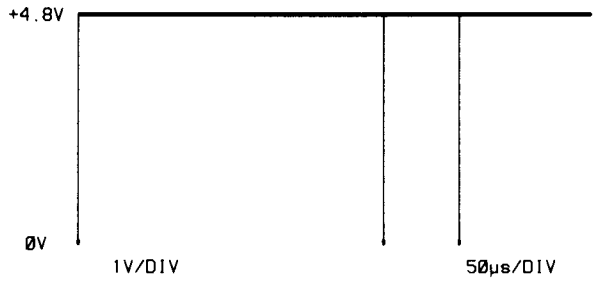
WAVEFORMS FOR DIAGRAM 14

WAVEFORMS 51 THROUGH 58 HAVE THE FOLLOWING 336 CONTROL SETTINGS:

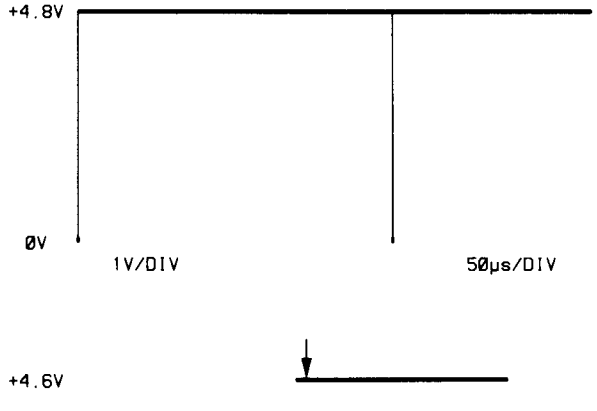
HORIZONTAL
DISPLAY MODE .....A
A SEC/DIV.....1 μs
DISPLAY SIGNAL.....1 kHz SQUARE WAVE

USE OF THE EXTENDER CIRCUIT BOARDS AND CABLES SUPPLIED IN THE SERVICE MAINTENANCE KIT PROVIDES EASE OF ACCESS TO THE WAVEFORM TEST POINTS.

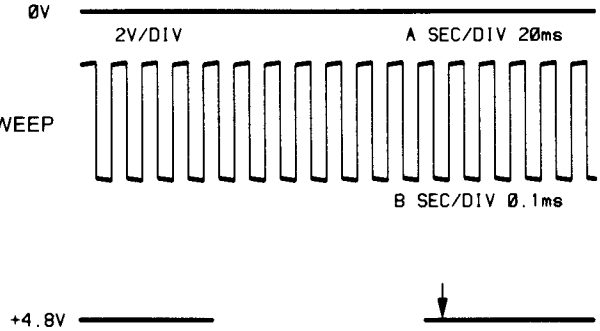
51



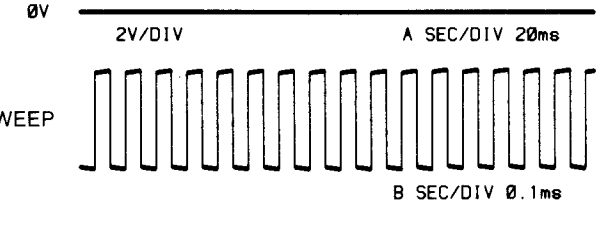
52



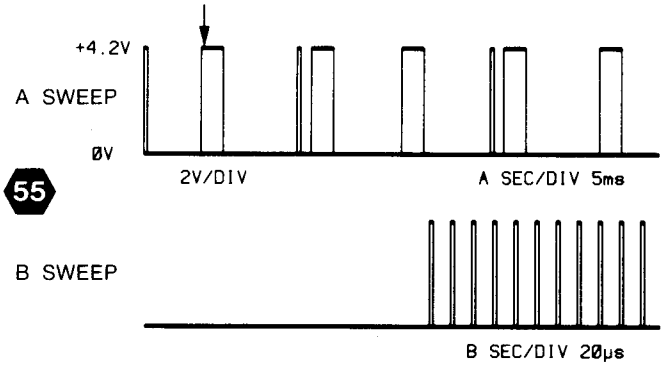
53



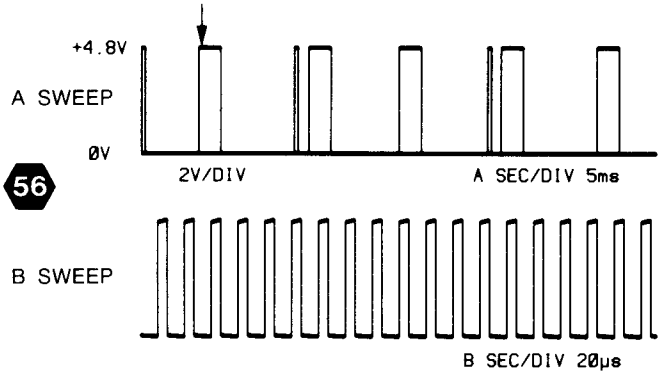
54



55

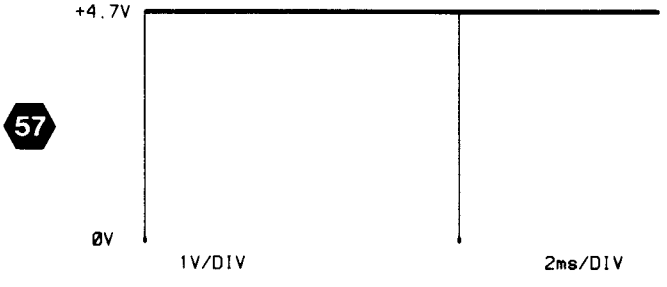


56

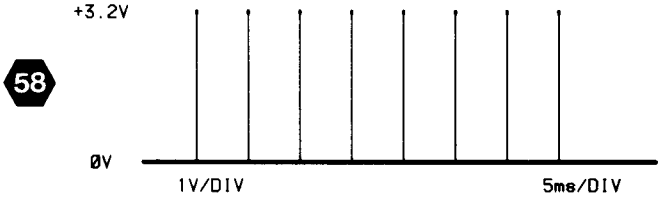


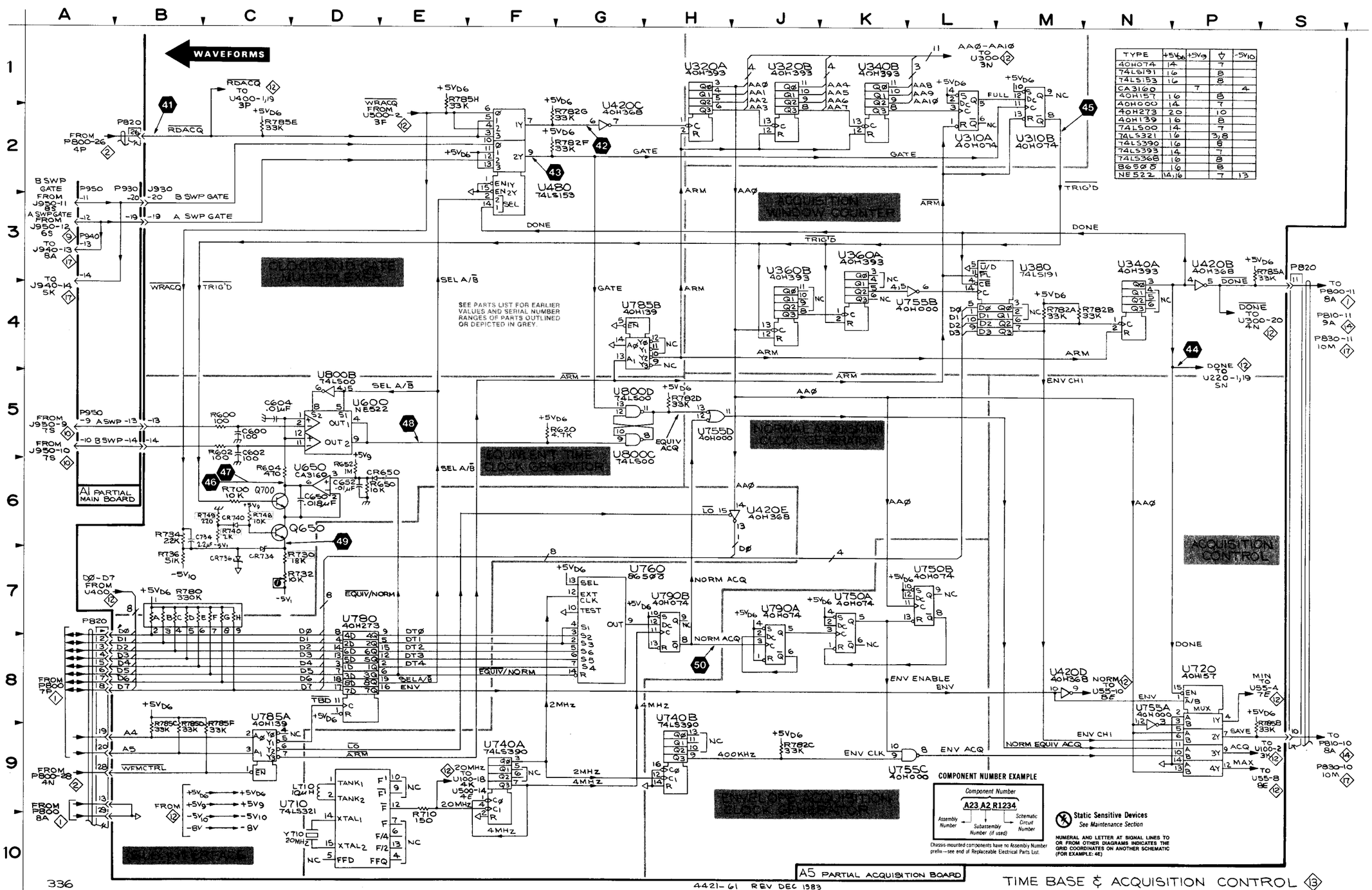
SET 336 CURSOR MODE .....ON

57



58





4421-61 REV DEC 1983

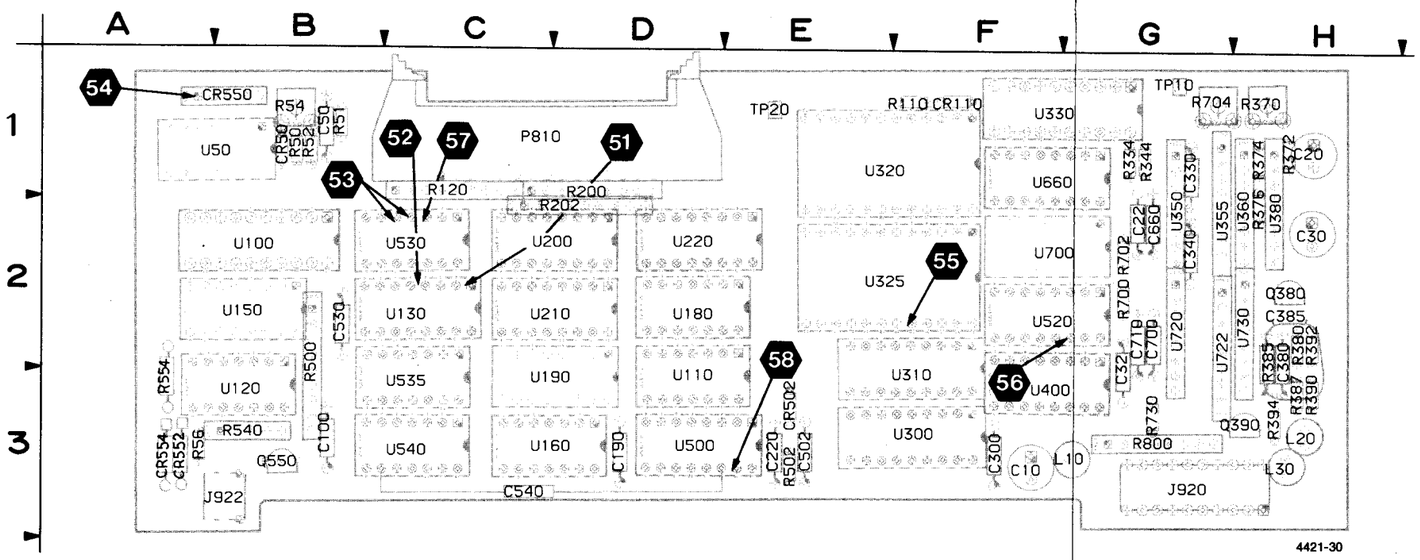
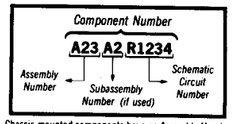


Figure 9-15. A6—Display board.

A6—DISPLAY BOARD

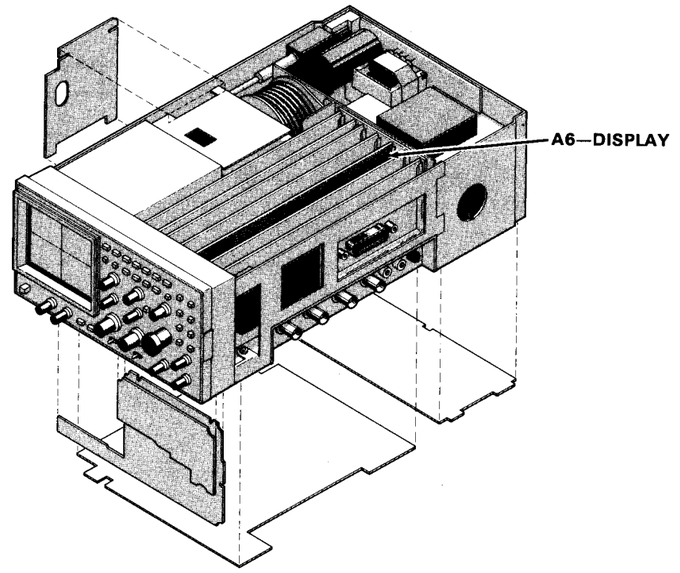
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C10	15	R51	15	R500E	14	U200	14
C20	15	R52	15	R500F	14	U210	14
C22	15	R54	15	R500G	14	U220	14
C30	15	R56	15	R500H	14	U300	14
C32	15	R110	14	R502	14	U310	14
C50	15	R120	14	R540A	14	U320	14
C100	15	R200A	14	R540B	14	U325	14
C190	15	R200B	14	R540C	14	U330	15
C220	15	R200C	14	R540D	14	U350A	15
C300	15	R200D	14	R554	14	U350B	15
C330	15	R200E	14	R700	15	U355	15
C340	15	R200F	14	R702	15	U360A	15
C380	15	R200G	14	R704	15	U360B	15
C385	15	R200H	14	R730	15	U380A	15
C502	14	R202A	14	R800A	15	U380B	15
C530	14	R202B	14	R800C	15	U400A	15
C540	14	R202C	14	R800D	15	U400B	15
C660	15	R202D	14	TP10	15	U400C	15
C700	15	R202E	14	TP20	15	U500	14
C710	15	R202F	14	U50	14	U520	14
CR50	15	R202G	14	U50	14	U530A	14
CR110	14	R202H	14	U50	15	U530B	14
CR502	14	R334	15	U50	15	U530C	14
CR550	14	R344	15	U100	14	U530D	14
CR552	14	R370	15	U110A	14	U535A	14
CR554	14	R372	15	U110B	14	U535B	14
J920	15	R374	15	U110C	14	U540A	14
J920	15	R376	15	U110D	14	U540B	14
J922	14	R380	15	U120A	14	U540C	14
J922	14	R385	15	U120B	14	U660	15
L10	15	R387	15	U130A	14	U700	15
L20	15	R390	15	U130B	14	U720	15
L30	15	R392	15	U150	14	U720	15
P810	14	R394	15	U160A	14	U722	15
Q380	15	R500A	14	U160B	14	U730	15
Q390	15	R500B	14	U180A	14	U730	15
Q550	14	R500C	14	U180B	14		
R50	15	R500D	14	U190	14		

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section



DISPLAY MEMORY & DISPLAY CONTROL

ASSEMBLY A6

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C502	6M	3D	R202C	1C	2C	U120B	7G	3A
C530	8C	2B	R202D	1C	2C	U130A	5D	2C
C540	6M	3B	R202E	1C	2C	U130B	3D	2C
			R202F	5C	2C	U150	4F	2B
CR110	4H	1F	R202G	4C	2C	U160A	7C	3B
CR502	4M	3D	R202H	8B	2C	U160B	7D	3B
CR550	8D	1A	R500A	4H	2B	U180A	7E	2D
CR552	9C	3A	R500B	4F	2B	U180B	7E	2D
CR554	9C	3A	R500C	4H	2B	U190	7H	3B
			R500D	8D	2B	U200	2J	2C
J922	5S	3A	R500E	5N	2B	U210	2G	2C
J922	8E	3A	R500F	4H	2B	U220	1F	2D
			R500G	5P	2B	U300	5L	3E
P810	1A	1C	R500H	5N	2B	U310	7L	3E
			R502	6M	3D	U320	4L	1E
Q550	8E	3A	R540A	5S	3A	U325	2L	2E
			R540B	5S	3A	U500	5M	3C
R110	3H	1F	R540C	5N	3A	U520	8M	2F
R120	5C	1C	R540D	5N	3A	U530A	8N	2C
R200A	1B	1D	R554	9D	2A	U530B	8C	2C
R200B	1B	1D				U530C	7B	2C
R200C	1B	1D	U50C	8C	1A	U530D	7C	2C
R200D	1B	1D	U50D	8C	1A	U535A	9P	3B
R200E	1B	1D	U100	9J	2B	U535B	8S	3B
R200F	1B	1D	U110A	3H	3C	U540A	5P	3B
R200G	1B	1D	U110B	3H	3C	U540B	8N	3B
R200H	2E	1D	U110C	7N	3C	U540C	6P	3B
R202A	1C	2C	U110D	3G	3C			
R202B	1C	2C	U120A	8G	3A			

Partial A6 also shown on diagram 15.

TYPE	+5VD7	
40H244	20	10
40H002	14	7
HM6147	18	9,5
HM6116	24	12
74LS379	16	8
40H175	16	8
40H011	14	7
40H000	14	7
40H393	14	7
40H153	16	8
40H157	16	8
40H074	14	7
40H139	16	8
74LS137	16	8

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
(Assembly Number – Subassembly Number (if used) – Schematic Circuit Number)

Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List

Static Sensitive Devices
See Maintenance Section

NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)

P/O DISPLAY CONTROL

WAVEFORMS

BUS INTERFACE

DISPLAY ADDRESS COUNTER

P/O DISPLAY CONTROL

DISPLAY MEMORY

CURSOR LOGIC

A6 PARTIAL DISPLAY BOARD

336

4421-62

DISPLAY MEMORY & DISPLAY CONTROL 14

STORAGE DISPLAY & READOUT

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P222	4S	7F	P920	4P	2G	P920	8B	2G

Partial A1 also shown on diagrams 1, 2, 3, 4, 5, 6, 7, 9, 11, 12, 13, 17, 18 and 19.

ASSEMBLY A6

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C10	9C	3E	Q380	8L	2H	R800D	2N	3F
C20	8C	1H	Q390	9L	3F			
C22	8C	2G				TP10	9C	1G
C30	9C	2H	R50	2B	1B	TP20	9B	1E
C32	9C	2G	R51	2A	1B			
C50	2B	1B	R52	2B	1B	U50A	3A	1A
C100	9C	3A	R54	2B	1B	U50B	3B	1A
C190	9C	3C	R56	3C	3A	U330	5F	1F
C220	9D	3D	R334	6F	1G	U350A	6G	2G
C300	9D	3E	R344	7G	1G	U350B	7G	2G
C330	6F	1G	R370	6K	1H	U355	6J	2G
C340	7F	2G	R372	6K	1H	U360A	6K	2H
C380	8K	2H	R374	6K	1H	U360B	7K	2H
C385	8M	2H	R376	6K	2H	U380A	6L	2H
C660	2F	2G	R380	8K	2H	U380B	9M	2H
C700	3G	2G	R385	9L	2H	U400A	5M	3E
C710	2F	2G	R387	9L	3H	U400B	6N	3E
			R390	9K	3H	U400C	3N	3E
CR50	2B	1B	R392	9K	2H	U660	2F	1F
			R394	9L	3G	U700	4F	2F
J920	1P	3F	R700	7F	2G	U720A	2H	2G
J920	8B	3F	R702	3G	2G	U720B	4H	2G
			R704	3G	1G	U722	2J	2G
L10	9B	3G	R730	4J	3F	U730A	2K	2H
L20	8B	3G	R800A	4N	3F	U730B	3K	2H
L30	9B	3G	R800C	6N	3F			

Partial A6 also shown on diagram 14.

A1 PARTIAL MAIN BOARD

OSCILLATOR

WAVEFORM D-A VECTOR GENERATORS

READOUT D-A VECTOR GENERATORS

STORAGE SWEEP

A6 PARTIAL DISPLAY BOARD

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

TYPE	+5V10	+5V07	⏚	⏥	-5V11
AD7524	14			3	
AD7528	17			1,5	
CD4053	6,8	16			7
40H000	14		7		
M5218L	8				4

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
(Assembly Number → Subassembly Number (if used) → Schematic Circuit Number)

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)

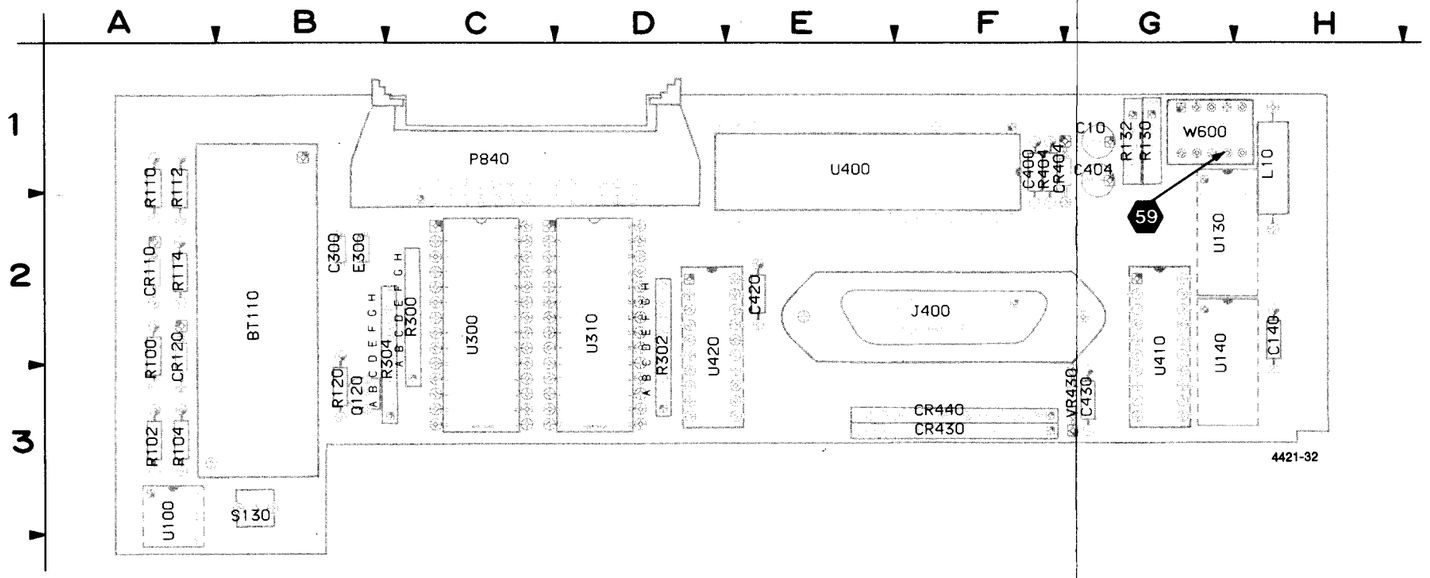
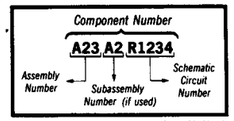


Figure 9-16. A8—Option board.

A8—OPTION

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
BT110	16	R120	16
C10	16	R130C	16
C140	16	R130D	16
C300	16	R132B	16
C400	16	R132C	16
C404	16	R132D	16
C420	16	R300	16
C430	16	R302E	16
CR110	16	R302F	16
CR120	16	R302G	16
CR404	16	R302H	16
CR430	16	R304	16
CR440	16	R404	16
E300	16	S130	16
J400	16	U100	16
L10	16	U130	16
P840	16	U140	16
Q120	16	U300	16
R100	16	U310	16
R102	16	U400	16
R104	16	U410	16
R110	16	U420	16
R112	16	VR430	16
R114	16	W600	2

COMPONENT NUMBER EXAMPLE

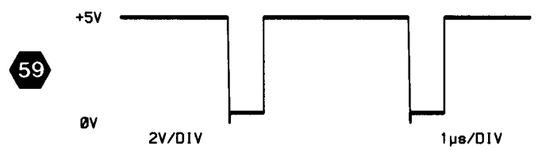


Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

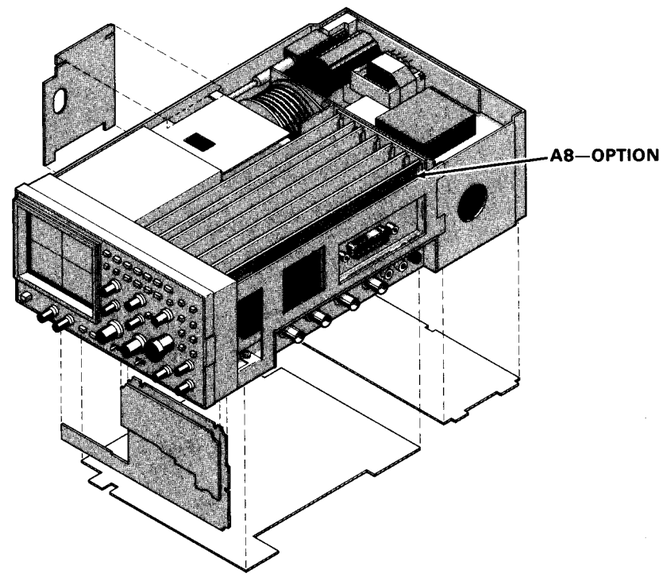
Static Sensitive Devices
See Maintenance Section

SEE TEST WAVEFORM SETUP ADJACENT TO DIAGRAM 1

WAVEFORMS FOR DIAGRAM 16



USE OF THE EXTENDER CIRCUIT BOARDS AND CABLES SUPPLIED IN THE SERVICE MAINTENANCE KIT PROVIDES EASE OF ACCESS TO THE WAVEFORM TEST POINTS.



EXTENDED MEMORY, BATTERY BACKUP & GPIB (OPTIONAL)

16

ASSEMBLY A8

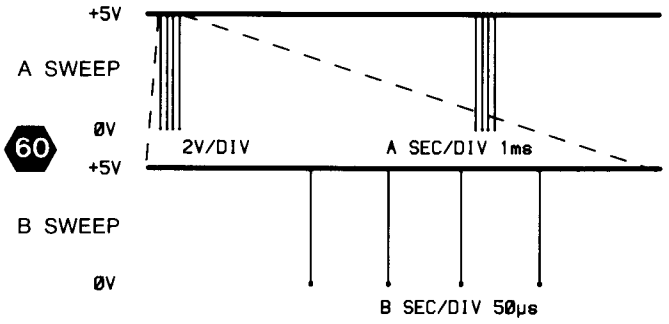
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
BT110	3E	2B	R110	2E	1A
			R112	2E	1A
C10	1B	1G	R114	3E	2A
C140	1B	2H	R120	2D	3B
C300	2F	2B	R130C	2K	1G
C400	1C	1F	R130D	2K	1G
C404	9G	1G	R132B	3H	1G
C420	1C	2E	R132C	2H	1G
C430	10M	3G	R132D	2H	1G
			R300	2C	2C
CR110	2E	2A	R302E	3D	2D
CR120	2E	2A	R302F	8F	2D
CR404	9G	1F	R302G	3D	2D
CR430	10N	3F	R302H	3D	2D
CR440	6N	3F	R304	4D	2B
			R404	9G	1F
E300	2F	2B			
			S130	3E	3B
J400	6S	2F			
			U100	2D	3A
L10	1B	1H	U130	1J	2G
			U140	3J	2G
P840	3A	1C	U300	3M	2C
			U310	3N	2D
Q120	2E	3B	U400	6H	1E
			U410	7K	2G
R100	1C	2A	U420	9K	3D
R102	2D	3A			
R104	2D	3A	VR430	10L	3G

Partial A8 also shown on diagram 2.

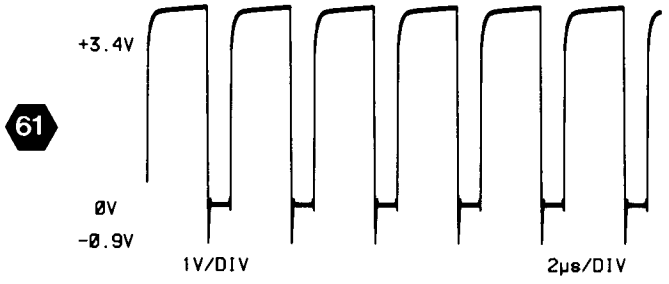
SEE TEST WAVEFORM SETUP ADJACENT TO DIAGRAM 1

WAVEFORMS FOR DIAGRAM 17

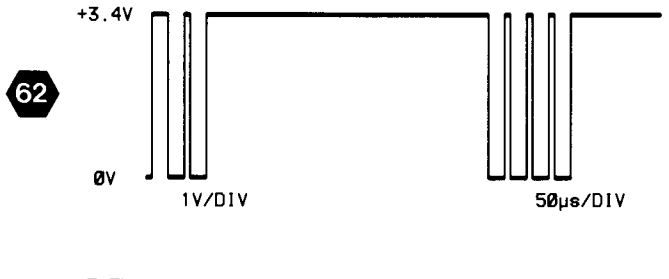
CHANGES TO 336 CONTROL SETTINGS:
HORIZONTAL
DISPLAY MODE .....A
DISPLAY MODE .....STORE
A SEC/DIV.....1 ms
TRIGGER MODE.....SINGLE

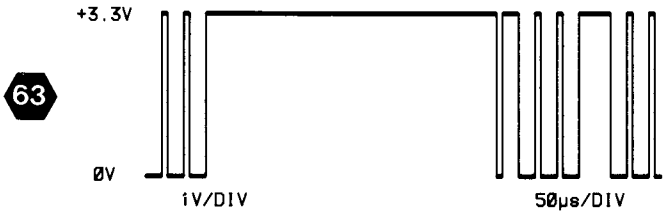


CHANGES TO 336 CONTROL SETTINGS:
DISPLAY MODE .....NONSTORE

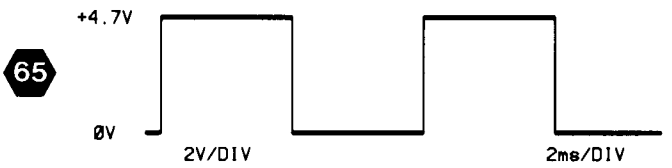


CHANGES TO 336 CONTROL SETTINGS:
HORIZONTAL
DISPLAY MODE .....ALT
SEC/DIV (BOTH).....1 ms

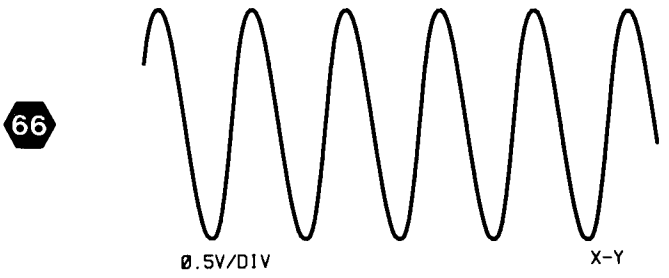




USE OF THE EXTENDER CIRCUIT BOARDS AND CABLES SUPPLIED IN THE SERVICE MAINTENANCE KIT PROVIDES EASE OF ACCESS TO THE WAVEFORM TEST POINTS.



TEST SETUP FOR CHART OUT WAVEFORM.
1. SET:
   VERT MODE.....CH1
   A SEC/DIV.....10 µs
   DISPLAY SIGNAL.....STORE
2. STORE A 5-DIVISION, 50 kHz SINE-WAVE SIGNAL IN THE 336 VIEW MEMORY.
3. SELECT VIEW DISPLAY MODE.
4. SELECT CHART OUT MENU.
5. SET TEST OSCILLOSCOPE TO X-Y MODE AND CONNECT THE CH1 INPUT TO X OUT AND CH2 INPUT TO Y OUT.
6. CALIBRATE THE X AND Y GAIN OF THE TEST SCOPE USING MENU BUTTON 3.
7. PRESS MENU BUTTON 1 TO START THE X-Y OUTPUT. (NOTE: THIS WAVEFORM IS TRACED OUT SLOWLY ON THE DISPLAY.)



4421-76

WAVEFORMS

TYPE	+5V11	+5V12	+5VD8	⏚
ICL8212			8	5
40H365	16		7	
40H175			16	7
TC555P		1,28		14
75160			20	10
75161			20	10

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
(Assembly Number — Subassembly Number (if used) — Schematic Circuit Number)

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices See Maintenance Section

NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)

A8 PARTIAL OPTION BOARD

4421-64

EXTENDED MEMORY, BATTERY BACKUP & GPIB (OPTION 01) 16

UNBLANKING LOGIC & CHART OUT 17

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
MA	2J	2F	P922	2M	2A	P942	2H	3A	R906	1P	2F
MA	3J	2F	P932	2P	3A	P942	3K	3A	R920	2P	5H
			P940	1H	3G	P942	3M	3A	R921	2M	6H
MF	2P	4A	P940	3H	3G	P942	3P	3A	R922	2M	6H
			P940	3L	3G	P952	2H	4A	R923	2P	6H
P222	2L	7F	P940	3P	3G	P960	2S	4G	R924	2M	5H
P922	2K	2A	P940	3S	3G				R925	2P	5G

Partial A1 also shown on diagrams 1, 2, 3, 4, 5, 6, 7, 9, 11, 12, 13, 15, 18 and 19.

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C120	1E	1A	J942	3K	3A	R430	4P	3E	U160B	2G	1B
C140	3E	2A	J942	3M	3A	R432	4L	1E	U180	6E	2C
C428	3P	1D	J942	3P	3A	R433	4K	2C	U220A	4G	3F
C431	4K	2C				R440	5P	1E	U400	9G	3B
C432	4L	1E	P420	3S	1D	R442	6P	1D	U402A	4F	3D
			P830	10M	1C	R444	6P	1E	U402B	2J	3D
CR120	1E	1A	P830	1A	1C	R446	4N	1E	U402C	7L	3D
CR122	2G	2H	P830	9A	1C	R450	3S	1E	U410	9H	3B
CR124	2G	2G				R470	6P	1E	U420	9K	3C
CR142	3G	2G	R100A	9F	1C	R472	7P	1E	U430	3L	2C
CR144	3G	2G	R100B	5C	1C	R474	7P	1E	U440	4N	2C
CR430	4P	2D	R100C	2B	1C	R480	3L	3E	U442A	4P	2D
CR440	6S	1E	R100D	2B	1C	R484	4G	3G	U442B	4P	2D
CR442	7S	1E	R100E	2B	1C	R486	4G	2G	U442C	5S	2D
CR444	7S	1E	R100F	10N	1C	R490	7E	1E	U442D	3M	2D
CR446	6S	1E	R100G	8G	1C	R492	9S	3E	U442E	7F	2D
CR448	5S	1D	R100H	1B	1C	R494	9S	3E	U450	7L	3E
CR450	5S	1D	R120	2G	3G	R496	9S	3F	U470A	7P	2D
			R122	2F	1A				U470B	7P	2D
J940	2H	3G	R124	3F	1B	RT432	4M	2D	U470C	6P	2D
J940	3H	3G	R126	2F	1B	RT440	4S	2D	U472A	7N	3E
J940	3L	3G	R128	2F	1B				U472B	8N	3E
J940	3P	3G	R130	3G	1B	U100	2E	2B	U472C	7N	3E
J940	3S	3G	R132	3G	3G	U110A	5C	2C	U480	10P	3D
J940	5K	3G	R136	2F	1B	U110B	9E	2C	U490	8M	3C
J940	8A	3G	R410	3N	2B	U120B	4F	2F			
J940	9S	3G	R412	10N	1D	U140	4E	3A			
J942	2H	3A	R420	8L	3C	U160A	2E	1B			

Partial A4 also shown on diagram 11.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J100	2J	CHASSIS	J102	3J	CHASSIS	J104	3J	CHASSIS	J906	1N	CHASSIS

WAVEFORMS

CHART OUT

A1 PARTIAL MAIN BOARD

UNBLANKING LOGIC

HORIZONTAL MODE CONTROL

VERTICAL MODE CONTROL

DECODER

CONTROL LATCH

DISPLAY CLOCK

U100 ITS80141

U160A M5218L

U160B M5218L

U120A M5218L

U120B M5218L

U140 ADT524

U402A 40H010

U220A CD4053

U110A 74LS139

U180 40H259

U442E CA3046

U402B 40H010

U110B 74LS139

U400 40H393

U410 40H158

U430 40H158

U442D CA3046

U440 40H158

U442A CA3046

U442C CA3046

U402C 40H010

U450 40H153

U472C 74LS10

U472A 74LS10

U472B 74LS10

U470C 74LS10

U470A 74LS10

U470B 74LS10

U490 40H175

U420 74LS170

U480 40H158

TYPE	+8V$_S$	+5V$_S$	+5V$_{DI}$	/\	▽	-5V$_S$
CD4053		16		8|6		7
AD7524		14		3		
74LS139			16		8	
40H393			14		7	
40H175			16		8	
74LS170			16		8	
40H158		16	16	8	8	
40H153		16		8		
74LS10		14		7		
40H010		14		7		
40H259			16		8	

NOTE: ↑U410

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
(Assembly Number · Subassembly Number (if used) · Schematic Circuit Number)

Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices — See Maintenance Section

NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)

A4 PARTIAL CONTROL BOARD

4421-65

336

UNBLANKING LOGIC & CHART OUT ◇17

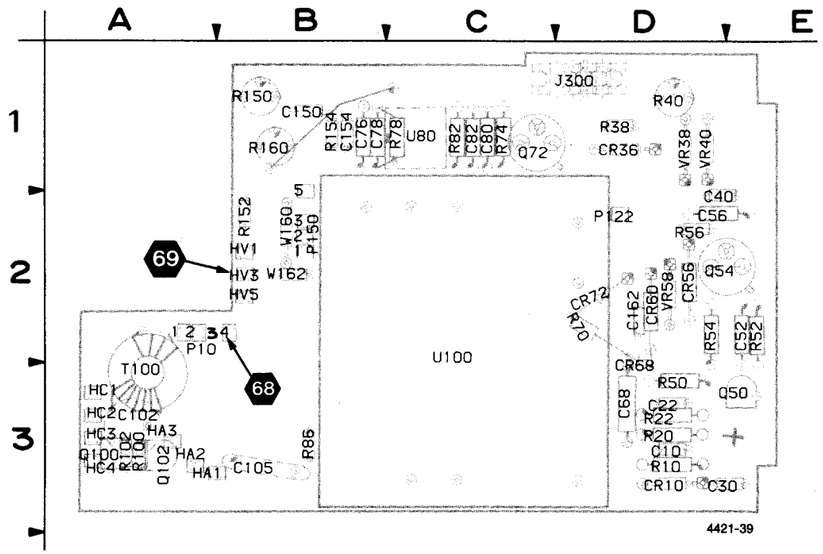
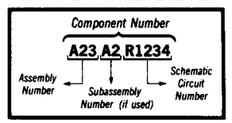


Figure 9-17. A15—High Voltage board.

A15—PRIMARY BOARD

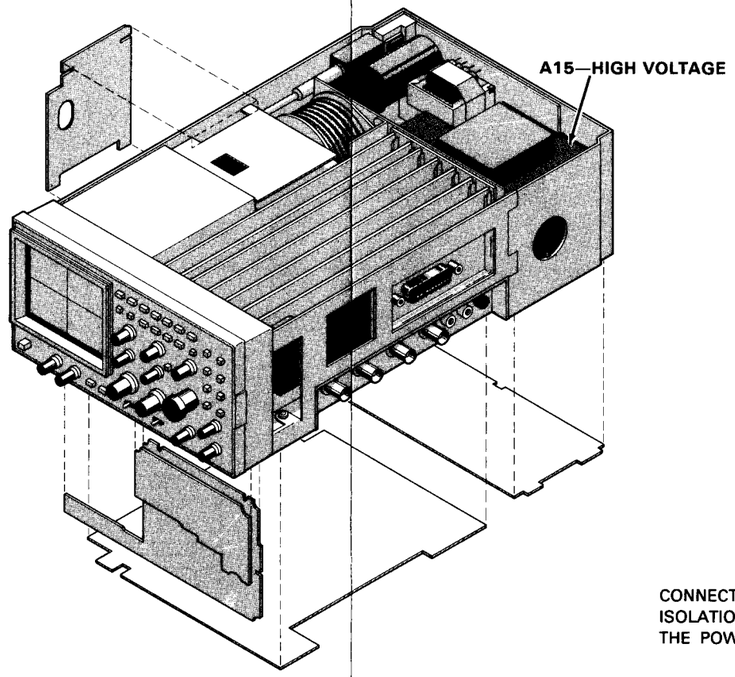
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C10	18	P10	18
C22	18	P122	18
C30	18	P150	18
C40	18	Q50	18
C52	18	Q54	18
C56	18	Q72	18
C68	18	Q100	18
C76	18	Q102	18
C78	18	R10	18
C80	18	R20	18
C82	18	R22	18
C102	18	R38	18
C105	18	R40	18
C150	18	R50	18
C154	18	R52	18
		R54	18
C162	18	R56	18
CR10	18	R70	18
CR36	18	R74	18
CR56	18	R78	18
CR60	18	R82	18
CR68	18	R86	18
		R100	18
CR72	18	R102	18
HA1	11	R150	18
HA2	11	R152	18
HA3	18	R154	18
HC1	18	R160	18
HC2	18	T100	18
HC3	18	U80	18
HC4	18	U100	18
HV1	18	VR38	18
HV3	18	VR40	18
HV5	18	VR58	18
J300	18	W160	18
P10	18	W162	18

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

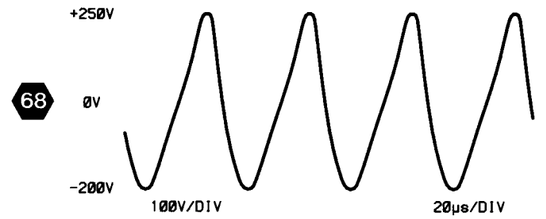
Static Sensitive Devices
See Maintenance Section



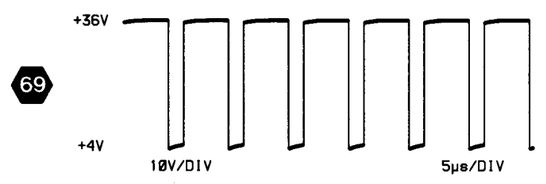
SEE TEST WAVEFORM SETUP ADJACENT TO DIAGRAM 1

WAVEFORMS FOR DIAGRAM 18

SEE FIGURE 9-8 A1 MAIN BOARD FOR LOCATION OF TEST POINT FOR WAVEFORM 67.



CHANGES TO 336 CONTROL SETTINGS:
HORIZONTAL
DISPLAY MODE .....A
A SEC/DIV.....0.5 µs



4421-77

WARNING

CONNECT THE AC SOURCE VOLTAGE TO THE 336 VIA AN ISOLATION TRANSFORMER WHENEVER TROUBLESHOOTING THE POWER SUPPLY.

Z-AXIS AMPL, CALIBRATOR, HIGH VOLTAGE AND CRT

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C901	4C	5A	ME	4B	5A	R982	2B	2B	R994	2D	1A
C980	1C	1A				R984	1C	1A			
C982	2B	1B	P922	4C	2A	R986	1C	1A	U980	2B	2B
			P926	2P	6G	R988	1C	1A			
MA	2D	2F				R990	1D	1A			
MA9	1B	1B	R926	2P	6H	R992	2D	1A			

Partial A1 also shown on diagrams 1, 2, 3, 4, 5, 6, 7, 9, 11, 12, 13, 15, 17 and 19.

ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C160	4D	1B	J222	4D	3B	P100	4D	1B			

Partial A11 also shown on diagram 6.

ASSEMBLY A12

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C510	6D	1A	CR606	7D	2C	Q600	7A	3C	R608	8C	2C
C602	7A	3C	CR608	7A	3C	Q620	7C	3C	R610	7A	3C
C614	7C	3C				Q640	7D	2C	R614	7C	3C
C640	6C	2C	HC	5B	3C	Q660	6C	2C	R618	6C	2C
C660	6C	1C							R620	6C	2C
			J100	4D	1B	R600	6A	3C	R622	6C	1C
CR600	7A	3C				R602	7A	3C	R624	6D	1C
CR602	6A	3C	P100	4E	1C	R604	6A	3C			
CR604	7A	3C				R606	7A	3C			

Partial A12 also shown on diagram 11.

ASSEMBLY A15

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C10	7F	3D	CR60	4H	2D	P150	4P	2B	R86	9F	3B
C22	6H	3D	CR68	8G	3D				R100	9L	3A
C30	6G	3D	CR70	8F	3B	Q50	4F	3D	R102	9L	3A
C40	7G	2D	CR72	8G	2D	Q54	4G	2D	R150	7P	1B
C52	4F	2E				Q72	9H	1C	R152	5P	2B
C56	4G	2D	HA3	8M	3A	Q100	9L	3A	R154	5P	1B
C68	8G	3D				Q102	9L	3A	R160	4S	1B
C76	9J	1B	HC1	5B	3A						
C78	9J	1B	HC2	5B	3A	R10	7F	3D	T100	9L	3A
C80	10J	1C	HC3	8M	3A	R20	7H	3D			
C82	9K	1C	HC4	8M	3A	R22	6H	3D	U80	9J	1C
C102	9L	3A				R38	7F	1D	U100	4K	3C
C105	9K	3B	HV1	2B	2B	R40	7F	1D			
C150	7P	1B	HV3	2B	2B	R50	4F	3D	VR38	7G	1D
C154	5P	1B	HV5	2B	2B	R52	4F	2E	VR40	7F	1D
C160	8F	1B				R54	4F	2D	VR58	4H	2D
C162	4P	2D	J300	2F	1D	R56	4G	2D			
						R70	8G	2D	W160	4P	2B
CR10	7F	3D	P10	8E	2A	R74	9J	1C	W162	4P	2B
CR36	7G	1D	P10	9L	2A	R78	9J	1C			
CR56	4G	2D	P122	8E	2D	R82	9K	1C			

Partial A15 also shown on diagram 11.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
L100	3M	CHASSIS	U120	3K	CHASSIS	V100	3	CHASSIS			

SEE TEST WAVEFORM SETUP ADJACENT TO DIAGRAM 1

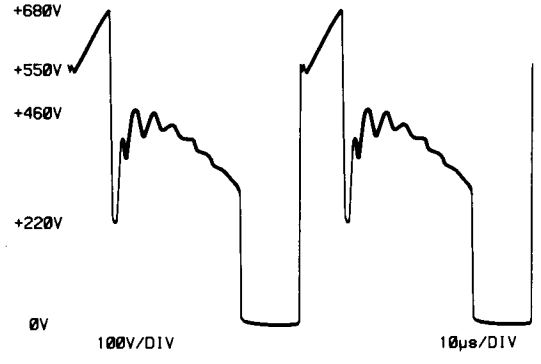
WAVEFORMS FOR DIAGRAM 19

WARNING

CONNECT THE AC SOURCE VOLTAGE TO THE 336 VIA AN ISOLATION TRANSFORMER WHENEVER TROUBLESHOOTING THE POWER SUPPLY.

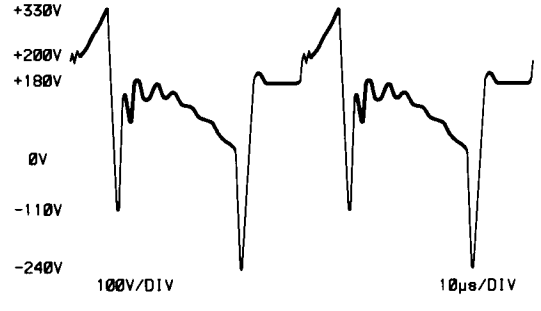
THE OPTIONAL POWER SUPPLY LOAD MODULE IS USEFUL FOR TROUBLESHOOTING THE POWER SUPPLY WHILE THE SUPPLY IS DISCONNECTED FROM THE MAIN 336 CHASSIS. WAVEFORMS ARE TYPICAL WHEN THE LOAD MODULE IS IN USE.

70

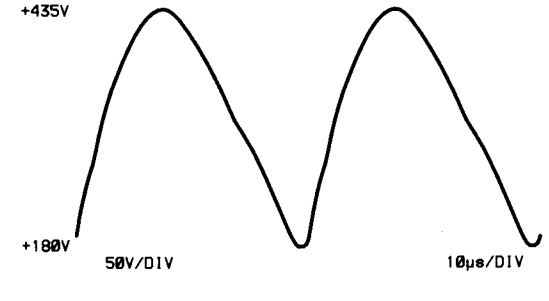


TRIGGER THE TEST OSCILLOSCOPE EXTERNALLY ON WAVEFORM 70 FOR WAVEFORMS 71 THROUGH 82.

71

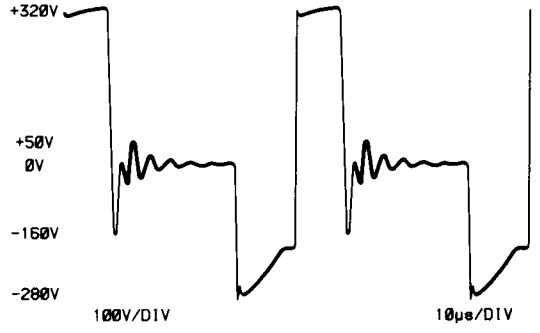


72

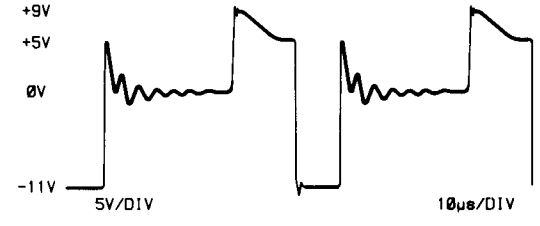


USE OF THE EXTENDER CIRCUIT BOARDS AND CABLES SUPPLIED IN THE SERVICE MAINTENANCE KIT PROVIDES EASE OF ACCESS TO THE WAVEFORM TEST POINTS.

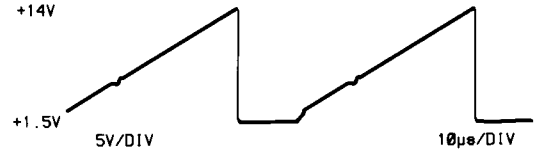
73



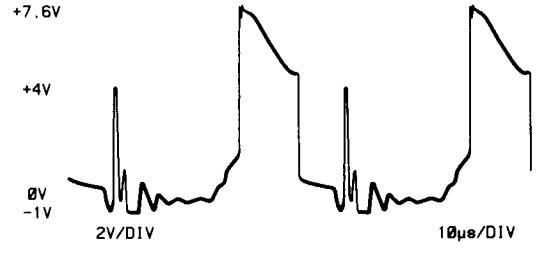
74



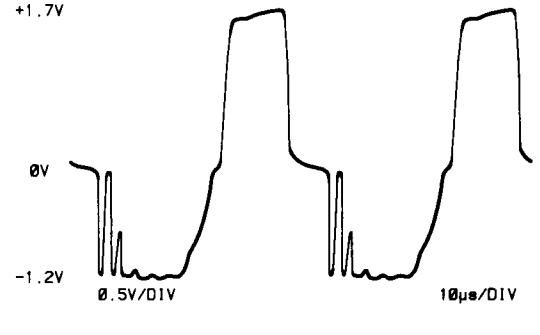
75

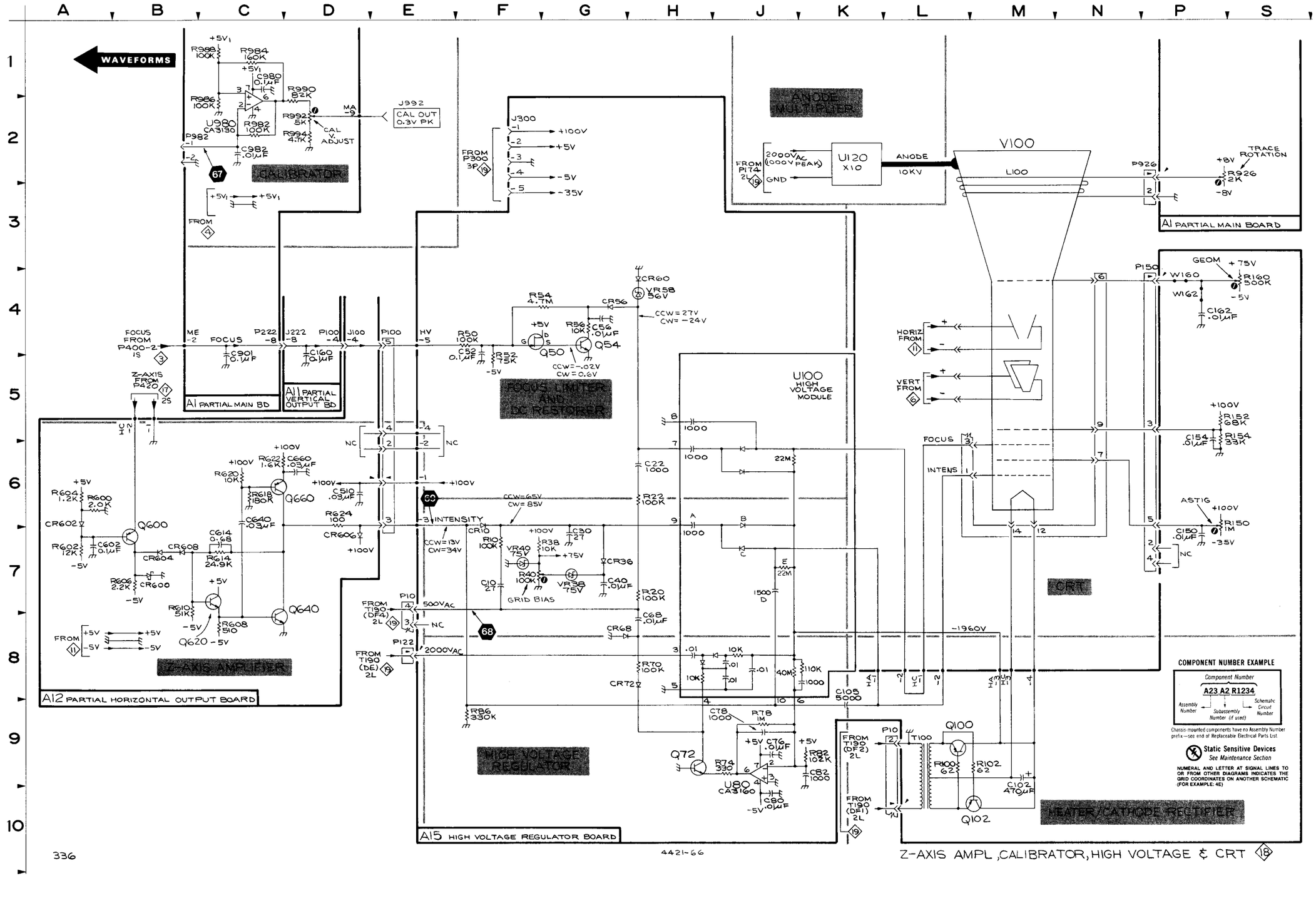


76



77




WAVEFORMS
CALIBRATOR
ANODE MULTIPLIER
U120 X10
2000VAC (1000V PEAK)
ANODE 10KV
V100
L100
TRACE ROTATION
R926 2K
A1 PARTIAL MAIN BOARD
GEOM +75V
R160 500K
W160
W162
C162 .01μF
-5V
P150
+100V
R152 68K
C154 .01μF
R154 33K
ASTIG +100V
R150 1M
C150 .01μF -35V
NC
CRT
FOCUS
INTENS
HORIZ FROM 11
VERT FROM 9
-1960V
FROM P300 3P 19
+100V
+5V
-5V
-35V
FROM P174 2L 19
GND
FROM 4
+5V1
R988 100K
R984 60K
C980 0.1μF
R986 100K
R990 82K
U980 CA3130
R992 5K
CAL V ADJUST
R994 4.7K
MA -9
J992
CAL OUT 0.3V PK
P982
C982 .01μF
67
R54 4.7M
CR60
VR58 56V
CR56
CCW=27V
CW=-24V
R56 10K
C56 .01μF
Q50
Q54
CCW=-.02V
CW=0.6V
R50 100K
C58 0.1μF
R52 75K
FOCUS LIMITER AND DC RESTORER
FOCUS FROM P400-2 15 3
ME -2
FOCUS C90 0.1μF
P222 -8
J222 -8
C160 0.1μF
P100 -4
J100 -4
P100 -5
HV -5
Z-AXIS FROM P420 17 25
A1 PARTIAL MAIN BD
A1 PARTIAL VERTICAL OUTPUT BD
U100 HIGH VOLTAGE MODULE
1000
22M
C22 1000
R22 100K
1500 D
E 22M
R20 100K
C68 .01μF
CR68
CR72
R70 100K
.01
10K
40M
110K
1000
C105 5000
R86 330K
C78 1000
R78 1M
Q72
R74 330
U80 CA3160
C76 .01μF
C80 .01μF
R82 102K
C82 1000
HIGH VOLTAGE REGULATOR
A15 HIGH VOLTAGE REGULATOR BOARD
FROM T190 (DF2) 2L 19
FROM T190 (DF1) 2L 19
P10
T100
Q100
Q102
R100 62
R102 62
C102 470μF
HEATER/CATHODE RECTIFIER
+100V
R622 1.6K
C660 .03μF
R620 10K
R618 180K
Q660
C510 .03μF
C640 .03μF
R624 100
CR602
Q600
R602 12K
C602 0.1μF
CR604
CR608
C614 0.68
R614 24.9K
R606 2.2K
CR600
R610 51K
Q640
R608 510
Q620
+5V
R694 1.2K
R600 2.0K
-5V
FROM 11
CR606
60
CCW=65V
CW=85V
INTENSITY
CR10
CCW=13V
CW=34V
R10 100K
VR40 75V
R38 10K
+75V
VR38 75V
C30 27
CR36
R40 100K
GRID BIAS
C10 27
C40 .01μF
68
P10 4
500VAC
NC
FROM T190 (DF4) 2L 19
P122
2000VAC
FROM T190 (DE) 2L 19
Z-AXIS AMPLIFIER
A12 PARTIAL HORIZONTAL OUTPUT BOARD
COMPONENT NUMBER EXAMPLE
Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number
Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.
Static Sensitive Devices
See Maintenance Section
NUMERAL AND LETTER AT SIGNAL LINES TO OR FROM OTHER DIAGRAMS INDICATES THE GRID COORDINATES ON ANOTHER SCHEMATIC (FOR EXAMPLE: 4E)

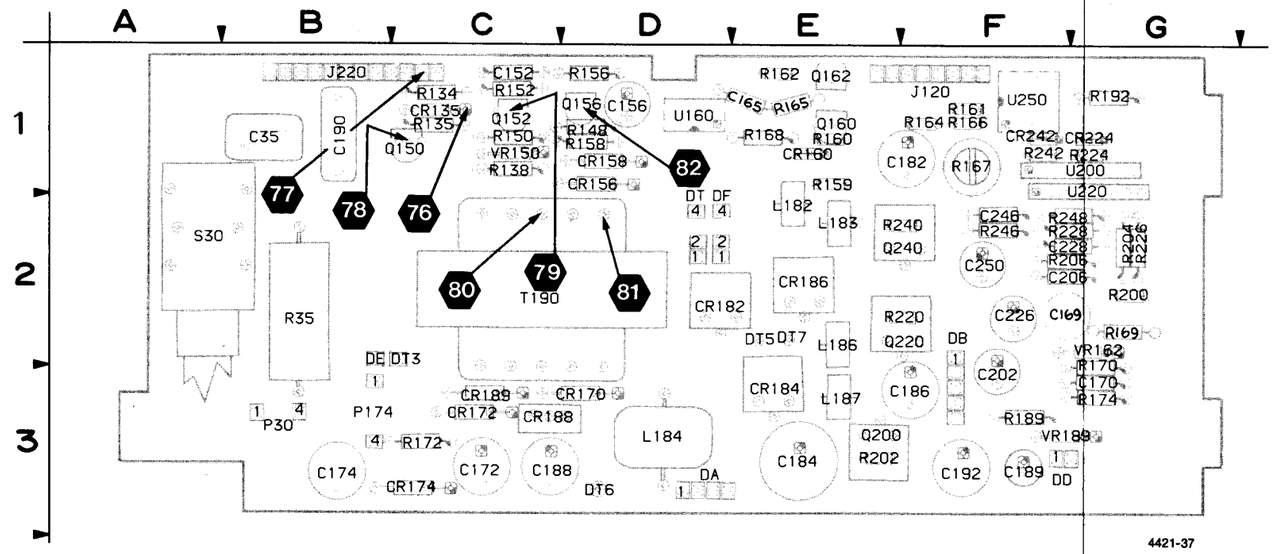
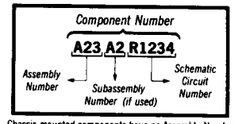


Figure 9-18. A13—DC/DC Converter board.

A13—DC/DC CONVERTER BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C35	19	CR184	19	L184	19	R169	19
C152	19	CR184	19	L186	19	R170	19
C156	19	CR186	19	L187	19	R172	19
C165	19	CR186	19	P30	19	R174	19
C169	19	CR188	19	P174	19	R189	19
C170	19	CR188	19	Q150	19	R192	19
C172	19	CR189	19	Q152	19	R200	19
C174	19	CR224	19	Q156	19	R202	19
C182	19	CR242	19	Q160	19	R204	19
C184	19	DA	19	Q162	19	R206	19
C186	19	DB	19	Q200	19	R220	19
C188	19	DB	19	Q220	19	R224	19
C189	19	DB	19	Q240	19	R226	19
C190	19	DD	19	R35	19	R228	19
C192	19	DD	19	R134	19	R240	19
C202	19	DE	19	R135	19	R242	19
		DF	19	R138	19	R246	19
C206	19	DF	19	R148	19	R248	19
C226	19	DT	19	R150	19	S30	19
C228	19	DT3	19	R152	19	T190	19
C246	19	DT5	19	R156	19	U160	19
C250	19	DT6	19	R158	19	U200	19
CR135	19	DT7	19	R159	19	U220	19
CR156	19	J120	19	R160	19	U220	19
CR158	19	J120	19	R161	19	U250	19
CR160	19	J120	19	R162	19	VR150	19
CR170	19	J220	19	R164	19	VR162	19
CR172	19	J220	19	R165	19	VR189	19
CR174	19	J220	19	R166	19		
CR182	19	L182	19	R167	19		
CR182	19	L183	19	R168	19		

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Static Sensitive Devices
See Maintenance Section

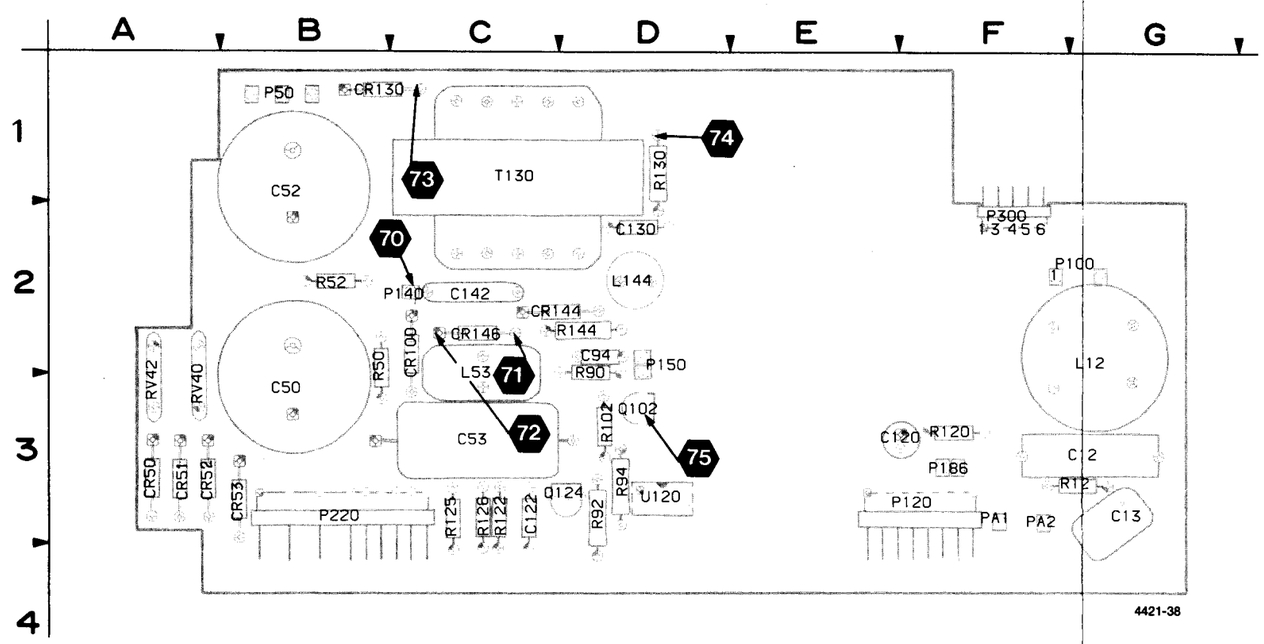
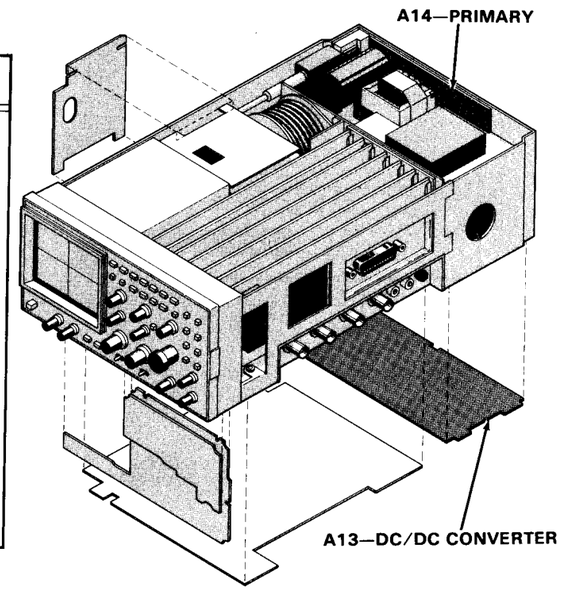


Figure 9-19. A14—Primary board.

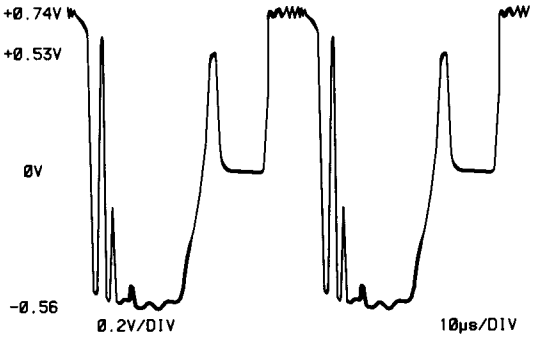
A14—PRIMARY BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C12	19	P150	19
C13	19	P186	19
C50	19	P220	19
C52	19	P220	19
C53	19	P220	19
C94	19	P300	19
C120	19	PA	19
C122	19	Q102	19
C130	19	Q124	19
CR50	19	R12	19
CR51	19	R50	19
CR52	19	R52	19
CR53	19	R90	19
CR100	19	R92	19
CR130	19	R94	19
CR144	19	R102	19
CR146	19	R120	19
L12	19	R122	19
L53	19	R125	19
L144	19	R126	19
P50	19	R130	19
P100	19	R144	19
P120	19	RV40	19
P120	19	RV42	19
P120	19	T130	19
P140	19	U120	19

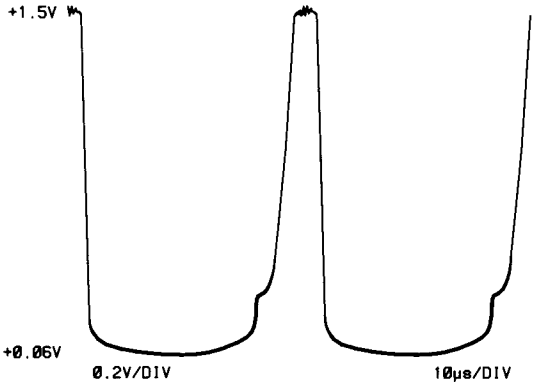


WAVEFORMS FOR DIAGRAM 19 (CONT)

78

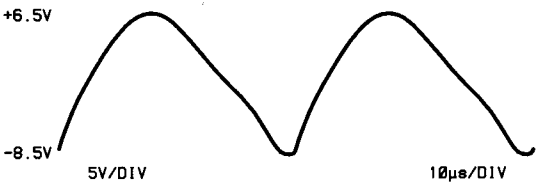


79

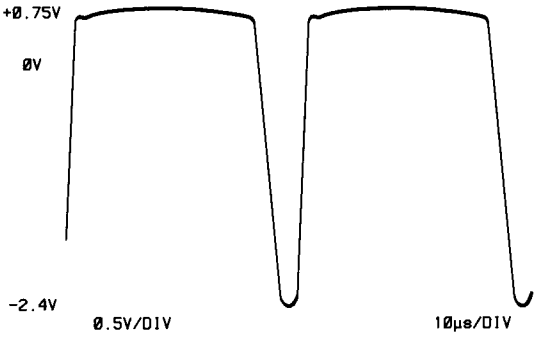


80

81



82



4421-78

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P50	4P	5G	P50	7P	5G	P56	6P	5G			

Partial A1 also shown on diagrams 1, 2, 3, 4, 5, 6, 7, 9, 11, 12, 13, 15, 17 and 18.

ASSEMBLY A13

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C35	5B	1B	CR186B	7K	2E	L183	9K	2E	R169	7F	2G
C152	8H	1C	CR188A	6K	3C	L184	8K	3D	R170	5K	2G
C156	6H	1D	CR188B	6K	3C	L186	7K	2E	R172	4K	3C
C165	8G	1E	CR189	6L	3C	L187	7K	3E	R174	3K	3G
C169	7F	2G	CR224	7N	1G				R189	6L	3F
C170	5K	3G	CR242	9N	1F	P30	6B	3B	R192	2N	1G
C172	4K	3C				P174	2L	3B	R200	5L	2G
C174	3K	3B	DA	8P	3D				R202	5L	3E
C182	9K	1F				Q150	6G	1C	R204	5K	2G
C184	8L	3E	DB	4P	2F	Q152	6H	1C	R206	5K	2F
C186	7K	3F	DB	7P	2F	Q156	7H	1D	R220	7L	2F
C188	6L	3C	DB	9P	2F	Q160	7G	1E	R224	7M	1G
C189	6L	3F				Q162	7G	1E	R226	7M	2G
C190	2N	1B	DD	6P	3F	Q200	6L	3E	R228	7M	2F
C192	2N	3F	DD	9E	3F	Q220	7L	2F	R240	9L	2F
C202	6M	2F				Q240	9L	2F	R242	9M	1F
			DE	2L	2B				R246	9M	2F
C206	5K	2F				R35	5B	2B	R248	9M	2F
C226	7N	2F	DF	1L	2D	R134	4G	1C			
C228	7L	2F	DF	2L	2D	R135	4H	1C	S30	5A	2A
C246	9M	2F				R138	5H	1C			
C250	9N	2F	DT	2J	2D	R148	6H	1D	T190	1J	2C
			DT3	2J	2C	R150	7H	1C			
CR135	4H	1C	DT5	8J	2E	R152	6H	1C	U160	8G	1D
CR156	5H	1D	DT6	9J	3D	R156	7H	1D	U200	5L	1G
CR158	4H	1D	DT7	9J	2E	R158	6H	1D	U220A	9M	1G
CR160	7F	1E				R159	7F	1E	U220B	7M	1G
CR170	5K	3D	J120	2N	1F	R160	7F	1E	U250	7L	1F
CR172	4K	3C	J120	3P	1F	R161	8F	1F			
CR174	3G	3C	J120	9E	1F	R162	8G	1E	VR150	6G	1C
CR182A	9K	2D	J220	2F	1B	R164	8G	1F	VR162	7F	2G
CR182B	9K	2D	J220	5B	1B	R165	8G	1E	VR189	6L	3F
CR184A	8K	3E	J220	6E	1B	R166	8F	1F			
CR184B	8K	3E				R167	8F	1F			
CR186A	7K	2E	L182	9K	2E	R168	8G	1E			

ASSEMBLY A14

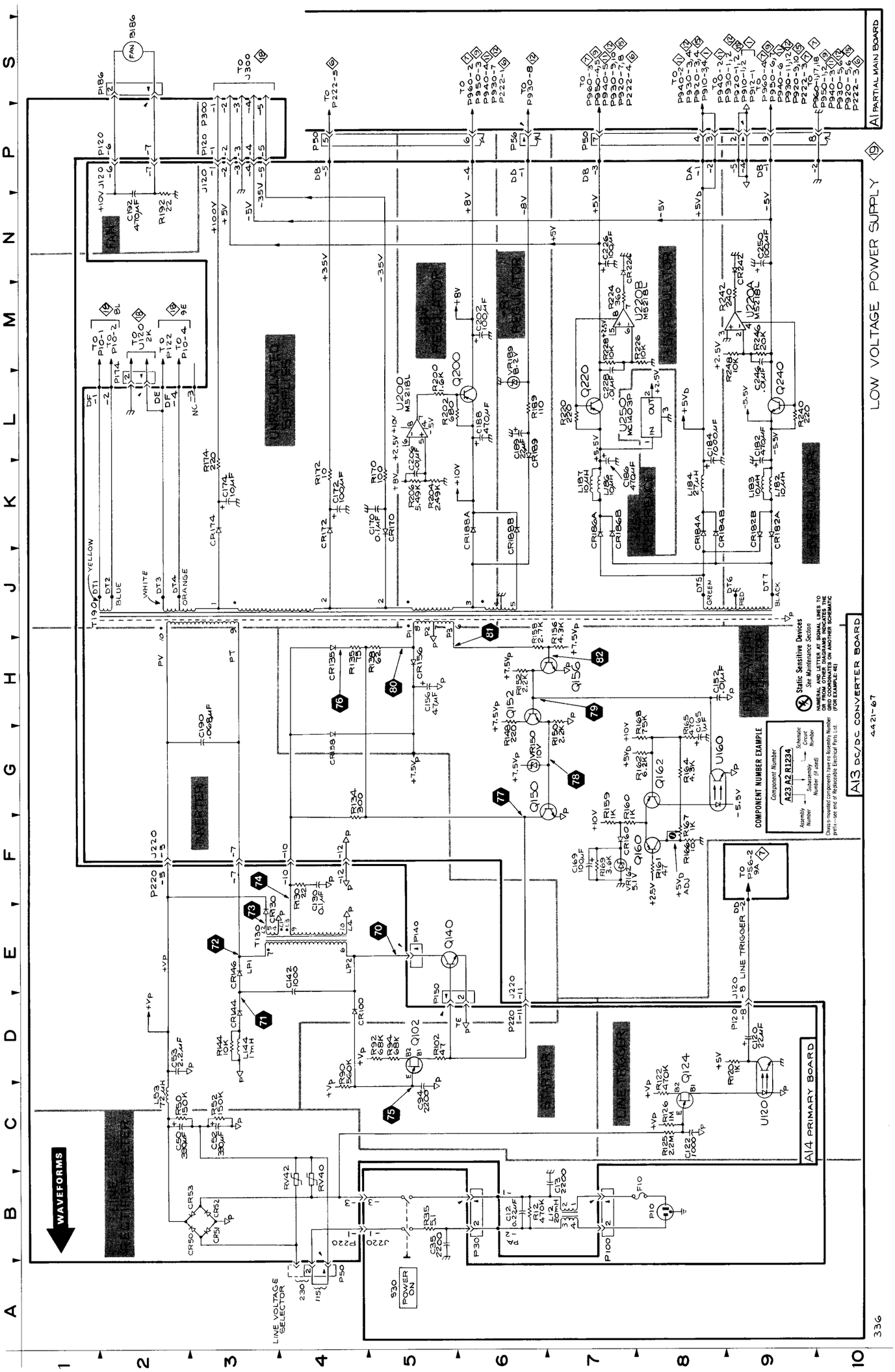
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C12	6B	3G	CR144	3D	2C	P220	4B	3B	R120	9D	3F
C13	7B	3G	CR146	3E	2C	P220	6D	3B	R122	8C	3C
C50	2C	3B				P300	3P	2F	R125	8C	3C
C52	3C	1B	L12	7B	2G				R126	8C	3C
C53	2D	3C	L53	2C	2C	PA	6B	3F	R130	4F	1D
C94	5D	2D	L144	3D	2D				R144	3D	2D
C120	9D	3E				Q102	5D	3D			
C122	8C	3C	P50	4B	2B	Q124	8C	3C	RV40	4B	3A
C130	4F	2D	P100	7B	2F				RV42	4B	3A
			P120	2P	4F	R12	6B	3F			
CR50	2B	3A	P120	3P	3E	R50	2C	2B	T130	3E	1C
CR51	3B	3A	P120	9D	3E	R52	3C	2B			
CR52	3B	3A	P140	5E	2C	R90	4D	2D	U120	9D	3D
CR53	2B	3A	P150	5D	2D	R92	5D	3D			
CR100	4D	2C	P186	2P	3F	R94	5D	3D			
CR130	3E	1B	P220	2F	3B	R102	5D	3D			

CHASSIS MOUNTED PARTS

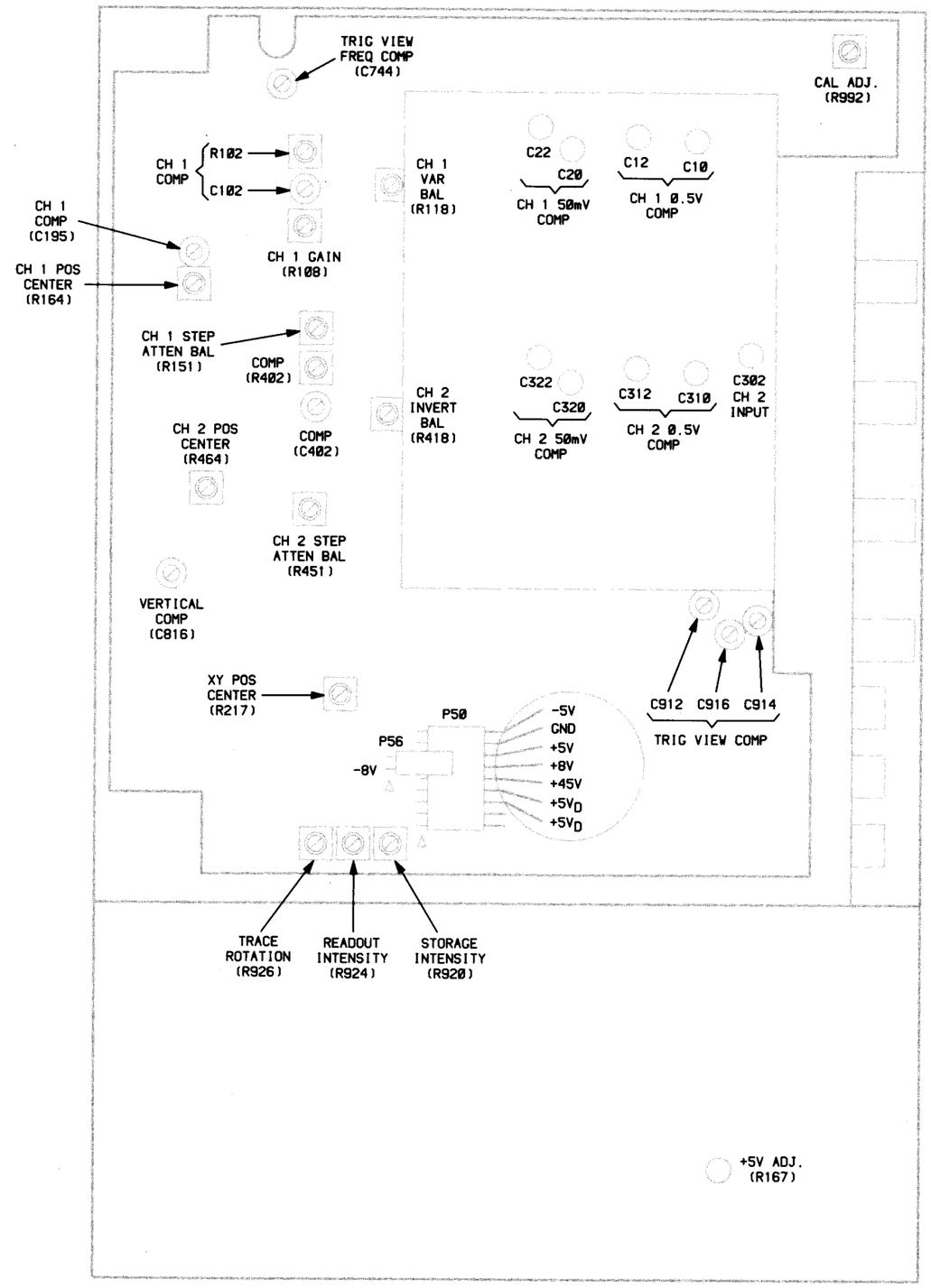
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
B186	2S	CHASSIS	F10	8B	CHASSIS	P10	8B	CHASSIS	Q140	5E	CHASSIS

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION
B186	19	2S
F10	19	8B
J1	4	2B
J100	17	2J
J102	17	3J
J104	17	3J
J108	7	2A
J301	4	9B
J906	17	1N
L100	18	3M
P10	19	8B
Q140	19	5E
U120	18	3K
V100	18	3M


LOW VOLTAGE POWER SUPPLY
A13 DC/DC CONVERTER BOARD
4421-67
A14 PRIMARY BOARD
A1 PARTIAL MAIN BOARD
WAVEFORMS
INVERTER
ENABLE
LINE TRIGGER
UNREGULATED SUPPLIES
REGULATED SUPPLIES
LINE VOLTAGE SELECTOR
POWER ON
Static Sensitive Devices
See Maintenance Section
COMPONENT NUMBER EXAMPLE
336

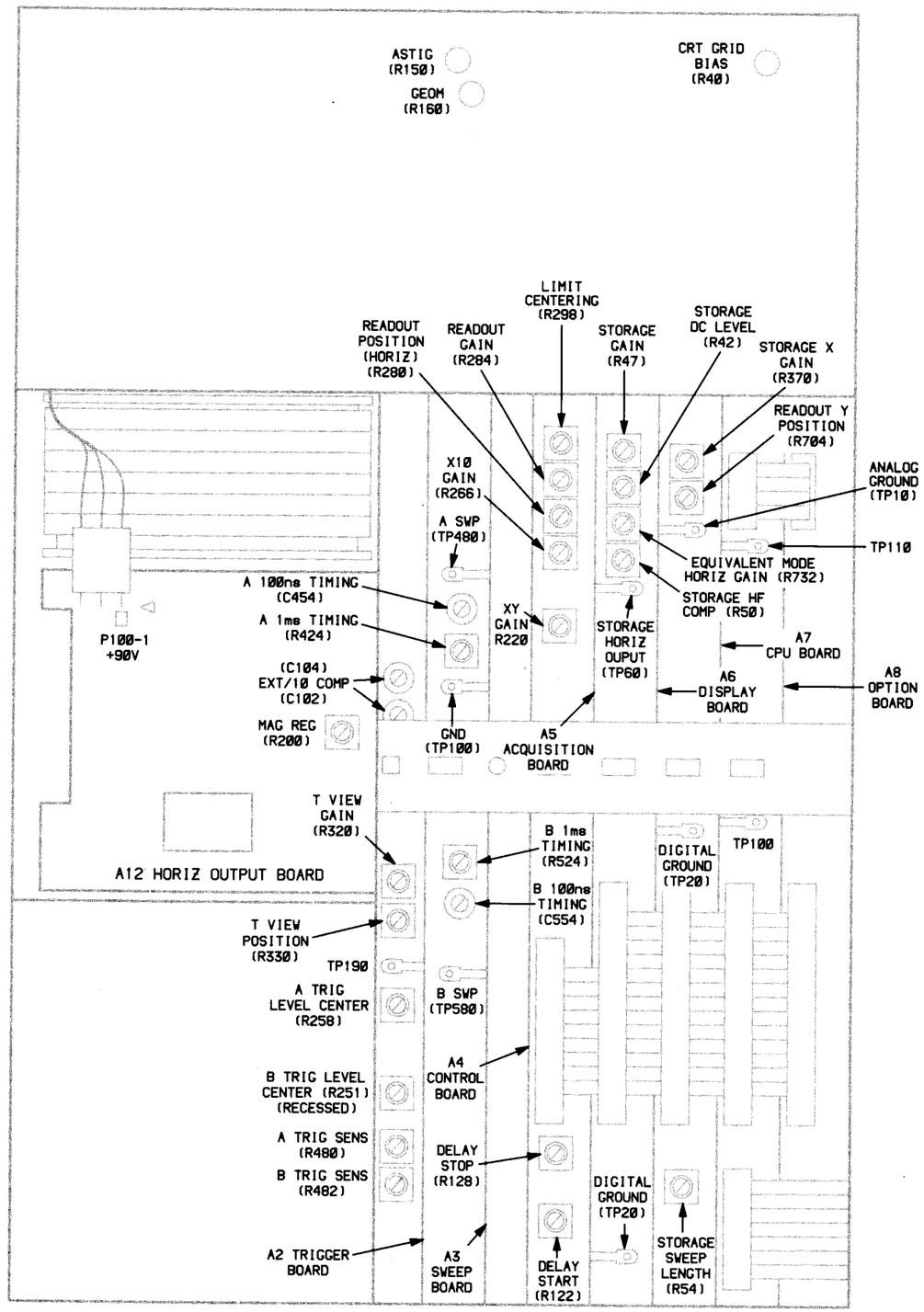
BOTTOM VIEW



REAR OF INSTRUMENT

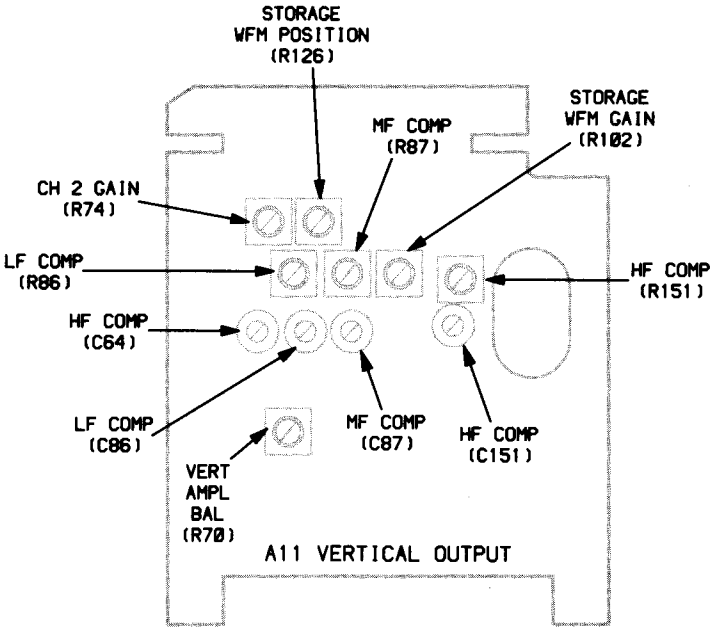
4421-83

REAR OF INSTRUMENT



TOP VIEW

4421-82


STORAGE
WFM POSITION
(R126)
MF COMP
(R87)
STORAGE
WFM GAIN
(R102)
CH 2 GAIN
(R74)
LF COMP
(R86)
HF COMP
(R151)
HF COMP
(C64)
LF COMP
(C86)
MF COMP
(C87)
HF COMP
(C151)
VERT
AMPL
BAL
(R70)
A11 VERTICAL OUTPUT

4421-81

NOTES

WARNING

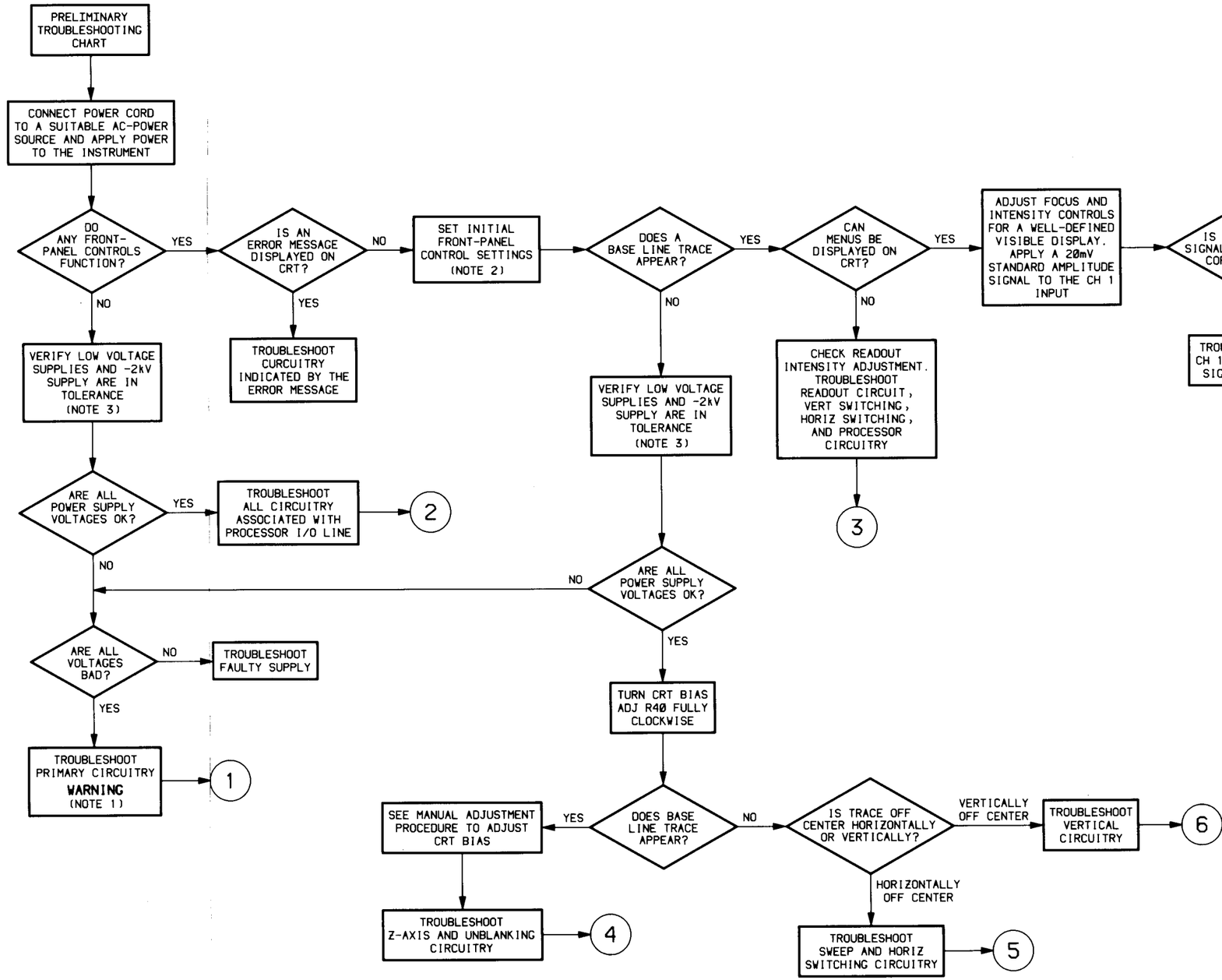
1. The PRIMARY circuit has a floating common reference with respect to chassis ground. AC power-source potential is present at the common reference points. To prevent electrical shock and possible equipment damage, connect an isolation transformer between the instrument and the ac power source before making measurements or attempting to troubleshoot the primary power supply circuitry.

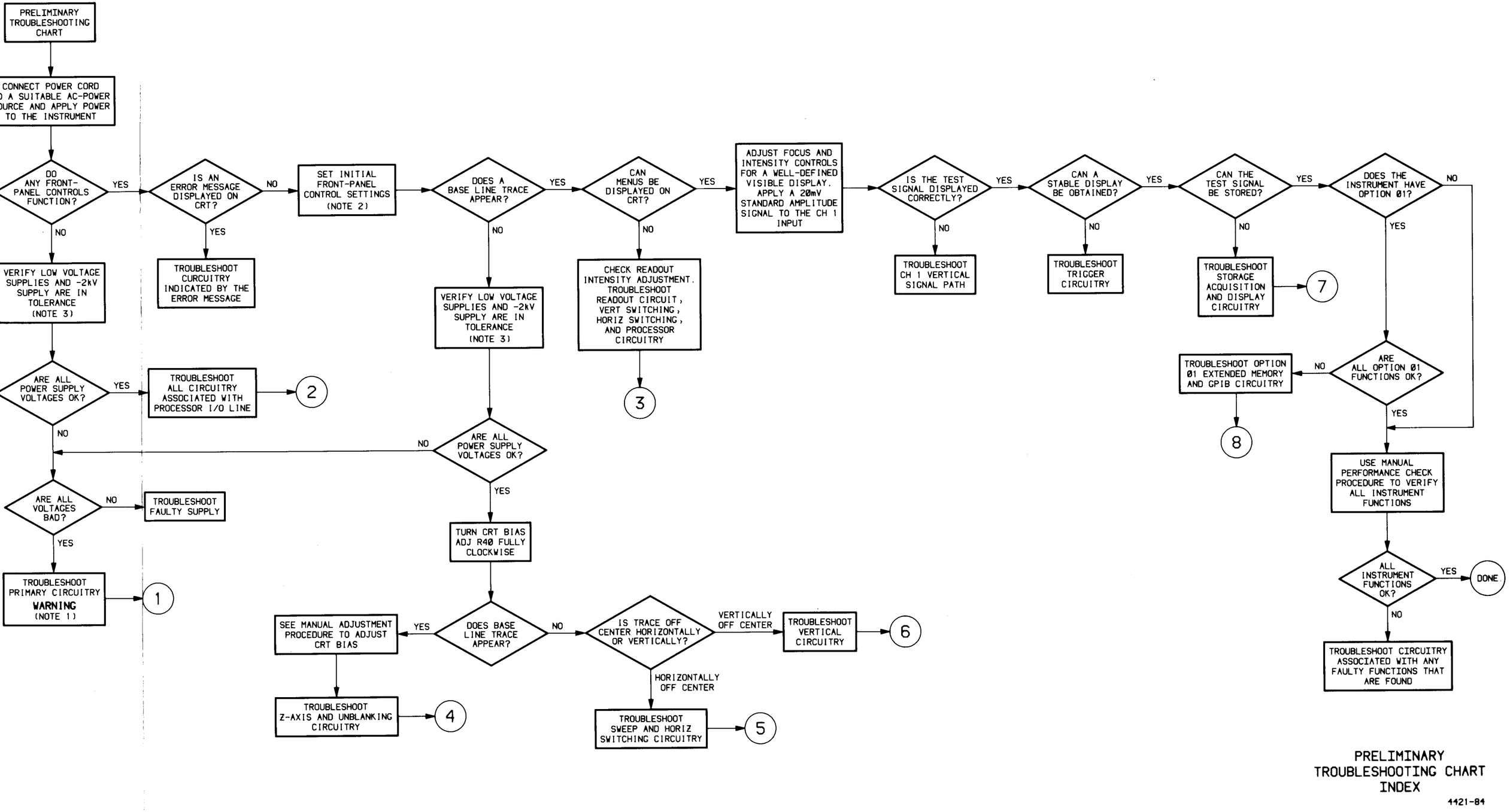
2. Control settings:

VERT MODE	CH 1
VOLTS/DIV	5mV
VOLTS/DIV VAR	CAL (in detent)
AC-GND-DC	AC
Vertical POSITION	Midrange
Trigger MODE	AUTO
Trigger SOURCE	CH 1
Trigger COUPLING	AC
SEC/DIV	0.1ms
VAR SWP/HOLDOFF	CAL/NORM (in detent)
X10 MAG	OFF
INTENSITY	Midrange
FOCUS	Midrange
Horizontal POSITION	Midrange
Horizontal Display Mode	A Sweep only (no delay)
DISPLAY MODE	NON STORE only

3. Power supply voltages and test points.

Nominal	Test Point
$+5V_D$	P50-3
+5V	P50-7
+8V	P50-6
-8V	P56-1
-5V	P50-9
-1960V	HA-3
+100V	P100-1
+45V	P50-5





PRELIMINARY TROUBLESHOOTING CHART INDEX

4421-84

NOTES

1. Power supply test setup procedure.

WARNING

To prevent electrical shock and possible equipment damage, use an isolation transformer between the 336 power supply and the ac power source. The 336 uses a switching-type supply having elevated common returns in the primary side of the supply.

With the power supply removed from the instrument, it cannot be powered for testing unless the secondary supplies are properly loaded. The optional power supply load module provides the necessary circuit loading of the secondary voltages (see Table 6-6 in Section 4 of this manual for part number).

Disconnect and remove the HV circuit board to gain ease of access to the Primary and DC to DC Convertor boards for testing. With the HV board removed, use extreme care to prevent contact with the disconnected leads to the HV board if the instrument is powered up.

2. Power supply secondary resistance to ground.

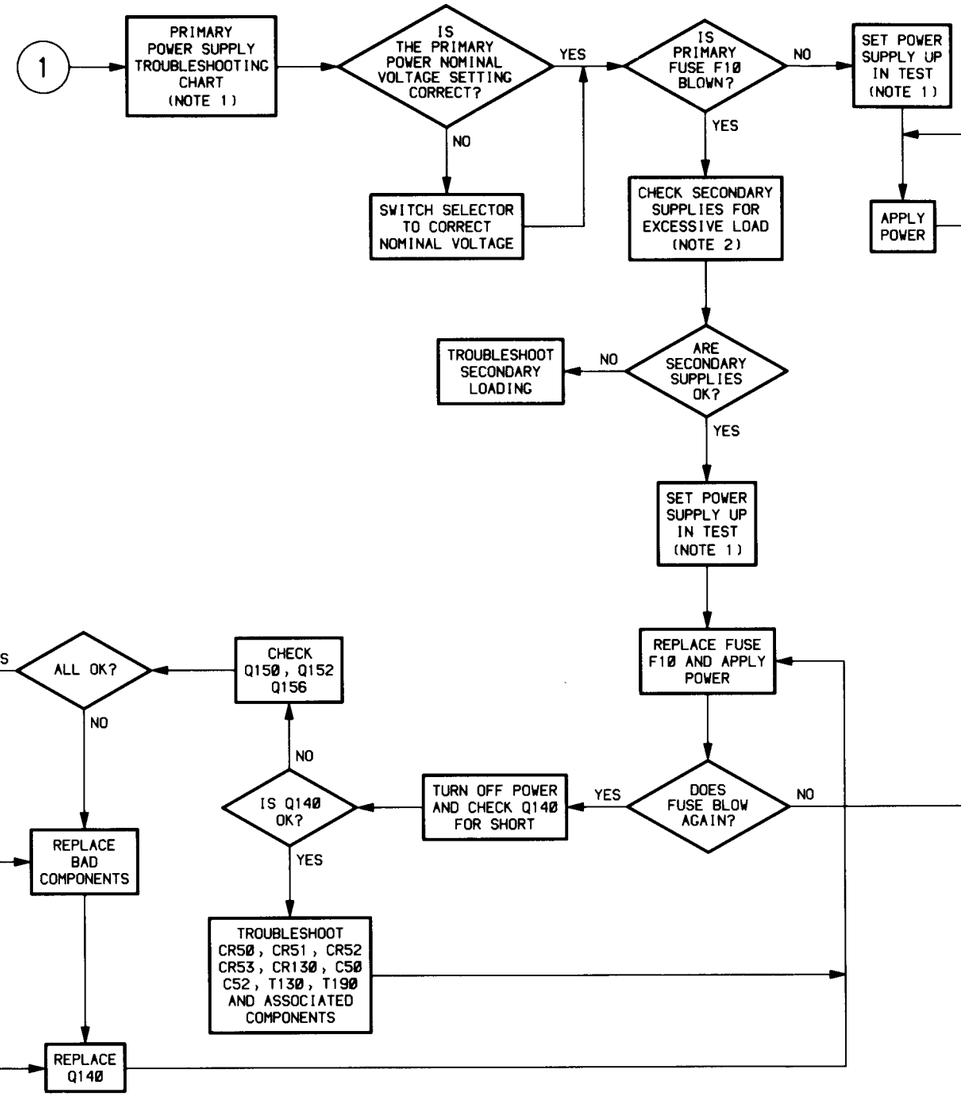
Voltage	Resistance	
	Connected To Instrument	Disconnected From Instrument
-5V	45Ω	1.2kΩ[a]
+5V	57Ω	900Ω[a]
+8V	475Ω	2kΩ[a]
+35V	HIGH	HIGH
$+5V_D$	238Ω	HIGH
-8V	615Ω	670Ω
+100V	13.5kΩ[b]	51kΩ[c]

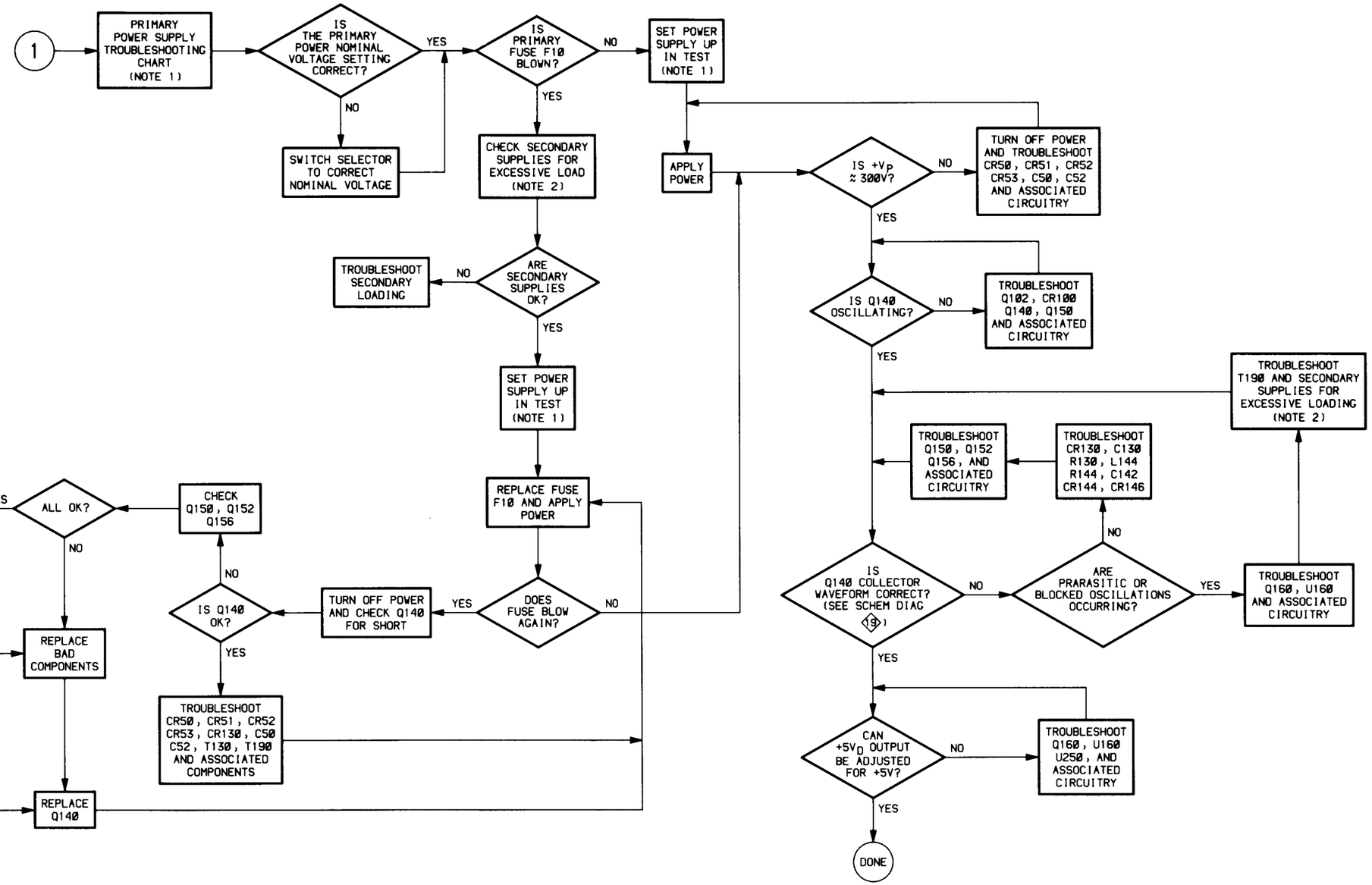
[a] After filter capacitors charge.

[b] DMM ON 20kΩ setting.

[c] DMM on 200kΩ setting.

These are typical resistance readings and they may vary from instrument to instrument by a small amount. Significant deviation from the listed values indicates a possible circuit loading problem.





1 PRIMARY POWER SUPPLY TROUBLESHOOTING

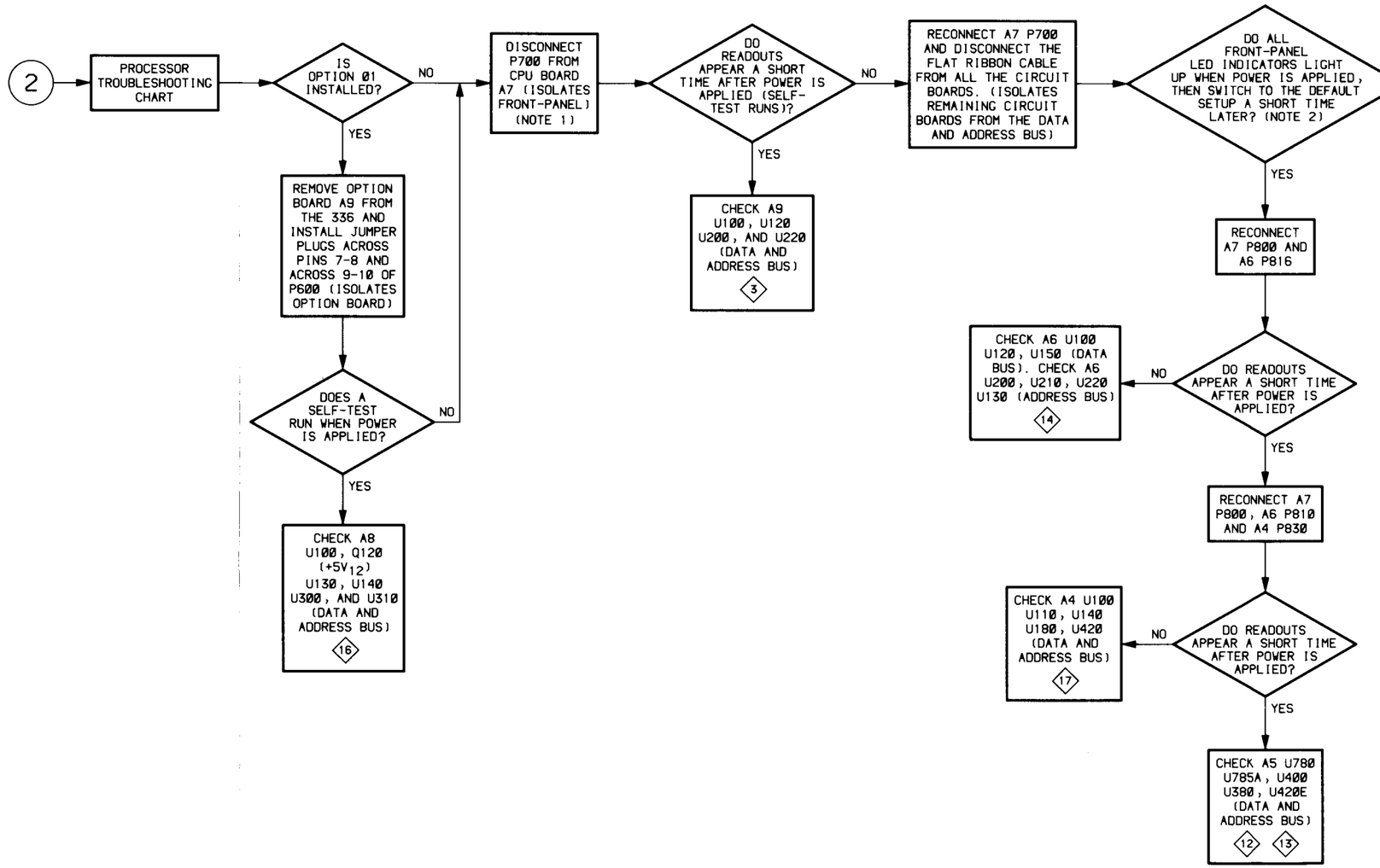
4421-85

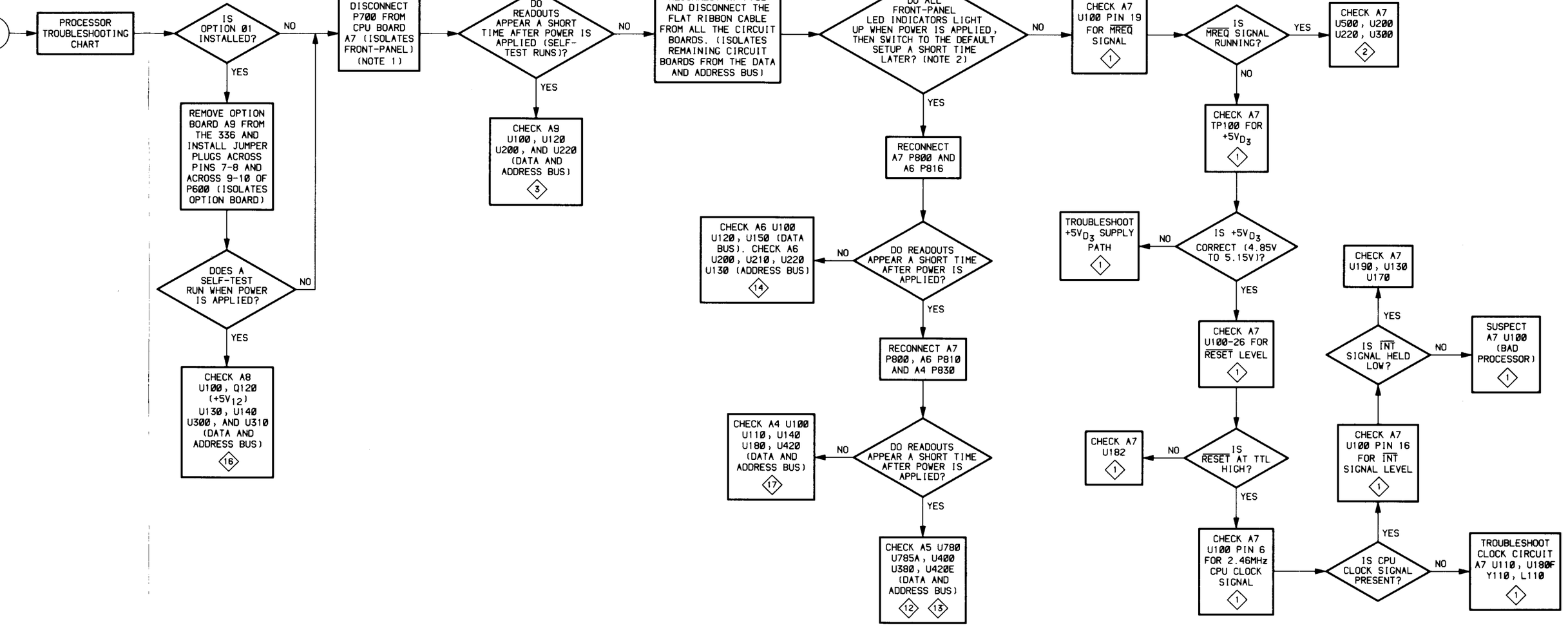
NOTES

1. Turn off power before disconnecting or reconnecting any plugs and before removing or replacing any components. See "Maintenance" section of this manual for "Static Sensitive" component handling and proper soldering techniques.

2. The default front-panel settings are:

VERT MODE	CH 1
DISPLAY MODE	NON STORE
VOLTS/DIV	50mV
SEC/DIV	2ms
TRIG MODE	AUTO
TRIG SOURCE	CH 1
TRIG COUPLING	AC



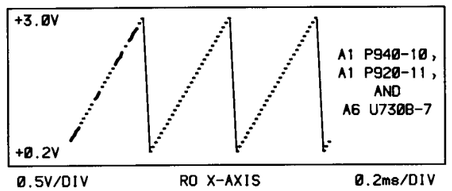


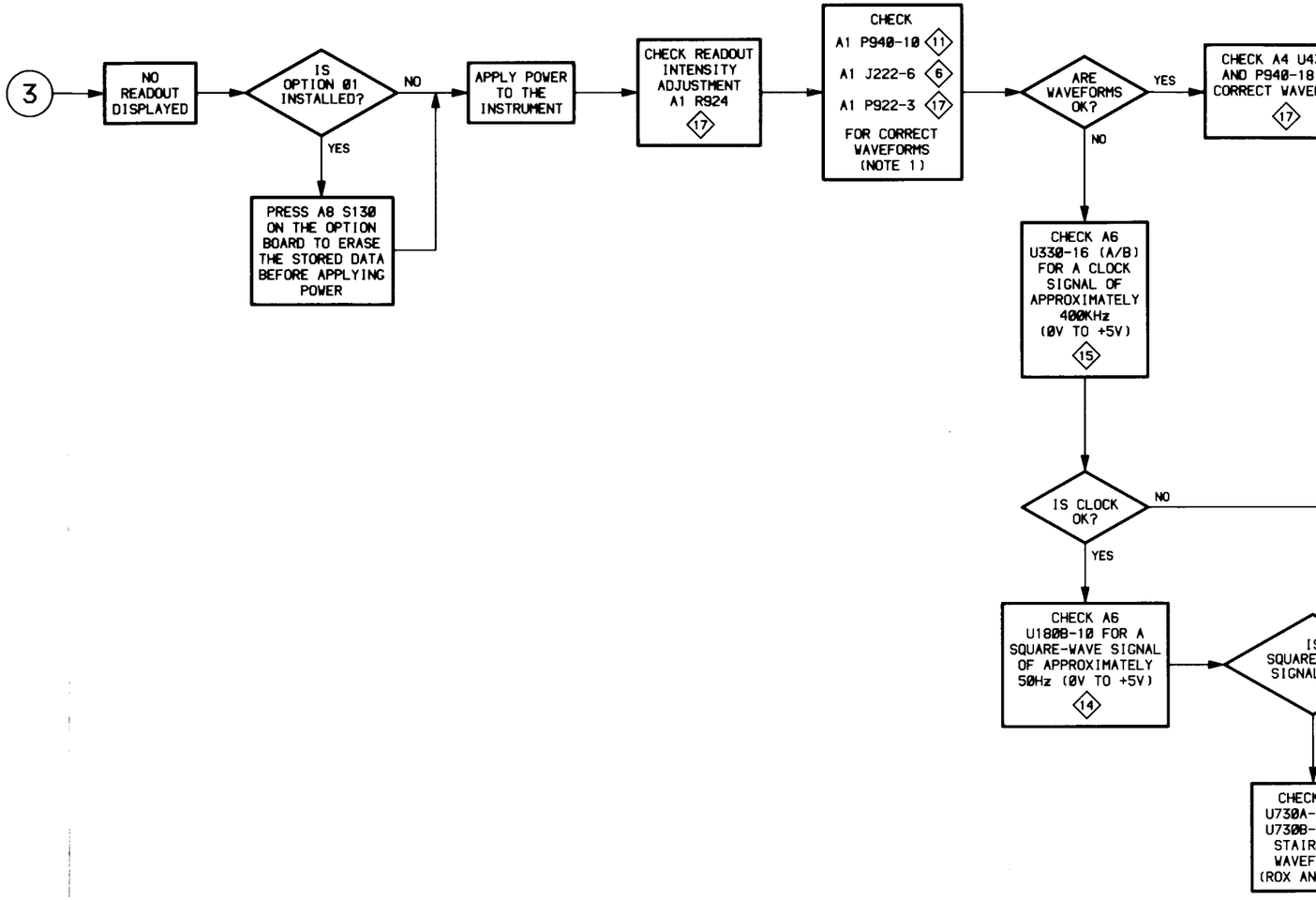
2 PROCESSOR TROUBLESHOOTING

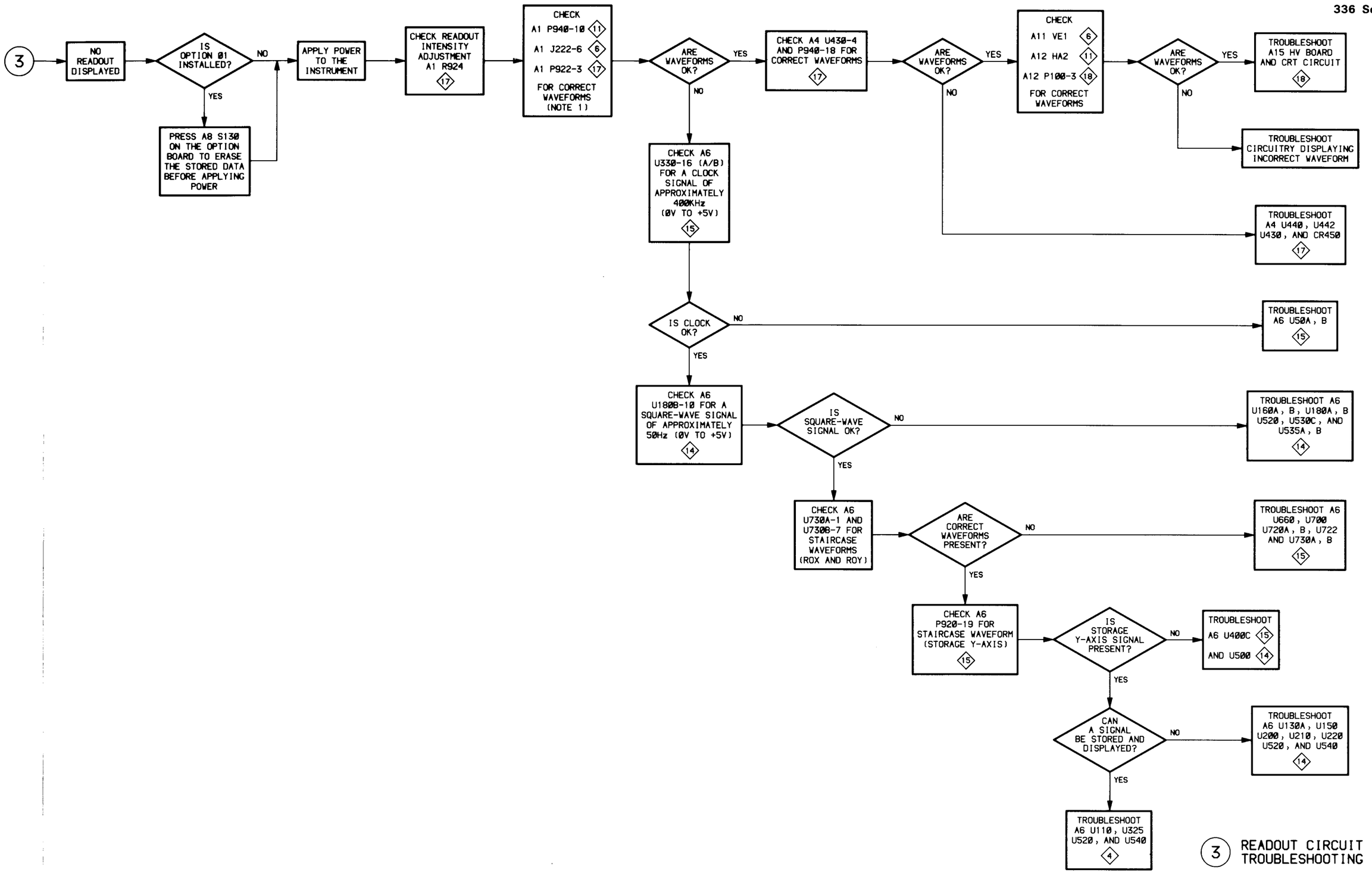
4421-86

NOTE

1. CONSIDER PLUGS, CABLES, AND CONNECTORS AS A POSSIBLE SOURCE OF TROUBLE WHEN CHECKING A PROBLEM AREA.

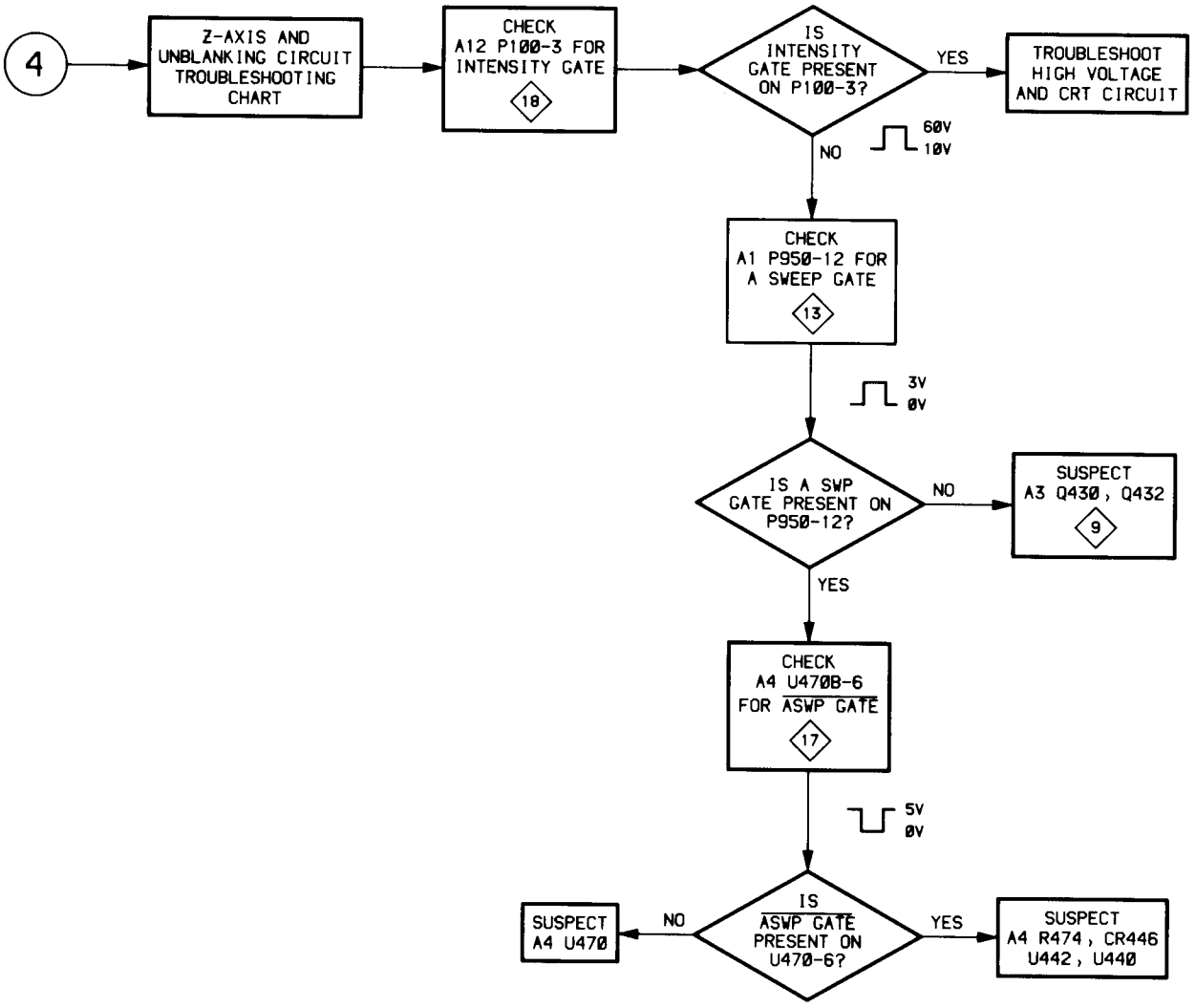






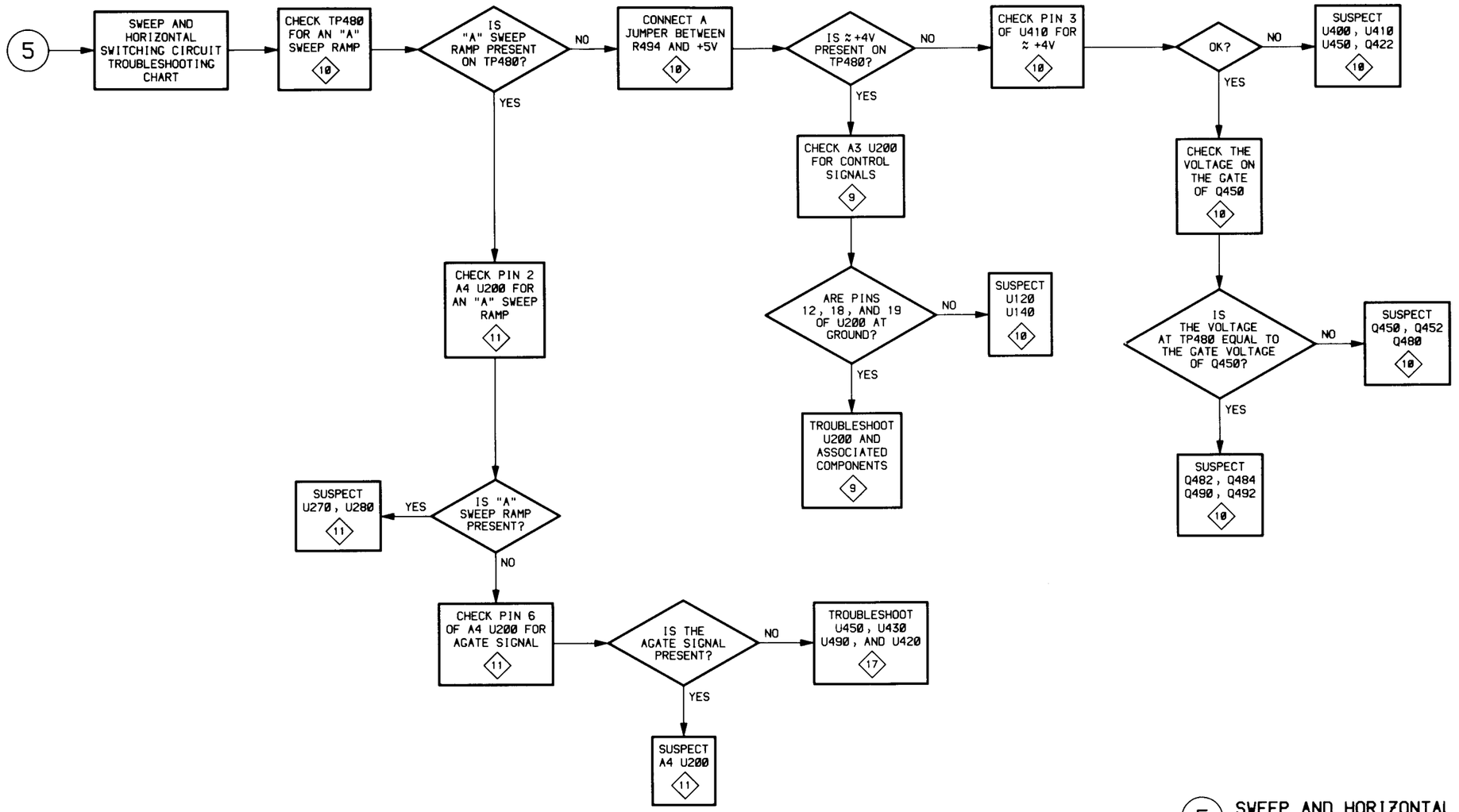
3 READOUT CIRCUIT TROUBLESHOOTING

4421-88



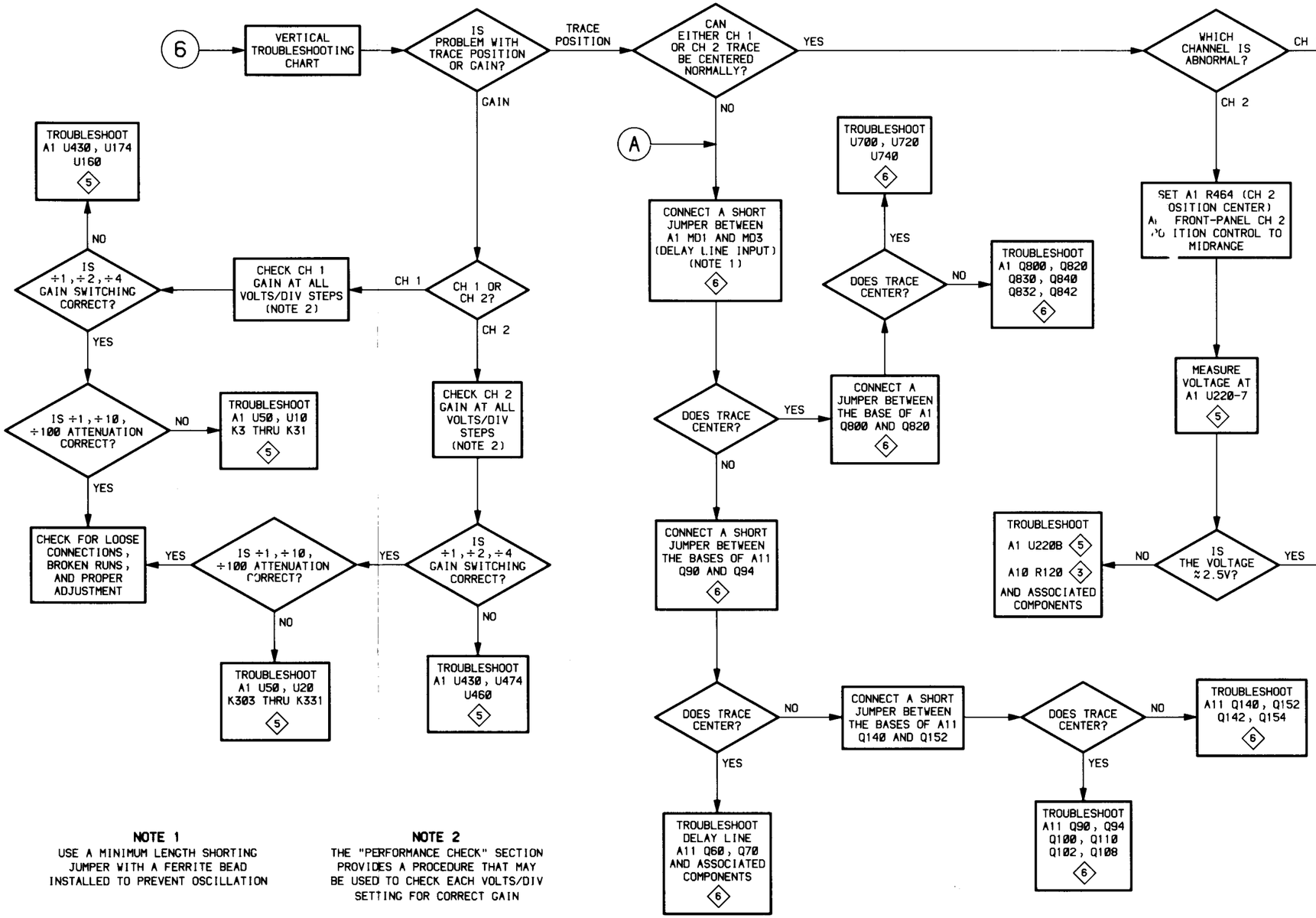
4 Z-AXIS AND UNBLANKING CIRCUIT TROUBLESHOOTING

4421-87



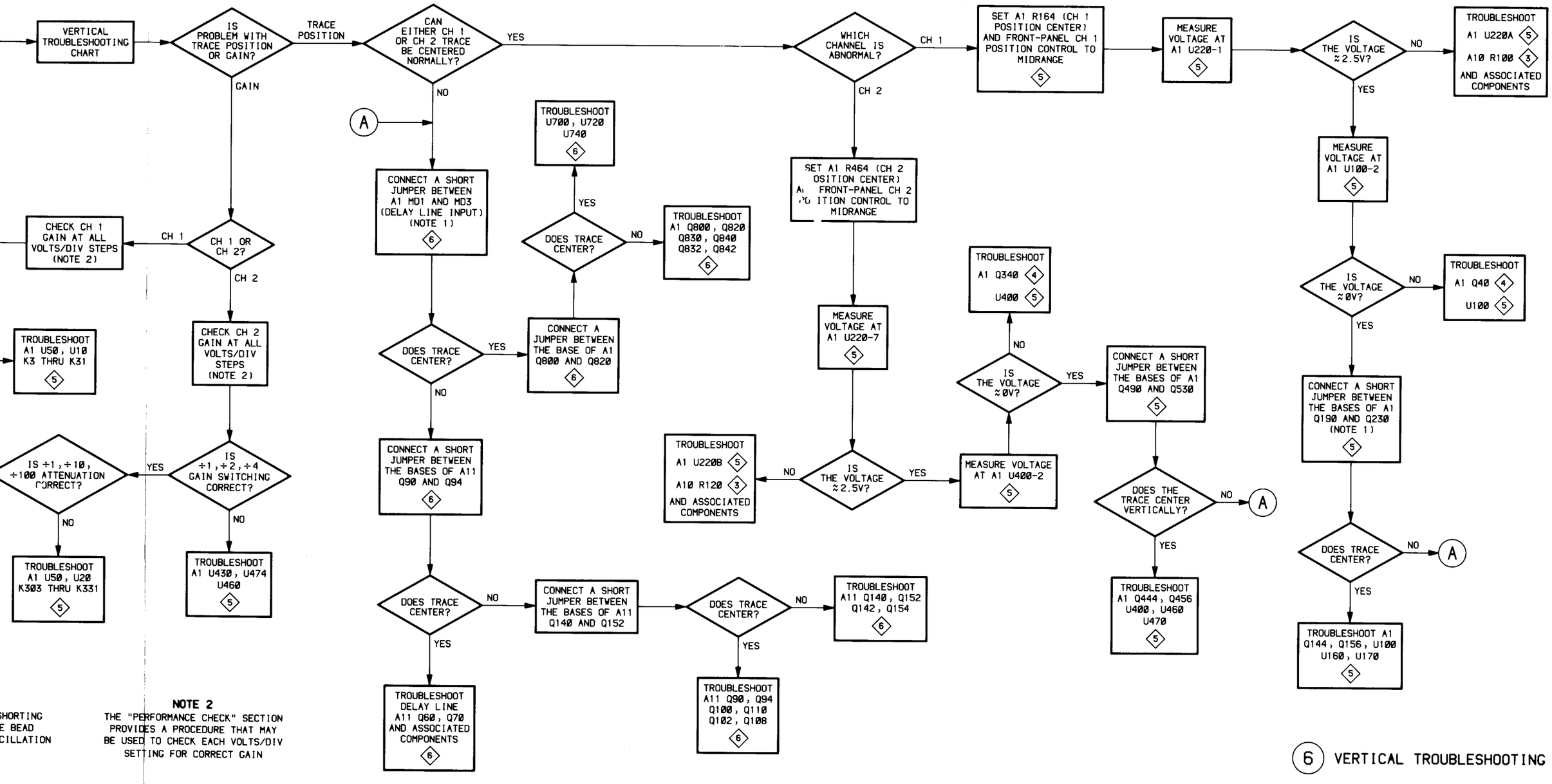
(5) SWEEP AND HORIZONTAL TROUBLESHOOTING

4421-89



NOTE 1
USE A MINIMUM LENGTH SHORTING JUMPER WITH A FERRITE BEAD INSTALLED TO PREVENT OSCILLATION

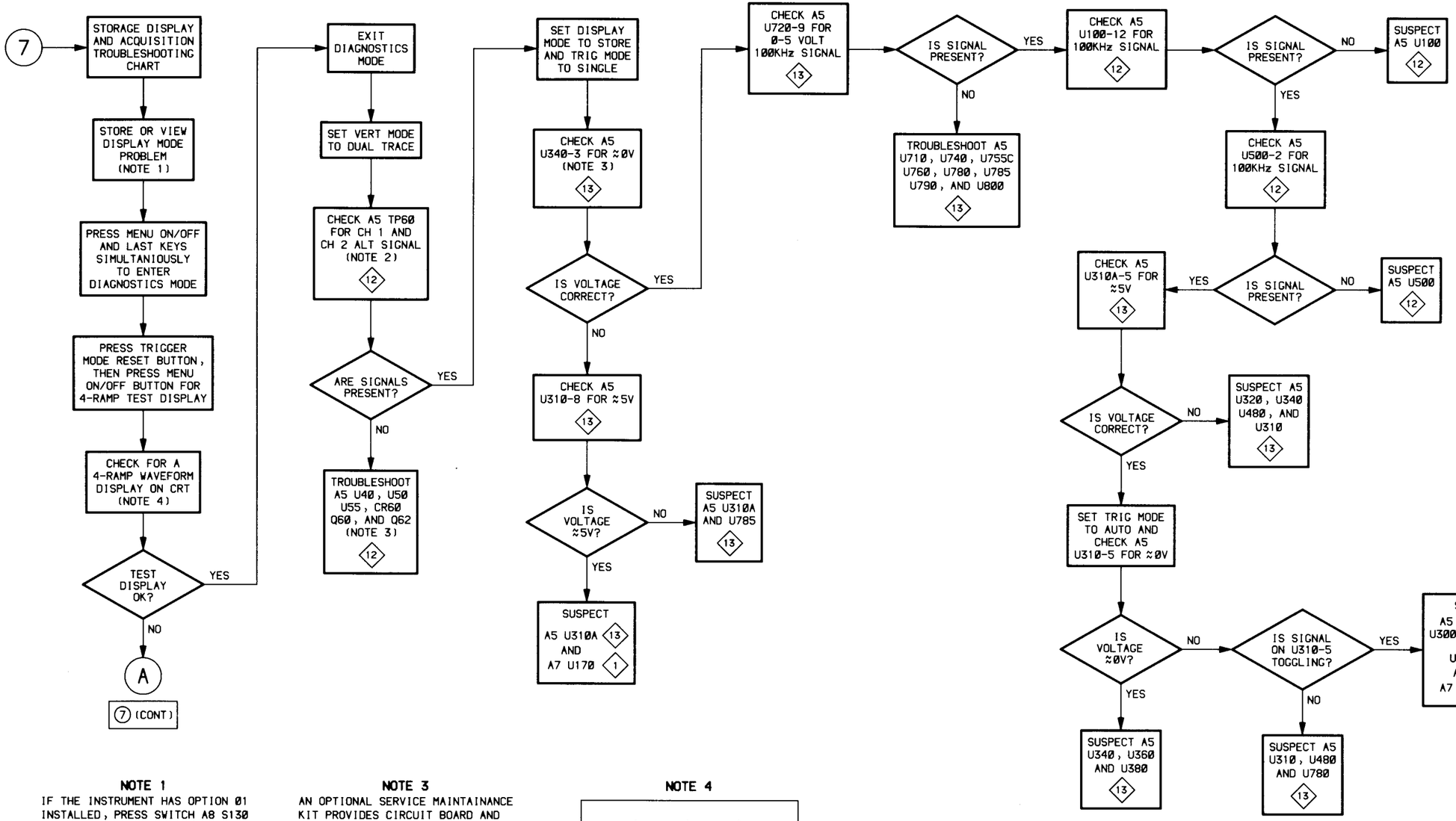
NOTE 2
THE "PERFORMANCE CHECK" SECTION PROVIDES A PROCEDURE THAT MAY BE USED TO CHECK EACH VOLTS/DIV SETTING FOR CORRECT GAIN



NOTE 2

THE "PERFORMANCE CHECK" SECTION PROVIDES A PROCEDURE THAT MAY BE USED TO CHECK EACH VOLTS/DIV SETTING FOR CORRECT GAIN

6 VERTICAL TROUBLESHOOTING



NOTE 1

IF THE INSTRUMENT HAS OPTION 01 INSTALLED, PRESS SWITCH A8 S130 WHILE THE INSTRUMENT POWER IS OFF BEFORE STARTING THIS TROUBLESHOOTING PROCEDURE.

NOTE 2

TEST OSCILLOSCOPE SET UP:

Vert Mode	CH 1
A SEC/DIV	0.2ms
Volts/Div	0.5V

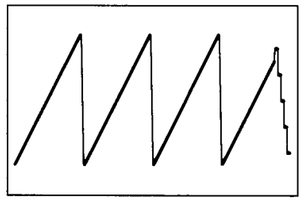
NOTE 3

AN OPTIONAL SERVICE MAINTAINANCE KIT PROVIDES CIRCUIT BOARD AND CABLE EXTENDERS TO EASE THE TASK OF TROUBLESHOOTING AND SIGNAL TRACING.

THE KIT ENABLES OPERATION OF THE INSTRUMENT WITH THE PLUG-IN CIRCUIT BOARDS IN AN EXTENDED POSITION.

SEE TABLE 6-6 IN SECTION 6 OF THIS MANUAL FOR THE TEKTRONIX PART NUMBER OF THE KIT.

NOTE 4



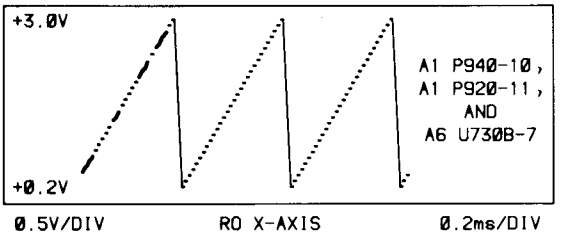
4-RAMP TEST SIGNAL DISPLAY

7 STORAGE DISPLAY AND ACQUISITION TROUBLESHOOTING

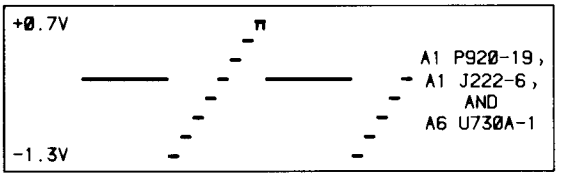
4421-92

NOTE 5

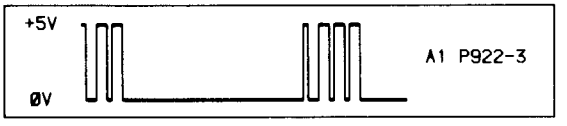
WAVEFORMS ASSOCIATED WITH TROUBLESHOOTING CHART 7 (CONT)



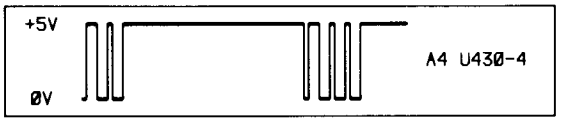
0.5V/DIV RO X-AXIS 0.2ms/DIV



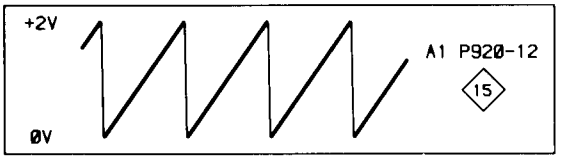
0.5V/DIV STORAGE Y-AXIS 2ms/DIV



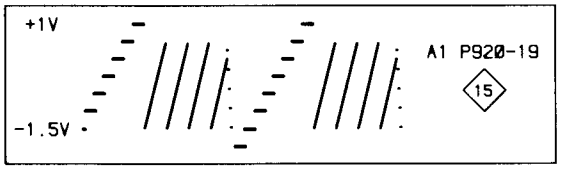
1V/DIV $\overline{\text{RO BLANK}}$ 0.1ms/DIV



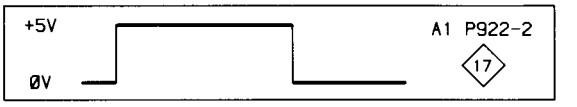
1V/DIV RO BLANK 0.1ms/DIV



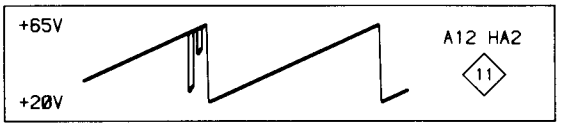
0.5V/DIV STORAGE X-AXIS 2ms/DIV



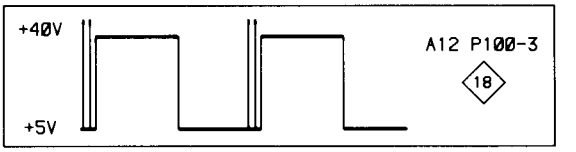
0.5V/DIV STORAGE Y-AXIS 2ms/DIV



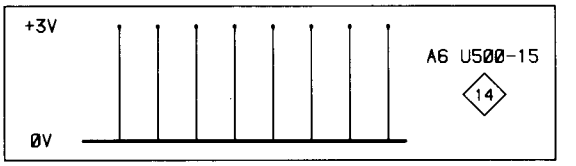
2V/DIV $\overline{\text{WFM BLANK}}$ 1ms/DIV



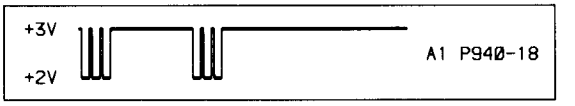
10V/DIV + HORIZ OUT 1ms/DIV



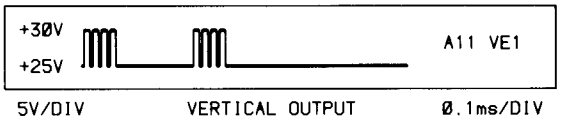
10V/DIV INTENSITY 2ms/DIV



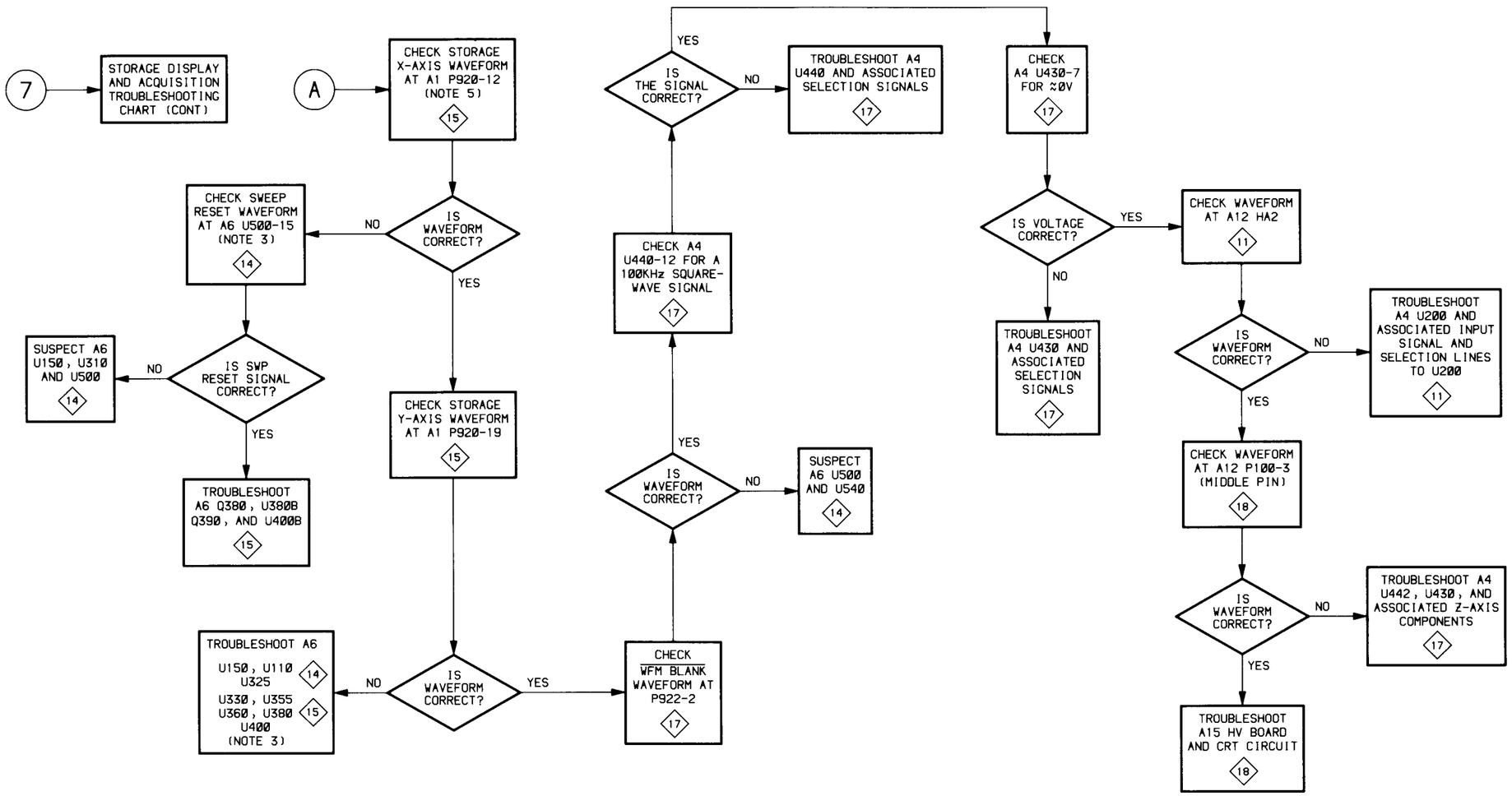
1V/DIV SWP RESET 5ms/DIV



0.5V/DIV REAL 0.1ms/DIV

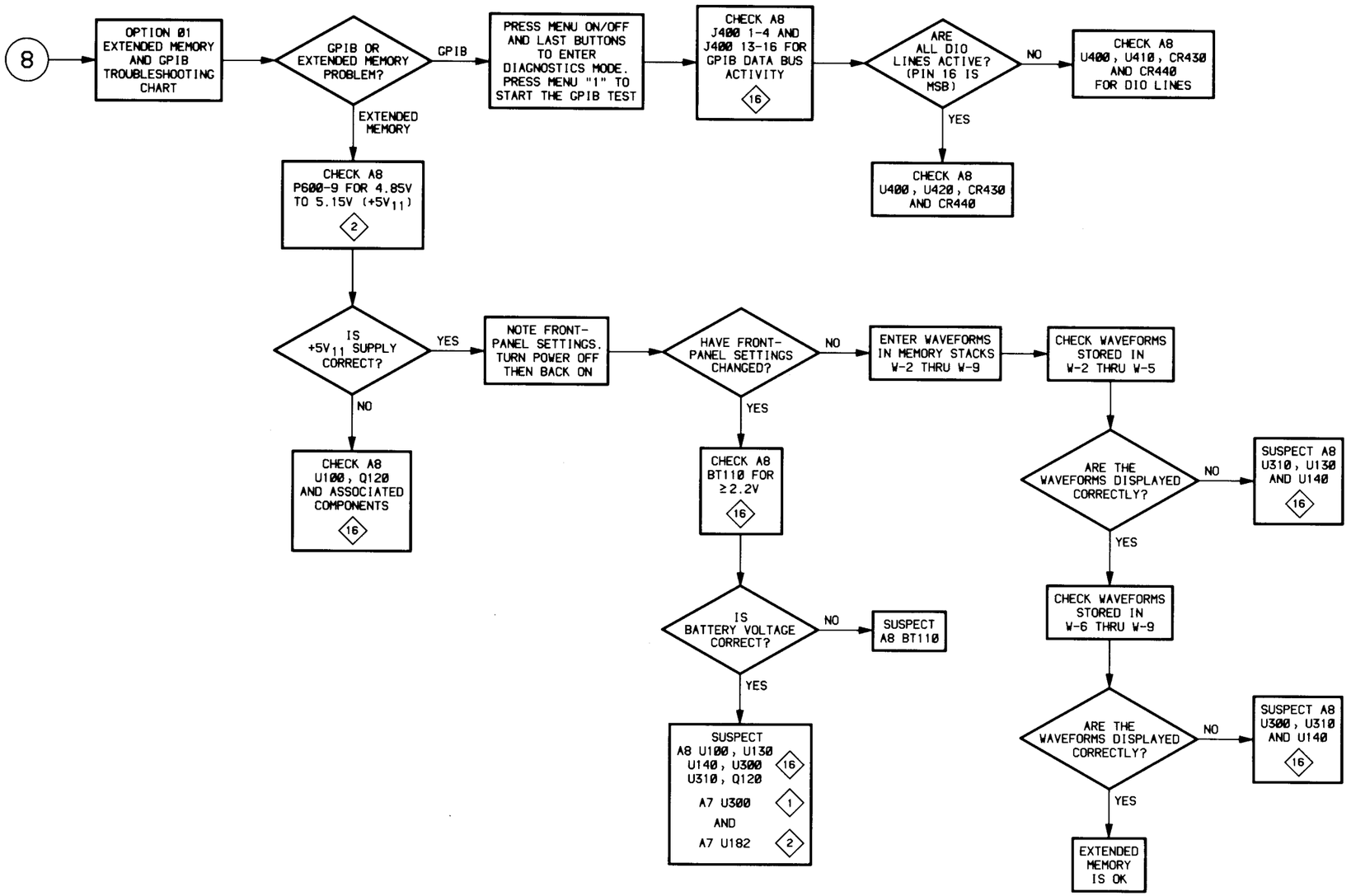


5V/DIV VERTICAL OUTPUT 0.1ms/DIV



7 STORAGE DISPLAY AND ACQUISITION TROUBLESHOOTING (CONT)

4421-93



8 OPTION Ø1 EXTENDED MEMORY AND GPIB TROUBLESHOOTING

4421-90

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 *Name & Description*

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
0000M	SONY/TEKTRONIX CORPORATION	P O BOX 14, HANEDA AIRPORT	TOKYO 149, JAPAN
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
06383	PANDUIT CORPORATION	17301 RIDGELAND	TINLEY PARK, IL 60477
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
16428	BELDEN CORP.	P. O. BOX 1331	RICHMOND, IN 47374
24931	SPECIALITY CONNECTOR CO., INC.	2620 ENDRESS PLACE	GREENWOOD, IN 46142
26365	GRIES REPRODUCER CO., DIV. OF COATS AND CLARK, INC.	125 BEECHWOOD AVE.	NEW ROCHELLE, NY 10802
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
74868	BUNKER-RAMO CORP., THE AMPHENOL RF DIV.	33 E. FRANKLIN ST.	DANBURY, CT 06810
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
80126	PACIFIC ELECTRICORD CO.	747 W. REDONDO BEACH,P O BOX 10	GARDENA, CA 90247
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
86928	SEASTROM MFG. COMPANY, INC.	701 SONORA AVENUE	GLENDALE, CA 91201
96904	NATVAR CORP.	211 RANDOLPH AVE.	WOODBRIDGE, NJ 07095
98159	RUBBER TECK, INC.	19115 HAMILTON AVE., P O BOX 389	GARDENA, CA 90247
98291	SEALECTRO CORP.	225 HOYT	MAMARONECK, NY 10544
S3109	C/O PANEL COMPONENTS CORP.	P.O. BOX 6626	SANTA ROSA, CA 95406
S3629	PANEL COMPONENTS CORP.	2015 SECOND ST.	BERKELEY, CA 94170

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	200-2856-00			1		RTNR,CRT SCALE:GRAY		
						**********(ATTACHING PARTS)**********		
-2	211-0101-00			2		SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
						**********(END ATTACHING PARTS)*********		
-3	378-0224-00			1		FILTER,LIGHT:BLUE,73.2MM X 60.5MM X 2.2MM		
-4	386-5028-00			1		SUPPORT,CRT:FRONT		
-5	366-2063-01			3		KNOB:DOVE GRAY,3.25MM ID X 12MM OD X 13MM		
-6	366-2062-01			3		KNOB:DOVE GRAY,3.25MM ID X 9.5MM OD X 13MM		
-7	366-2065-01			1		KNOB:DOVE GRAY,6.35MM ID X 18MM OD X 18MM		
-8	366-2064-01			2		KNOB:DOVE GRAY,4.1MM ID X 16MM OD X 15.5MM		
-9	426-1072-00			1		FRAME,PUSH BTN:PLASTIC	80009	426-1072-00
-10	366-2062-03			4		KNOB:DOVE GRAY,3.25MM ID X 9.5MM OD X 13MM		
-11	211-0680-00			4		SCREW,MACHINE:2-56 X 0.138 L,HEX SOCKET		
	361-1266-00			4		SPACER,RING:0.7 L X 2.4 ID MM		
-12	333-3027-01			1		PANEL,FRONT:		
-13	----- -----			1		CKT BOARD ASSY:MOTHER KEYBOARD(SEE A9 REPL		
						**********(ATTACHING PARTS)**********		
-14	211-0661-00			5		SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	78189	OBD
						**********(END ATTACHING PARTS)*********		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
-15	407-3079-00			1		.BRACKET,VAR RES:		
-16	407-3082-00			1		.BRACKET,VAR RES:		
-17	407-3081-00			1		.BRACKET,VAR RES:		
-18	214-2017-00			1		.ACTUATOR,SWITCH:A&B SEC/DIV		
						.**********(ATTACHING PARTS)**********		
-19	211-0101-00			1		.SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
						.**********(END ATTACHING PARTS)*********		
-20	376-0214-00			1		.CPLG,SHAFT,RIGID:6.2 ID X 8.9 OD		
-21	214-2016-00			1		.ACTUATOR,SL SW:A&B SEC/DIV		
-22	210-0406-00			1		.NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
-23	129-1008-00			2		.SPACER,POST:13.9MM L,2/4-40 INT THD ONE E		
-24	354-0009-00			1		RING,RETAINING:E TYPE 5,4.3MM OD		
-25	----- -----			1		CKT BOARD ASSY:KEYBOARD(SEE A10 REPL)		
-26	407-3080-00			1		.BRACKET,VAR RES:		
-27	366-2056-00			1		PUSH BUTTON:FLINT GRAY,5.5MM X 2.8MM X 13M		
-28	366-2059-00			11		PUSH BUTTON:CLEAR,2.8MM SQ X 11.4MM H		
-29	366-2060-00			7		PUSH BUTTON:DOVE GRAY,55MM X 2.8MM X 1.3MM		
-30	366-2061-00			1		PUSH BUTTON:FLINT GRAY,2.8MM SQ X 13MM H		
-31	----- -----			-		(SUBPARTS OF A10R100,R120,R140 REPL)		
-32	366-2057-00			2		PUSH BUTTON:DOVE GRAY,5.5MM X 2.8MM X 2.5M		
-33	351-0710-00			1		GUIDE,PB:		
-34	220-0738-00			2		NUT,CIRCUIT BD:4-40 X 0.188 HEX,BRS NP	0000M	220-0738-00
-35	129-1013-00			1		SPACER,POST:20.6MM L W/4-40 INT THD ONE EN		
-36	210-0407-00			1		NUT,PLAIN,HEX.:6-32 X 0.25 INCH,BRS	73743	3038-0228-402
-37	210-0202-00			1		TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
-38	129-1014-00			4		SPACER,POST:25.4MM L W/4-40 INT THD,HEX		
-39	386-5028-00			1		SUPPORT,CRT:FRONT		
						**********(ATTACHING PARTS)**********		
-40	211-0105-00			2		SCREW,MACHINE:4-40 X 0.188,100 DEG,FLH ST	83385	OBD
						**********(END ATTACHING PARTS)*********		
-41	----- -----			1		POWER SUPPLY:(SEE U120 CHASSIS REPL)		
						**********(ATTACHING PARTS)**********		
-42	211-0102-00			2		SCREW,MACHINE:4-40 X 0.500",FLH,STL	83385	OBD
-43	220-0646-00			2		NUT,PRESSMOUNT:4-40 X 0.188 HEX		
						**********(END ATTACHING PARTS)*********		
-44	----- -----			1		CABLE DELAY LINE:(SEE DL500 CHASSIS REPL)		
-45	343-0549-00			3		STRAP,TIEDOWN:0.091 W X 3.62 L	06383	PLT1M
-46	276-0301-00			1		FORM,COIL:DELAY LINE		
						**********(ATTACHING PARTS)**********		
-47	211-0007-00			2		SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
	210-0004-00			2		WASHER,LOCK:#4 INTL,0.015 THK,STL CD PL	000BK	OBD
						**********(END ATTACHING PARTS)*********		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-48	441-1672-00			1		CHASSIS,SCOPE:CENTER		
						**********(ATTACHING PARTS)**********		
-49	211-0101-00			2		SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
						**********(END ATTACHING PARTS)*********		
-50	386-3201-00			1		SUPPORT,CRT:REAR	0000M	386-3201-00
	136-0266-01			1		SKT,PL-IN ELEK:ELCTRN TUBE,12 CONT,W/LEADS	0000M	OBD
-51	334-1378-03			1		MARKER,IDENT:MKD SERIAL NO. FOR SONY/TEK		
-52	334-3360-00			1		MARKER,IDENT:MARKED WARNING	0000M	334-3360-00
-53	337-3106-00			1		SHIELD,CRT:		
-54	162-0018-00			?		INSUL SLVG,ELEC:0.208 ID,VINYL	96904	OBD
-55	348-0067-00			2		GROMMET,PLASTIC:0.312 INCH DIA	80009	348-0067-00
-56	----- -----			1		COIL,TUBE DEFL:(SEE L100 CHASSIS REPL)		
						**********(ATTACHING PARTS)**********		
-57	211-0661-00			4		SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	78189	OBD
						**********(END ATTACHING PARTS)*********		
-58	220-0738-00			2		NUT,CIRCUIT BD:4-40 X 0.188 HEX,BRS NP	0000M	220-0738-00
-59	211-0501-00			1		SCREW,MACHINE:6-32 X 0.125 INCH,PNH STL	83385	OBD
-60	210-0202-00			1		TERMINAL,LUG:0.146 ID,LOCKING,BRZ TINNED	78189	2104-06-00-2520N
-61	----- -----			1		CKT BOARD ASSY:HORIZONTAL OUTPUT(SEE A12 R		
						**********(ATTACHING PARTS)**********		
-62	211-0661-00			2		SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	78189	OBD
						**********(END ATTACHING PARTS)*********		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
	198-5156-00			1		.WIRE SET,ELEC:	80009	198-5156-00
-63	----- -----			1		CKT BOARD ASSY:VERTICAL OUTPUT(SEE A11 REP		
						**********(ATTACHING PARTS)**********		
-64	211-0661-00			2		SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	78189	OBD
						**********(END ATTACHING PARTS)*********		
	----- -----			-		CKT BOARD ASSY INCLUDES:		
	198-5157-00			1		.WIRE SET,ELEC:	80009	198-5157-00
-65	211-0105-00			4		SCREW,MACHINE:4-40 X 0.188,100 DEG,FLH ST	83385	OBD
-66	220-0738-00			2		NUT,CIRCUIT BD:4-40 X 0.188 HEX,BRS NP	0000M	220-0738-00
-67	366-2055-00			1		PUSH BUTTON:DOVE GRAY,POWER SWITCH		
-68	384-0503-00			1		EXTENSION SHAFT:8.346 L X 0.079 OD		
-69	343-1097-00			1		COLLAR,SHAFT:		
-70	214-3451-00			1		SPRING,HLCPS:3.5MM OD X 12.0MM L,OPEN END		
-71	131-2937-00			1		CONN,RCPT,ELEC:BNC,FEMALE		
						**********(ATTACHING PARTS)**********		
-72	211-0005-00			2		SCREW,MACHINE:4-40 X 0.125 INCH,PNH STL	83385	OBD
						**********(END ATTACHING PARTS)*********		
-73	348-0171-00			1		GROMMET,PLASTIC:U-SHAPED	80009	348-0171-00
-74	441-1673-00			1		CHASSIS,SCOPE:LEFT	80009	441-1673-00

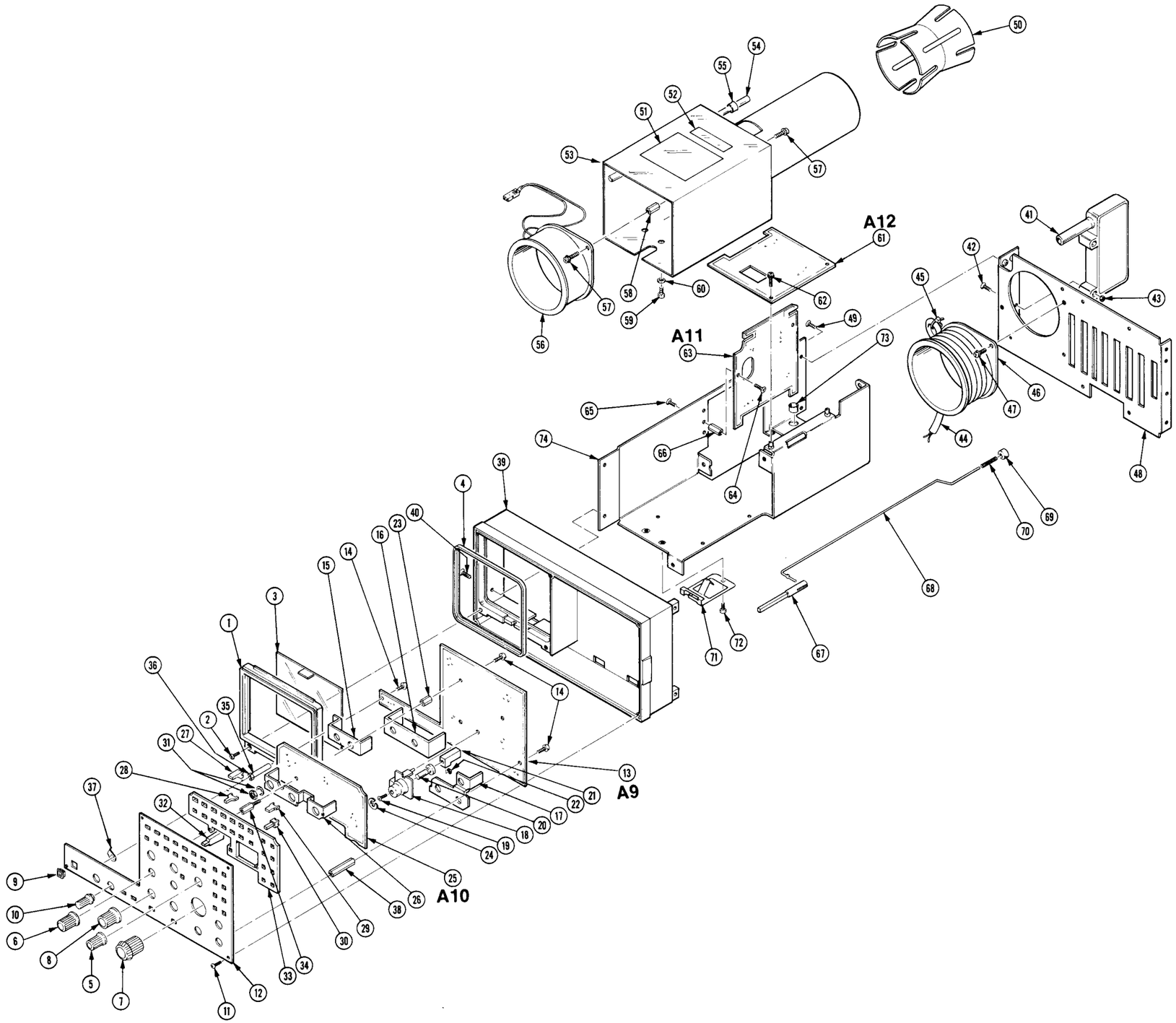

A12
A11
A9
A10

FIG. 2 CIRCUIT BOARDS

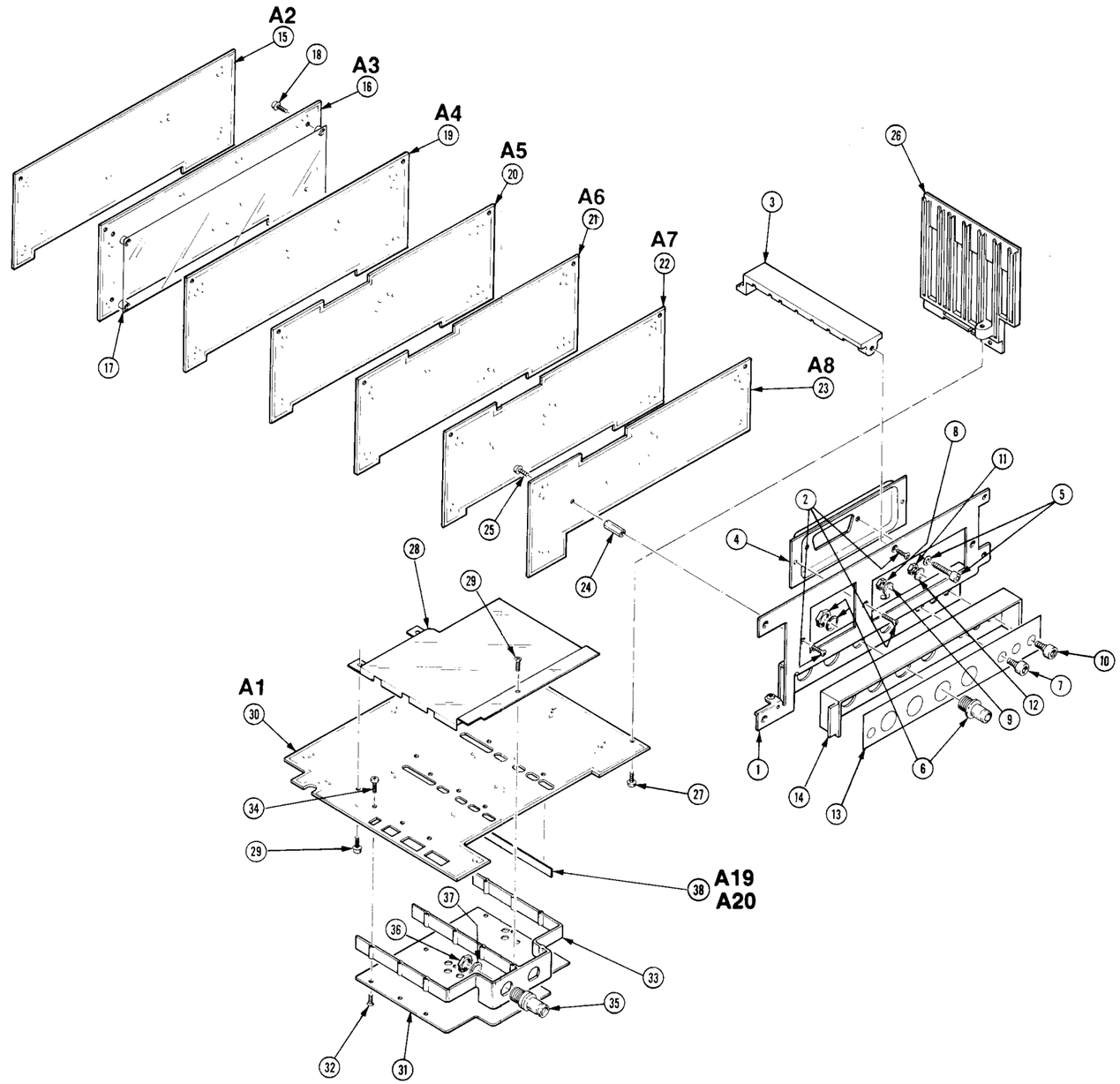


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-1	441-1671-00			1		CHASSIS,SCOPE:RIGHT	80009	441-1671-00
						**********(ATTACHING PARTS)**********		
-2	211-0101-00			7		SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
						**********(END ATTACHING PARTS)*********		
-3	343-1100-00			1		RETAINER,CKT BD:108MM L X 20MM W,GRAY		
	200-2878-00			1		COVER,GPIB:STANDARD		
	----- -----			-		(STANDARD INSTRUMENT - NOT SHOWN)		
-4	200-2860-00			1		COVER,CONNECTOR:ALUM		
	----- -----			-		(GPIB OPTION ONLY)		
						**********(ATTACHING PARTS)**********		
-5	----- -----			2		CONN,RCPT,ELEC:FEMALE,GPIB,2A CONT		
	----- -----			-		(SUBPARTS-SEE A8J400 REPL)		
						**********(END ATTACHING PARTS)*********		
-6	----- -----			2		CONN,RCPT:(SEE J106,J108 CHASSIS REPL)		
-7	----- -----			2		CONN,RCPT:(SEE J100,J102 CHASSIS REPL)		
						**********(ATTACHING PARTS)**********		
-8	210-0465-00			2		NUT,PLAIN,HEX.:0.25-32 X 0.375 INCH BRS	73743	3095-402
-9	210-0223-00			2		TERMINAL,LUG:0.25 INCH DIA,SE	86928	A313-136
						**********(END ATTACHING PARTS)*********		
-10	----- -----			1		JACK,TIP:(SEE J104 CHASSIS REPL)		
						**********(ATTACHING PARTS)**********		
-11	210-0465-00			1		NUT,PLAIN,HEX.:0.25-32 X 0.375 INCH BRS	73743	3095-402
-12	210-0046-00			1		WASHER,LOCK:0.261 ID,INTL,0.018 THK,BRS	78189	1214-05-00-0541C
						**********(END ATTACHING PARTS)*********		
-13	386-5027-00			1		PANEL,SIDE:		
-14	407-3077-00			1		BRACKET,INPUT:	80009	407-3077-00
-15	----- -----			1		CKT BOARD ASSY:TRIGGER(SEE A2 REPL)		
	198-5160-00			1		.WIRE SET,ELEC:	80009	198-5160-00
	131-1555-00			1		.CONTACT,ELEC:GROUNDING		
-16	----- -----			1		CKT BOARD ASSY:SWEEP(SEE A3 REPL)		
-17	337-3105-00			1		.SHIELD,ELEC:SWEEP		
						.**********(ATTACHING PARTS)**********		
-18	211-0661-00			4		.SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	78189	OBD
						.**********(END ATTACHING PARTS)*********		
	198-5159-00			1		.WIRE SET,ELEC:	80009	198-5159-00
-19	----- -----			1		CKT BOARD ASSY:CONTROL(SEE A4 REPL)		
-20	----- -----			1		CKT BOARD ASSY:ACQUISITION(SEE A5 REPL)		
	346-0032-00			1		.STRAP,RETAINING:0.075 DIA X 4.0 L,MLD RBR	98159	2859-75-4
-21	----- -----			1		CKT BOARD ASSY:DISPLAY(SEE A6 REPL)		
-22	----- -----			1		CKT BOARD ASSY:CPU(SEE A7 REPL)		
-23	----- -----			1		CKT BOARD ASSY:OPTION		
	----- -----			-		(SEE A8 REPL - GPIB OPTION ONLY)		
	175-8961-00			1		.CA ASSY,SP,ELEC:10,26 AWG,90MM L,RIBBON		
-24	129-1010-00			1		.SPACER,POST:14.3MM L W/4-40 INT THD,HEX		
						.**********(ATTACHING PARTS)**********		
-25	211-0661-00			1		.SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	78189	OBD
						.**********(END ATTACHING PARTS)*********		
-26	351-0711-00			1		GUIDE,CKT BD:90.5MM L		
						**********(ATTACHING PARTS)**********		
-27	211-0101-00			1		SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
	211-0661-00			1		SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	78189	OBD
						**********(END ATTACHING PARTS)*********		
-28	200-2859-00			1		COVER,ATTEN:BOTTOM		
	----- -----			-		(SUBPART OF A1)		
						**********(ATTACHING PARTS)**********		
-29	211-0661-00			3		SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	78189	OBD
						**********(END ATTACHING PARTS)*********		
-30	----- -----			1		CKT BOARD ASSY:MAIN(SEE A1 REPL)		
	131-0157-00			2		.TERMINAL,PIN:0.25 L X 0.04 OD,BRS	98291	013-1001-000-479
	198-5161-00			1		.WIRE SET,ELEC:	80009	198-5161-00
-31	200-2858-00			1		.COVER,ATTENUATOR:TOP		
						**********(ATTACHING PARTS)**********		
-32	211-0101-00			9		.SCREW,MACHINE:4-40 X 0.25,100 DEG,FLH STL	83385	OBD
						**********(END ATTACHING PARTS)*********		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-33	337-3109-00			1		.SHIELD,ELEC:ATTENUATOR		
						**********(ATTACHING PARTS)**********		
-34	211-0661-00			9		.SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	78189	OBD
						**********(END ATTACHING PARTS)*********		
-35	----- -----			2		.CONN,RCPT:(SEE A1J1,J301 REPL)		
						**********(ATTACHING PARTS)**********		
-36	220-0497-00			2		.NUT,PLAIN,HEX.:0.5-28 X 0.562 INCH HEX,BR	73743	OBD
-37	210-1039-00			2		.WASHER,LOCK:INT,0.521 ID X 0.625 INCH O	24931	OBD
						**********(END ATTACHING PARTS)*********		
-38	----- -----			2		.CKT BOARD ASSY:ATTENAUTOR(SEE A19,A20 REP		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-32	----- -----			1		CKT BOARD ASSY:PRIMARY(SEE A14 REPL)		
	198-5154-00			1		.WIRE SET,ELEC:	80009	198-5154-00
	342-0652-00			2		.INSULATOR,DISK:32.5MM OD		
	346-0128-00			1		.STRAP,TIE DOWN:0.1W X 8.0" LONG,NYLON	06383	PLT2M
						**********(ATTACHING PARTS)**********		
	211-0040-00			2		.SCREW,MACHINE:4-40 X 0.25",BDGH PLSTC	26365	OBD
	343-0509-00			1		.RETAINER,CAP:GRAY		
						**********(END ATTACHING PARTS)**********		
-33	342-0641-00			1		INSUL,PWR SPLY:		
	334-3379-00			1		MARKER,IDENT:MARKED GROUND SYMBOL	80009	334-3379-00
-34	441-1674-00			1		CHASSIS,SCOPE:REAR	80009	441-1674-00

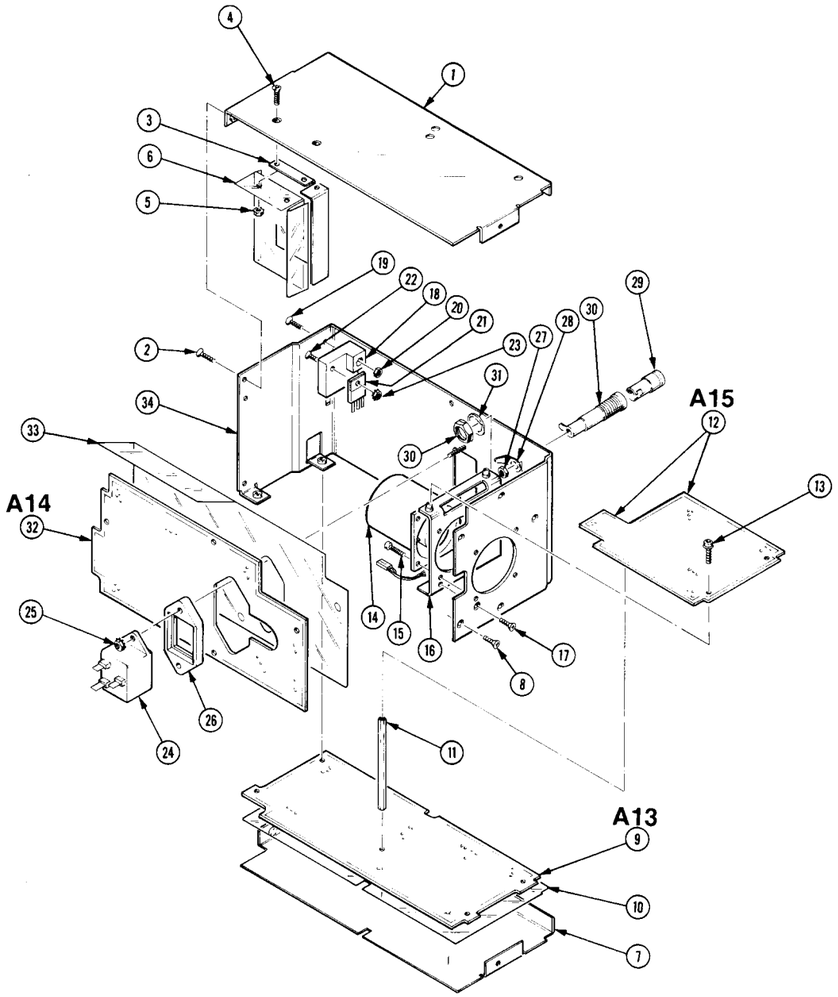
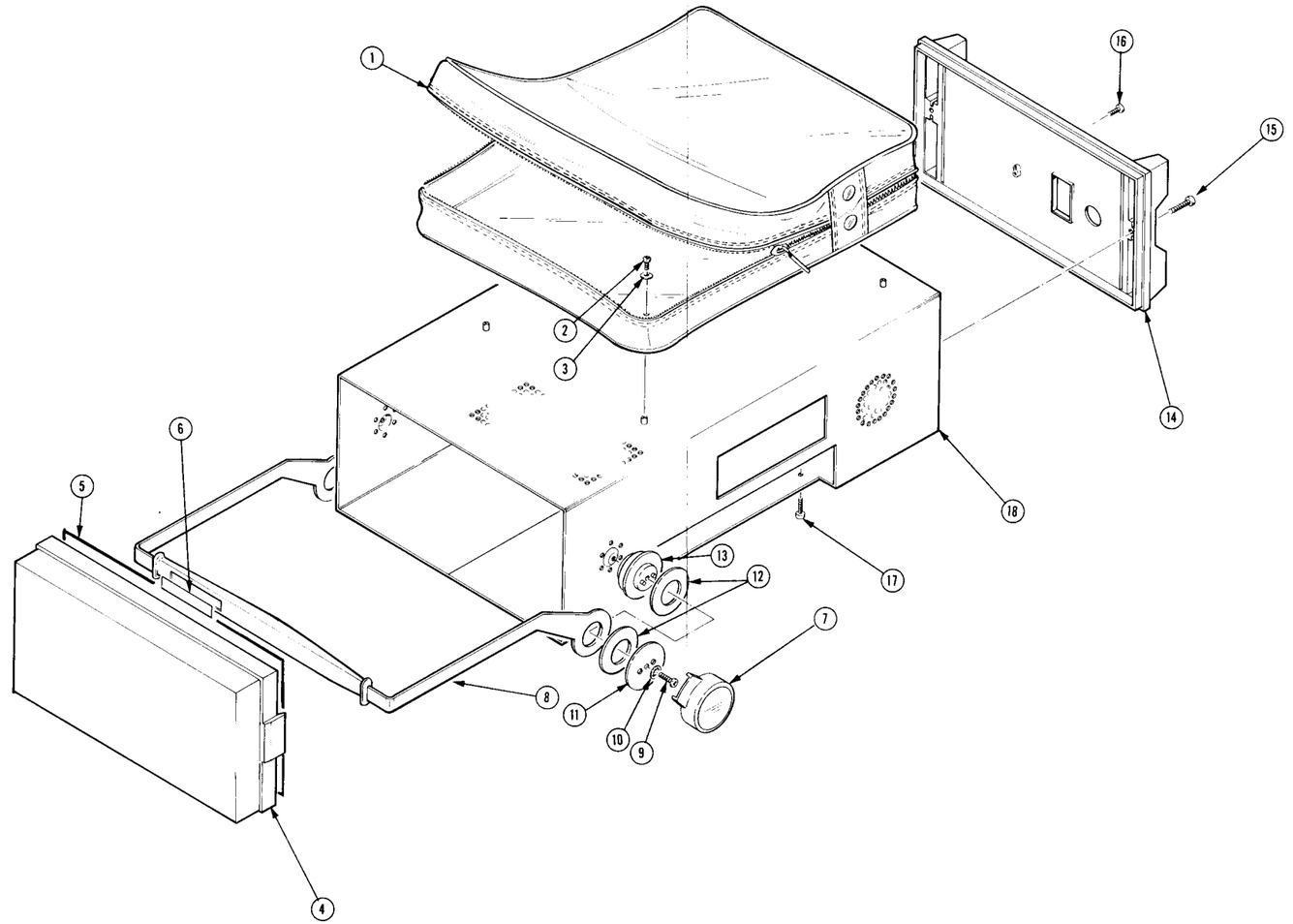


FIG. 3 REAR SECTION

FIG. 4 CABINET & ACCESSORIES



TYPE 336 OSCILLOSCOPE

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
	010-6148-00			2		PROBE,VOLTAGE:10X,PASSIVE	80009	010-6148-00
4-1	016-0718-00			1		POUCH,ACCESSORY:	80009	016-0718-00
						**********(ATTACHING PARTS)**********		
-2	211-0007-00			4		SCREW,MACHINE:4-40 X 0.188 INCH,PNH STL	83385	OBD
-3	210-0851-00			4		WASHER,FLAT:0.119 ID X 0.375 INCH OD,ST	12327	OBD
						**********(END ATTACHING PARTS)*********		
	016-0692-00			1		POUCH,ACCESSORY:2445/2465	80009	016-0692-00
-4	016-0719-00			1		COVER,PROT:FRONT	80009	016-0719-00
-5	334-5128-00			1		MARKER,IDENT:MKD MENU DIAGRAM	80009	334-5128-00
	159-0016-00			1		FUSE,CARTRIDGE:3AG,1.5A,250V,FAST-BLOW	71400	AGC 1 1/2
	378-0225-00			1		FILTER,LIGHT:CLEAR,73.2MM X 60.5MM X 2.0MM		
	070-4420-00			1		MANUAL,TECH:OPER,336 DIGITAL STORAGE SCOPE	80009	070-4420-00
	070-4421-00			1		MANUAL,TECH:SVCE,336 DIGITAL STORAGE SCOPE	80009	070-4421-00
						CUSTOMER MAY SELECT ONE OF SIX POWER SUPPL OPTIONS WHICH WILL BE INSTALLED.		
	161-0104-00			1		CABLE ASSY,PWR,:3 WIRE,98.0" LONG	16428	KH8352
	----- -----			-		(STANDARD)		
	161-0104-06			1		CABLE ASSY,PWR:3 X 0.75MM SQ,220V,98.0L	S3109	OBD
	----- -----			-		(A1 EUROPEAN)		
	161-0104-07			1		CABLE ASSY,PWR:3 X 0.75MM SQ,240V,98.0 L	80126	OBD
	----- -----			-		(A2 UNITED KINGDOM)		
	161-0104-05			1		CABLE ASSY,PWR:3,18 AWG,240V,98.0 L	S3109	OBD
	----- -----			-		(A3 AUSTRALIAN)		
	161-0104-08			1		CABLE ASSY,PWR:3,18 AWG,240V,98.0 L	80126	OBD
	----- -----			-		(A4 NORTH AMERICAN)		
	161-0167-00			1		CABLE ASSY,PWR:3.0 X 0.7,6A,240V,2.5M		
	----- -----			-		(A5 SWISS)		
						THE FOLLOWING ARE SUBPARTS OF THE CABINET:		
-6	334-5132-00			1		PLATE,IDENT:MKD 336 OSCILLOSCOPE		
-7	200-1342-00			2		COVER,HANDLE:35.5MM OD X 14MM H,PLASTIC	0000M	200-1342-00
-8	367-0203-00			1		HANDLE,CARRYING:BLACK VINYL	0000M	367-0203-00
						**********(ATTACHING PARTS)**********		
-9	212-0003-00			2		SCREW,MACHINE:	83385	OBD
-10	210-0008-00			2		WASHER,LOCK:INTL,0.172 ID X 0.331"OD,S	78189	1208-00-00-0541C
-11	386-3936-00			2		PLATE,MOUNTING:HANDLE,STEEL	0000M	386-3936-00
-12	386-2182-00			4		PLATE,FRICTION:	0000M	386-2182-00
-13	343-0757-00			2		RETAINER,HANDLE:	0000M	343-0757-00
						**********(END ATTACHING PARTS)*********		
-14	200-2857-00			1		COVER,REAR:		
						**********(ATTACHING PARTS)**********		
-15	211-0511-00			2		SCREW,MACHINE:6-32 X 0.500,PNH,STL,CD PL	83385	OBD
						**********(END ATTACHING PARTS)*********		
-16	213-0816-00			1		SCREW,TPG,TC:2-56 X 0.188 L,TYPE T PNH	000BK	OBD
-17	211-0504-00			2		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
-18	390-0900-00			1		CABINET,SCOPE:OPTION	80009	390-0900-00
	----- -----			-		(OPT 01 OR OPT 03 ONLY)		
	390-0901-00			1		CABINET,SCOPE:STANDARD	80009	390-0901-00
	----- -----			-		(STANDARD OR OPT 02 ONLY)		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						OPTIONAL ACCESSORIES		
	012-0630-03					CABLE,INTCON:2 METERS L	74868	AC30147-102
	012-0630-04					CABLE,INTCON:4.0 M	74868	408-301471-X
	016-0297-00					VISOR,CRT:	80009	016-0297-00
	016-0327-01					ADAPTER,CAMERA:EXTENSION		
	067-1161-00					FIXTURE,CAL:SERVICE MAINTENANCE	80009	067-1161-00
	----- -----					(FOR SERVICING ONLY)		
	346-0132-01					STRAP ASSEMBLY:W/PROTECTIVE RINGS		
	378-0223-00					FILTER,MESH:73.MM X 61.1MM X 2.2MM		
	670-8133-00					CKT BOARD ASSY:LOAD MODULE	80009	670-8133-00
	----- -----					(FOR SERVICING ONLY)		
	----- -----					C30B SERIES CAMERA		