SECTION 5

MAINTENANCE

5.1 INTRODUCTION

Section 5 contains information concerning general RF-590 repair, Built-In Test Equipment (BITE) description and fault code chart, overall receiver performance tests, and component data.

5.2 PWB REPAIRS

The following general rules and techniques are useful in servicing RF-590 printed circuit boards.

- When replacing components on printed wiring boards (PWB), clip the mounting leads with a suitable pair of diagonal cutters and remove the component. This is especially helpful on multilead components such as the dual inline and circular type integrated circuits. The individual leads are then removed from the PWB with a low wattage iron.

- Before removing an integrated circuit from a PWB, note orientation of the pin locating tab and make sure the replacement component is reinstalled in exactly the same way.

- Because of the double sided construction used on many of the PWBs in the RF-590, a component lead may be soldered to printed circuit areas on the top and bottom of the PWB. Consequently, when a component lead is removed, the replacement component should be resoldered top and bottom as applicable.

- Overheating a printed circuit conductor may cause it to pull loose from the board material. Apply only the minimum amount of heat necessary for component removal or replacement. The use of a soldering iron in the 25 to 35 watt range is recommended.

- A desoldering tool (solder-sucker) is very convenient (and minimizes board damage) when removing multilead components which cannot be cut loose with diagonal cutters. Components of this type include special PWB transformers mounted on solderable leads and double balanced mixers, both used extensively in the various assemblies.

- A convenient device to use in place of a solder-sucker is a roll of Solder-Wick, manufactured by Solder Removal Co., Covina, California. This flux-saturated copper braid is often more effective than a solder-sucker for removing solder from PWBs.

5.3 MOSFET REPLACEMENT

When handling and replacing Metal-Oxide Substrate Field-Effect Transistor (MOSFET) devices, the following three (3) steps should be performed.

a. Remove new MOSFET from package. The four leads will be connected together with a small ferrule or wire to prevent static voltage differences from developing between the gate and substrate terminals. If the ferrule is present, wrap several turns of small solid wire around the leads and then remove the ferrule.

b. Position the four leads and carefully install the MOSFET on the PWB.

c. Remove the jumper(s) only after the leads have been soldered.

5.4 CMOS HANDLING AND REPLACEMENT

All Complementary Offset Symmetry Metal-Oxide Semiconductor (CMOS) devices have diode input protection against adverse electrical environments such as static electricity.

Although the devices contain circuitry to protect inputs against damage due to high voltages or electrical fields, precautions should be taken to avoid application of any voltage higher than maximum rated voltages.

Unfortunately, severe electrical conditions can develop during the process of handling. For example, static voltages generated by a person walking across a common waxed floor have been measured in the 4 to 15 kV range. This depends to a great extent upon the humidity, surface conditions, friction, and other factors. These static voltages are potentially disastrous when discharged into a CMOS input, considering the energy stored in the human body at these voltage levels.

Present CMOS gate protection structures can generally protect against overvoltages. However, these same structures will break down under severe conditions such as described above. The following are some suggested handling procedures for CMOS devices, many of which apply to most semiconductors.

- All CMOS devices should be stored or transported in materials that are conductive. CMOS devices must never be inserted into conventional plastic packing material or plastic trays.

- Avoid contact with the leads of the device. The component should always be handled very carefully by the ends or the side opposite the leads.

- Avoid contact between printed wiring board circuits or component leads and synthetic clothing while handling static sensitive devices or assemblies containing them.

- Do not insert or remove CMOS devices when power is applied. Check all power supplies to be used for testing CMOS devices to be certain that the voltage and polarity are correct, and that no transients are present.

- Use only soldering irons and tools that are properly grounded. Ungrounded soldering tips will destroy these devices. Never use soldering guns.

NOTE

When replacing CMOS devices in a PWB, it is recommended that the same procedures for replacing MOSFET devices be followed.

5.5 BUILT-IN TEST EQUIPMENT (BITE) SELF DIAGNOSTICS

The RF-590 has the capability of extensive self-testing in the event of a failure. The general types of tests and the assemblies affected are as follows:

a. Control circuits tests

- Control Board A14
- Driver Board A13A2
- Display Boards A13A4 and A13A5
- Remote Control Board A17

b. Frequency Synthesizer tests

- Reference Generator A12 and Frequency Standard A21
- BFO Assembly A11
- PLL V Assembly A10
- PLL IV Assembly A9
- PLL III Assembly A8
- PLL II Assembly A7
- PLL I Assembly A6

c. Signal Path tests

- Input Filter Assembly A1
- First Converter Assembly A2
- Second Converter Assembly A3
- IF Filter Assembly A4
- IF/Audio Assembly A5A1
- AGC Assembly A5A2

d. Power Supply tests

- Power Supply Assembly A15

Most of these tests can be automatically performed by momentarily pressing the TEST button located on the receiver's front panel. Once the TEST button has been pressed, all receiver front panel controls (except AF GAIN, SPEAKER, and AUDIO LINE LEVEL) become inoperative, and the signal overload relay located on the A1 assembly deenergizes to prevent any possible spurious radiation of test signals during BITE diagnostics.

The normal length of the self-test is approximately 5 seconds. All tests are performed sequentially in their order of importance.

If it is determined that a fault exists in a particular assembly, that assembly number and the corresponding fault code number defining the type of failure will be displayed on the receiver's front panel alphanumeric display. (See table 5-1 for a listing of assembly numbers and fault codes). For example, if the reception of LSB signals became difficult (due to unknown reasons), initiate self-test by pressing TEST. The display, Assy 04 FAULT "02", would probably be shown. Table 5-1 indicates that this would be a fault due to IF Filter Assembly A4 LSB Filter.

If no faults were found during the self testing, the front panel will display ---TEST PASSED---

NOTE

A fault indication may be displayed at initial turn on and will remain on until the frequency standard stabilizes.

When interpreting Built-In Test (BIT) fault indications, do not overlook the possibility that the fault condition at the indicated module may be caused by a failure or marginal condition in an associated module.

Table 5-1. Fault Code Listing

Assembly Number	Fault Code	Description
A1	1	Antenna Overload
	2	Relay Fault (Closed)
	3	BITE Oscillator or A1 RF Det.
	4	Front End Filter
	5	Relay (Open) or dc Det. (TP5)
A2	1	A2 Detector
A3	1	A3 Detector
A4	1	Bypass Signal Path Fault (WBP Pad)
	2	LSB Filter
	3	USB Filter
	4	CW Filter
	5	CW Filter
	6	Special Filter - Slot 5
	7	Special Filter - Slot 6
	8	Special Filter - Slot 7
	9	A5 IF Input Peak Detector or A4 IF Amplifier and Output Circuitry
A5	1	A5 Gain
	2	AM Detector
	3	Line Audio

Table 5-1. Fault Code Listing (Cont.)

Assembly Number	Fault Code	Description
A5 (Cont.)	4	Product Detector
	5	FM Detector
A6	1	PLL I Out-of-Lock
A7	1	Serial Data
	2	PLL II Out-of-Lock
A8	1	Serial Data
	2	PLL III Out-of-Lock
A9	1	PLL IV Out-of-Lock
A10	1	Serial Data
	2	PLL V Out-of-Lock
A11	1	Serial Data
	2	BFO PLL Out-of-Lock
A12	1	1 MHz Reference
	2	800 kHz Reference
	3	40 MHz PLL Out-of-Lock
A13	No Fault Codes (Converter Module)	
A14	1	PROM Failure
	2	8155 RAM Failure
	3	CMOS RAM Failure
	4	Serial Data
	5	8155 Output Port Failure

Table 5-1. Fault Code Listing (Cont.)

Assembly Number	Fault Code	Description
A14 (Cont.)	6	8255 Output Port Failure
	7	A/D Conversion Timing Test
	8,9	A/D Converter Result Test
A15	No Fault Codes (Linear Power Supply)	
A17	1	LCU PROM
	2	LCU Communication
	3	LCU Interface
A18	1	A18 Peak Detector or A4 Output Failure
	2	A18 AGC Level Test
	3	A18 Line Audio Detector

5.5.1 Continuous Self-Test Monitoring

Certain critical circuits which may adversely affect receiver operation or even cause physical damage if they malfunction, are continuously monitored by the self diagnostics. These circuits are as follows:

a. Power Supply A15. All power lines distributed to the receiver are continuously monitored for acceptable voltage limits.

b. RF Input or Antenna Overload. The signal presented to the receiver from the antenna is constantly monitored so that signal path shut down circuits will protect the receiver from an input signal greater than approximately 1.5 Vrms.

c. All Synthesizer Phase Lock Loops (PLL). These PLLs are continually monitored for a locked condition, indicating that the receive frequency stability is assured.

Any of the above mentioned items will cause a front panel FAULT LED to illuminate. Additionally, the RF signal overload would result in a front panel display of ANTENNA OVERLOAD.

5.5.2 Self Diagnostic Operation

The RF-590 self diagnostic tests are a series of sequential tests and measurements used to verify the proper operation of the RF-590. They are described in the following paragraphs. It may be necessary to consult the specific circuit schematics under discussion. These schematics are in the assembly subsections.

5.5.2.1 Lamp Test

The first test performed is a lamp test. All LEDs and segments of the 10 character and 20 character displays located on the front panel are lit. This condition is maintained for approximately 4 seconds for the operator to examine all front panel indicators and while the remainder of the receiver testing is being accomplished.

5.5.2.2 ROM Test (Assembly A14)

ROM test of Control Board Assembly A14 is the next test performed. U5, U6, and U19 contain all the firmware used to control the main receiver functions and are tested to determine that the information they contain is correct. If any of these are found to have a problem, the corresponding fault message will be displayed on the front panel. If at any time this fault is displayed, factory replacements should be obtained. These devices are factory programmed and cannot be repaired in the field.

5.5.2.3 RAM Test (Assembly A14)

The next test to be performed is the RAM test. This test will determine the read/write capability of the 2K CMOS RAM (U8) and 256 byte RAM of the 8155 (U7) located on Control Board Assembly A14. If it is determined that a fault exists, then the appropriate fault message will be displayed on the front panel.

5.5.2.4 I/O Port Tests

Parallel output ports of the A14 assembly are tested next. Output bit patterns are written to U7 and U9 ports, and then read back by the microprocessor to check the data bus path to these devices. If the bit pattern read back is not the same as written, a fault is noted.

5.5.2.5 Serial Data Test

The operation of the parallel-in/serial-out shift registers (U17, U18) on the Control Board and the capability of all synthesizers to accept serial data from the Control Board will now be tested. If a synthesizer fails to receive data correctly, then that assembly will be identified as having failed. If all synthesizers fail then it will be assumed that the Control Board is the faulty assembly.

The synthesizer PLLs are first loaded with all zeros and tested. They are then loaded with 00000000 00000000 001 binary. The one (1) bit will set the serial check line (SW1) of the PLLs to logic 1. This bit is then tested for all PLLs. If a fault occurs, the appropriate fault message will be displayed on the front panel.

5.5.2.6 Reference Generator Test (Assembly A12)

Reference Generator Assembly A12 will be tested next. The 40 MHz lock bit is read and tested for a lock condition (0 = lock). If detected as being out of lock, the proper fault code and assembly number will be displayed on the front panel.

The 1 MHz and 800 kHz detect lines are now read and if a logic 1 is read (indicating a fault), the appropriate fault code and the appropriate assembly number are displayed on the front panel.

5.5.2.7 A/D Converter Tests

The analog-to-digital converter used in the remaining BITE tests is now tested. A conversion is made to confirm that a result is available in approximately 100 microseconds (as indicated by the end-of-conversion output line). Readings are also obtained from two A/D channels tied to the +5 V and ground reference points, respectively. The conversion result bounds are checked. Failure of any of these three tests causes an A14 fault to be indicated.

5.5.2.8 Phase Locked Loop (PLL) Tests

The BFO PLL, PLL I, PLL II, PLL III, PLL IV, and PLL V are now tested to ensure that they can be tuned over their entire range. This testing is done in three steps. These three steps are shown in table 5-2.

Table 5-2. BFO Tuning Range

Range	Receiver Frequency	BFO Frequency
LOW	00,000.000 kHz	9.99 kHz
MID	15,050.500 kHz	0.00 kHz
HIGH	29,999.999 kHz	-9.99 kHz

At each frequency, all PLLs are tested to determine the status of their respective lock lines. They are tested in order starting with PLL V and finishing with BFO PLL. If a fault occurs as a result of these tests, the appropriate fault code and assembly number are displayed on the front panel.

5.5.2.9 Input Filter Test (Assembly A1)

Input Filter Assembly A1 will be tested next. This is done by testing the relay, the BITE oscillator, and front end filter.

First the input is tested for an overload condition. If an overload exists, then the test is terminated and an antenna overload message is displayed. If no overload exists, testing is continued.

The antenna relay is tested by energizing the relay, passing dc through it, and sampling the A1 dc detector to ensure that the signal path is complete. Sampling the A1 detector output (as well as the A2, A3, and A5 detector outputs) is done by an analog to digital converter (A/D) located on Control Board Assembly A14.

If this test fails, there will not be an immediate fault. The result is saved for future use during this test. The relay is then turned off using the relay control line and the BITE detector level is again tested. If a signal is still present, then the problem is in the relay or its associated control circuitry. If this is the case, a fault is reported indicating a relay failure.

If a fault condition is not detected, an RF test of the A1 assembly is performed by removing the dc relay test signal and activating the 100 kHz BITE oscillator. The BITE oscillator signal level at the output of the A1 assembly is -20 dBm. The A1 RF detector level is measured. If it is found that the output level is too low then the results of the relay test are checked. If the relay test also failed, then the fault is in the front end filter or the detector line to the A14 assembly. If the relay test passed, then the fault is in either the BITE oscillator or the RF detector. If the RF test is passed and the relay test failed, then the fault is either the relay or the dc detector.

5.5.2.10 First Converter Test (Assembly A2)

After the A1 assembly has been found to be operating correctly, First Converter Assembly A2 is tested. It should be pointed out that the BITE oscillator was left activated from the previous test and will be used as a signal source during the testing of this assembly. The AGC is set to OFF, the RF GAIN is set to maximum and the receiver is tuned to 100 kHz. The A2 DET line is now read by the A/D converter and the results tested to ensure the level is correct. If a fault occurs as a result of this test, the A2 assembly will be flagged as the faulty module and the appropriate fault code will be displayed.

5.5.2.11 Second Converter Test (Assembly A3)

If the First Converter is operating correctly then the Second Converter module is tested. AGC, RF GAIN, and BITE oscillator are in the same state as used in the testing of the First Converter. Since all conditions are set up, it is only necessary to measure the A3 detector level using the A/D converter and to verify the correct level. If the level is incorrect, the appropriate fault information will be displayed.

5.5.2.12 IF Filter Test (Assembly A4)

After it has been determined that the Second Converter is operating satisfactorily, IF Filter Assembly A4 can be tested. FSK filters will not be tested because of the wide variety of center frequencies and shifts available. The BITE test oscillator located on the A1 assembly will be disabled at this time. A signal generated by the first LO (via signal leakage through the First Converter A2 mixer) will be used. (The first LO signal is used to obtain better frequency accuracy for some of the narrow bandwidth filters that may be present in IF Filter Assembly A4.)

First the 16 kHz bypass path is tested to verify that a signal can be passed through the filter assembly amplifiers to the peak detector located on the input of IF/Audio Assembly A5. The 16 kHz bypass is selected and the level of the peak detector is read by the A/D converter. The results of this test are stored until after the USB filter is tested since, at this time, there could be a problem in either the A4 bypass circuitry or a problem in the A5 input peak detector.

To pinpoint any possible problem, the receiver will now be tuned to set the first LO to 40.454 MHz. This will generate a 1 kHz USB tone. USB filter (BW2) will be selected and the peak detector output read using the A/D converter. If a fault exists, then the results of the 16 kHz bypass test will be examined to pinpoint the fault. If the USB filter test passed but the bypass test indicated a fault, then the bypass path is flagged as the faulty circuit. If the USB filter test failed and the bypass path test passed, then the USB filter is identified as the faulty circuit. If both of these tests failed, then the fault is identified as being either the A5 peak detector or the A4 filter amplifiers and their associated circuitry. If the test results indicate that both are operating correctly, then testing the remaining filters installed in the A4 assembly continues.

The LSB filter (BW1) is tested by tuning the first LO to a frequency of 40.456 MHz and enabling the A4 LSB filter slot. A 1 kHz LSB tone is generated, detected by the A5 input peak detector, and measured by the A14 A/D converter. If a fault exists, the LSB filter is identified as the faulty circuit.

Next the CW filter slot (BW3) is tested. The first LO is tuned to 40.455 MHz and the CW filter slot is enabled. The level of the peak detector is read by the A/D converter. If the level monitored indicates that a problem exists, then the CW filter (BW3) is identified as being the faulty circuit.

The CW filter slot (BW4) is now tested. The same procedure is used to test this filter as was used to test BW3 CW filter. If a problem exists, then this CW filter (BW4) is identified as being the faulty circuit.

Filter slots 5, 6, and 7 may have a variety of filters installed. The only types of filters allowed in these slots are AM, FM, CW, or FSK. Since FSK filters will not be tested and AM, FM, and CW can all be tested at the same frequency, we only need to determine if a filter is present and whether or not it is an FSK type. Testing is identical to that of the CW filters, BW3, and BW4. If a problem exists in any of these filters, the appropriate fault message is displayed.

NOTE

The eight pole dip switch (S2) located on the A14 assembly must be set correctly for the above test to be performed correctly. This switch is set at the factory (based on the filter configuration of the A4 assembly) and should not be altered.

5.5.2.13 IF Audio Test (Assembly A5)

IF/Audio Assembly A5 is now tested to determine that the SSB, AM, and FM detectors are operating correctly. The A4 filter is set to select the 16 kHz bypass path. The AGC speed is set to MEDIUM, the mode is set to USB, and the A1 assembly BITE test oscillator is enabled.

The receiver is first tuned to 104.000 kHz. Since the BITE oscillator has a frequency of 100 kHz, a 4 kHz USB tone will result. The second IF AMP GAIN is tested by measuring the AGC voltage through the A/D converter. If the level is incorrect, an AGC fault is displayed on the front panel of the receiver. If this level is satisfactory, then the product detector is tested. The BITE test oscillator is disabled and the receiver is tuned to 4 kHz. The results of this test are stored since there could be a problem in either the line audio circuits or the USB product detector (if a fault indication is detected).

The AM test is now performed. With the receiver tuned to 4 kHz, the receiver mode is set to AM. The 16 kHz bypass is again used for this test. To simulate an AM signal, the receiver will be tuned repetitively from 4 kHz to 100 kHz using LO No. 2 leakage as a signal source. The line audio level is measured to verify that the AM detector is operational. The results of this test and those of the SSB test are compared to determine where possible faults may have occurred. Table 5-3 shows the results of this test and that of the SSB test.

Table 5-3. AM and SSB Test Results and Fault Locations

AM and SSB Test Results	Fault Location
If AM passed and SSB passed	no fault
If AM passed and SSB failed	product detector fault
If AM failed and SSB passed	AM detector fault
If AM failed and SSB failed	line audio fault

The next test concerned with the A5 assembly is the FM detector test. The receiver is set to FM mode and tuned to a frequency of 5 kHz. The receiver will then be tuned from +5 kHz to -5 kHz repetitively to simulate a FM signal using LO No. 1 leakage as a signal source. The line audio will be read through the A/D converter. If a problem exists, the appropriate fault message is displayed on the front panel of the receiver.

5.5.2.14 ISB Test (Assembly A18, If Installed)

ISB option assembly A18 (if installed) is now tested to determine that the IF Peak Detector, ISB AGC, and ISB Line Audio Detector are operating correctly.

Filter Assembly A4 is first set to select the LSB filter. Next, the receiver mode is set to ISB and the RF GAIN is set to maximum. The 100 kHz bite oscillator located on Input Filter Assembly A1 is now activated and the receiver is tuned to 95 kHz (resulting in a LSB frequency of 5 kHz).

Now the ISB Peak Detector level is sampled to determine whether an inband ISB signal has been found (level greater than 1 volt dc). If this level is not found, the frequency of the receiver is increased 200 Hz and the detector level is checked again. This process is repeated until the correct level is found or until the receiver frequency is greater than 115 kHz.

If the frequency is greater than 115 kHz, the no inband tone was found so it is assumed that the input peak detector has failed or the signal path between Filter Assembly A4 and the A18 ISB Assembly has been interrupted. If this is true, the fault code for the A18 Peak Detector will be displayed on the receiver front panel and no further testing of the assembly will take place.

If the inband tone was found; the frequency is increased by 1.5 kHz, placing the tone in the center of the LSB filter.

Once the receiver is tuned, the peak detector, AGC detector, and line audio detector levels are measured to verify their operation. If any of these are found to be at an improper level, the appropriate fault code will be displayed on the receiver front panel and all further receiver testing is aborted.

If the three levels are found to be correct, then the assembly is considered to be functioning correctly.

5.5.2.15 LCU Test (Assembly A17)

The last thing to be tested during self-test is Remote Control Assembly A17. The information used to control these tests is contained within the remote control assembly firmware. If it is determined that the remote control assembly is installed, the remote control assembly will test the UART, the LCU ROM (U7), and the RS-422 interface. If any of these are found to be at fault, then the corresponding fault information is displayed on the front panel. The LCU also reports, to the remote site, any self-test pass/fail conditions that may occur as a result of the TEST function being performed.

Upon completion of the self-test, if no fault has occurred, a – – – TEST PASSED – – – message is displayed indicating to the operator that the radio is operating satisfactorily.

5.5.3 Self Diagnostics Sequence Summary

The RF-590 self diagnostics are done in the order of assembly importance. If a fault is discovered during testing, this failure must be corrected before the remaining tests are attempted.

The order of testing from the first to last test is shown in table 5-4.

Table 5-4. Self Diagnostics Sequence Summary

1.	ROM Test – Assembly A14
2.	RAM Test – Assembly A14
3.	Output Port Test – Assembly A14
	3.1 8155 Ports B, C
	3.2 8255 Port A

Table 5-4. Self Diagnostics Sequence Summary (Cont.)

4. Serial Data Tests 4.1 Assembly A14 4.2 Assembly A11 4.3 Assembly A7 4.4 Assembly A10 4.5 Assembly A8
5. Reference Generator Tests – Assembly A12 5.1 40 MHz Phase locked loop 5.2 1 MHz Reference 5.3 800 kHz Reference
6. Phase Locked Loops 6.1 Assembly A10 - PLL V 6.2 Assembly A9 - PLL IV 6.3 Assembly A8 - PLL III 6.4 Assembly A7 - PLL II 6.5 Assembly A6 - PLL I 6.6 Assembly A11 - BFO PLL
7. A/D Converter Test – Assembly A14 7.1 Conversion Timing Test 7.2 +5 Reference Measurement 7.3 Gnd Reference Measurement
8. Input Filter Test – Assembly A1 8.1 Antenna overload test 8.2 Dc signal test 8.2.1 Relay closed 8.2.2 Relay open

Table 5-4. Self Diagnostics Sequence Summary (Cont.)

8.3 RF signal test **NOTE** If both tests 8.2.1 and 8.3 fail then it is assumed that the filter is faulty.
9. First Converter Test – Assembly A2
10. Second Converter Test – Assembly A3
11. IF Filter Tests – Assembly A4 11.1 16 kHz Bypass Test 11.2 USB Filter Test **NOTE** If both tests 11.1 and 11.2 fail then it is assumed that either the IF amplifier or the A5 assembly peak detector is faulty. 11.3 LSB Filter Test 11.4 CW Filter Test 11.5 CW Filter Test 11.6 Special Filter 5 Test 11.7 Special Filter 6 Test 11.8 Special Filter 7 Test **NOTE** Tests 11.6, 11.7, and 11.8 are done only if filters are installed and if they are not FSK filters.
12. IF/Audio Test – Assembly A5 12.1 AGC Test 12.2 SSB Noise Test 12.3 SSB Signal Test

Table 5-4. Self Diagnostics Sequence Summary (Cont.)

12.4 AM Noise Test 12.5 AM Signal Test **NOTE** If both test 12.3 and 12.5 fail then it is assumed that the line audio detector is faulty. 12.6 FM Noise Test 12.7 FM Signal Test
13. ISB Test – Assembly A18 (If Installed) 13.1 Peak Detector 13.2 AGC Test 13.3 Line Audio Detector
14. Remote (LCU) Test – Assembly A17 (If Installed) 14.1 PROM Test 14.2 Communications Test 14.3 Interface Test

5.6 RECEIVER PERFORMANCE TEST PROCEDURES

Table 5-5 shows tests used to verify RF-590 operation.

Table 5-5. RF-590 Test Procedures

Test	Paragraph
Local Control Function Test	2.7
Sensitivity	5.6.1

Table 5-5. RF-590 Test Procedures (Cont.)

Test	Paragraph
Audio Output Level and Distortion	5.6.2
AGC Range	5.6.3
Ultimate Quieting	5.6.4
IF Filter Selectivity	5.6.5

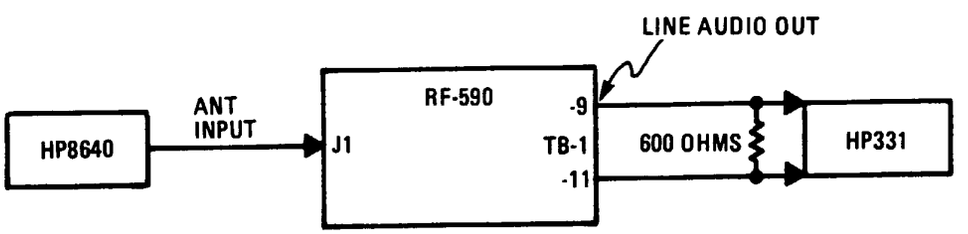
5.6.1 Sensitivity Test

The following test equipment is required to perform this test.

- HP-8640B Signal Generator
- HP-331A Audio Distortion Analyzer
- 600 Ohm Feedthrough Termination

The following steps describe the sensitivity test procedure.

a. Connect equipment as shown in figure 5-1.



590-44(1)

Figure 5-1. Sensitivity Test Setup

b. Initially set receiver's AGC to OFF and RF GAIN to maximum.

c. Perform steps d through f for each of the modes and bandwidths listed in table 5-6.

d. Set generator for a minimum RF output.

e. Adjust audio distortion analyzer sensitivity for a convenient reference indication.

f. Adjust generator output until the audio output rises 10 dB above the reference noted in step e. Record the signal generator output level in table 5-6. Note that this value must be no greater than the maximum allowable 10 dB $\frac{S+N}{N}$ sensitivity listed.

NOTE

Generator frequencies may be varied within the passband range to obtain a peak audio output in the channel being tested.

NOTE

In AM mode, it will be necessary to set the signal generator for 50 percent modulation at the modulation frequency indicated. Increase carrier power until a 10 dB difference above the reference level is obtained between modulation OFF and modulation ON.

NOTE

In FM mode, set the generator for 4.7 kHz deviation at the modulation frequency indicated. Increase carrier power until a 17 dB difference is obtained on the audio voltmeter between modulation OFF and modulation ON.

Table 5-6. Sensitivity Test Reports

Mode	BW kHz	Radio Frequency MHz	Generator Frequency MHz	Modulation Frequency kHz	*Maximum 10 dB $\frac{S+N}{N}$ Sensitivity uVrms	Measured 10 dB $\frac{S+N}{N}$ Sensitivity uVrms
LSB	3.2	2.000000	1.999000	–	.35	_____
		16.000000	15.999000	–	.35	_____
		29.999999	29.999000	–	.35	_____
USB	3.2	2.000000	2.001000	–	.35	_____
		16.000000	16.001000	–	.35	_____
		29.999999	30.001000	–	.35	_____
CW	.3	2.000000	2.000150	–	.15	_____
		16.000000	16.000150	–	.15	_____
		29.999999	30.000150	–	.15	_____
CW	1.0	2.000000	2.000500	–	.25	_____
		16.000000	16.000500	–	.25	_____
		29.999999	30.000500	–	.25	_____

Table 5-6. Sensitivity Test Reports (Cont.)

Mode	BW kHz	Radio Frequency MHz	Generator Frequency MHz	Modulation Frequency kHz	*Maximum 10 dB $\frac{S+N}{N}$ Sensitivity uVrms	Measured 10 dB $\frac{S+N}{N}$ Sensitivity uVrms
AM	3.2	2.000000 16.000000 29.999999	2.000000 16.000000 29.999999	1.0 1.0 1.0	1.25 1.25 1.25	_____ _____ _____
AM	6.0	2.000000 16.000000 29.999999	2.000000 16.000000 29.999999	1.0 1.0 1.0	1.5 1.5 1.5	_____ _____ _____
FM	16.0	2.000000 16.000000 29.999999	2.000000 16.000000 29.999999	1.0 1.0 1.0	2.0 2.0 2.0	_____ _____ _____

* = These numbers double when the RF-596-02 Preselector option is installed.

5.6.2 Audio Output Level and Distortion Test

The following test equipment is required to perform this test.

- HP-8640B Signal Generator
- HP-331A Distortion Analyzer
- 600 Ohm Feedthrough Termination
- 8 Ohm 5 Watt Termination

Use the following procedures to check line output, headphone output, and speaker output.

5.6.2.1 Line Output Check

To check the line input proceed as follows:

a. Set signal generator to -20 dBm, 2.001500 MHz. Set receiver to 2.000000 MHz, AGC to MEDIUM, Mode to USB, and RF GAIN to maximum.

b. Connect equipment as shown in figure 5-2.

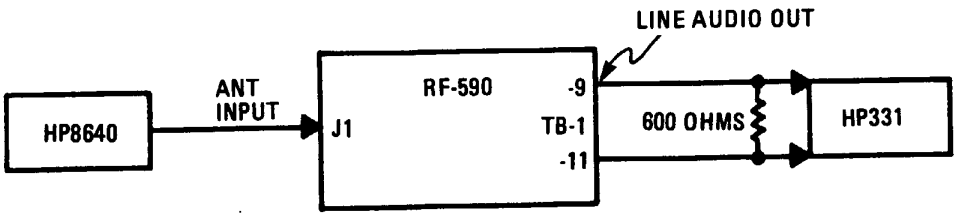


Figure 5-2. Line Audio Test Setup

c. Measure line audio output level. Level must be adjustable from -16 dBm (.123 Vrms) to +10 dBm (2.45 Vrms) (.1 mW to 10 mW). Record range in table 5-7.

Table 5-7. Audio Output Level and Distortion Test Report

Test	Output Level Measured Vrms	Output Level Limits Vrms	Distortion Measured dBc	Distortion Limits dBc
Line Audio		.123 to 2.45 Minimum		-40
Headphone Audio		2.45 Minimum		-40
Speaker Audio		4.0 Minimum		-26

d. Set line audio level to 2.45 Vrms. Measure total harmonic distortion (THD). THD must be at least -40 dBc (1% maximum). Record in table 5-7.

e. Reset line audio level to .775 Vrms (0 dBm). Check that the RF-590 front panel meter indicates 0 dBm ±2 dB.

5.6.2.2 Headphone Output Check

To check the headphone output proceed as follows:

a. Set signal generator to -20 dBm, 2.001500 MHz. Set receiver to 2.000000 MHz, AGC to MEDIUM, Mode to USB, and RF GAIN to maximum.

b. Connect equipment as shown in figure 5-3.

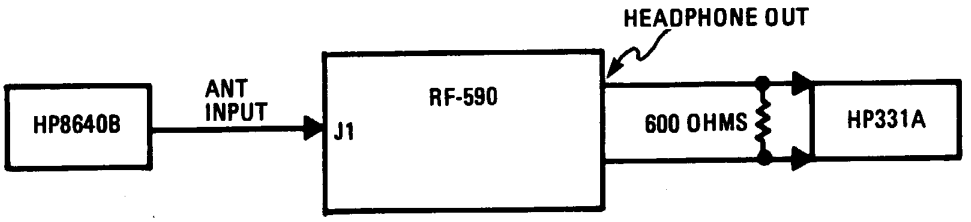


Figure 5-3. Phone Audio Test Setup

c. Set speaker to OFF. Adjust AF GAIN control for maximum output. Headphone output level must be 2.45 Vrms (10 mV) minimum. Record in table 5-7.

d. Measure Total Harmonic Distortion at 2.45 Vrms output. THD must be at least -40 dBc (1% maximum). Record in table 5-7.

e. Readjust AF GAIN to minimum.

5.6.2.3 Speaker Output Check

To check speaker output proceed as follows:

a. Set signal generator to -20 dBm, 2.00150 MHz. Set receiver to 2.000000 MHz, AGC to MEDIUM, Mode to USB, and RF GAIN to maximum.

b. Connect equipment as shown in figure 5-4.

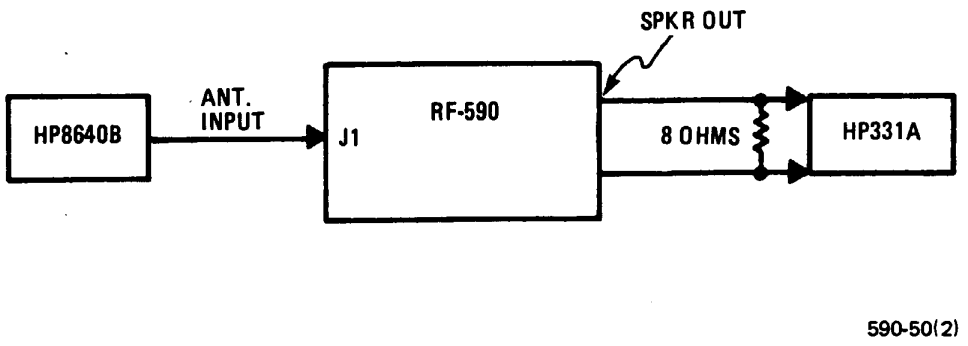


Figure 5-4. Speaker Audio Test Setup

NOTE

It will be necessary to disconnect the audio lines to the speaker and connect them to the 8 ohm load to perform this test.

c. Set speaker to ON, and adjust AF GAIN to maximum. Speaker audio output level must be 4.0 Vrms (2.0 W) minimum. Record in table 5-7.

d. Measure total harmonic distortion (THD) at 4.0 Vrms output. THD must be at least -26 dBc (5% maximum). Record in table 5-7.

e. Set speaker to OFF, AF GAIN to minimum. Disconnect 8 ohm load and reconnect speaker.

5.6.3 AGC Range

The following test equipment is required to perform this test.

- HP-8640B Signal Generator
- HP-331A Audio Distortion Meter
- 600 Ohm Feedthrough Termination

Use the following procedures to perform the AGC range test.

a. Connect equipment as shown in figure 5-5.

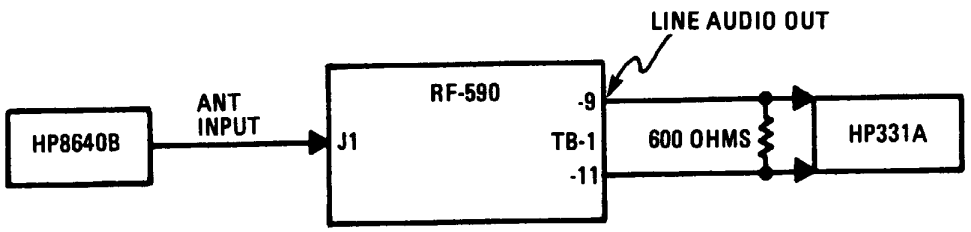


Figure 5-5. AGC Range Test Setup

b. Set signal generator to 10.001500 MHz and RF output level at 2 uVrms.

c. Set AGC to MEDIUM, RF GAIN to maximum, Mode to USB, Receive Frequency to 10.000000 MHz, BFO to 0.00 kHz, and Line Audio Output to 0 dBm.

d. Set a convenient reference level on the distortion analyzer, and then increase signal generator output to 1 Vrms. The audio output level should not increase by more than 3 dB. Record level change below.

Total Audio Output Level Change: _____ dB (3 dB maximum)
(RF input level 2 uVrms to 1 Vrms)

5.6.4 IF Filter Selectivity

The following test equipment is required for this test:

- HP-8640B Signal Generator
- Boonton Model 91-H RF Millivoltmeter with 50 ohm adapter.
- HP-5383A Frequency Counter

Use the following procedures to verify filter IF response.

a. Initially set receiver to 10.000,000 MHz, AGC to OFF, BFO to 0.00 kHz, and MODE to USB. Connect equipment as shown in figure 5-6.

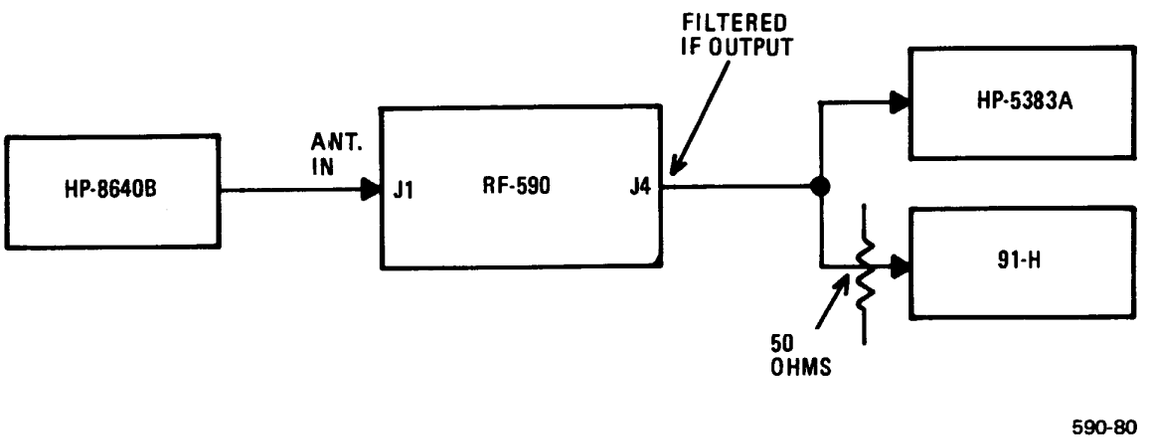


Figure 5-6. IF Filter Selectivity Test Setup

b. Set signal generator frequency f_o to 10.0015 MHz. Adjust generator output to set a convenient millivoltmeter reference level in the generator's -110 dB range (i.e., below the receiver's AGC threshold).

c. Vary the generator frequency ±10 kHz and note the IF output -3 dB roll-off frequencies. (Note that only one major, distinct peaked response should occur for any selected filter. However there may be some passband ripple.) Calculate the -3 dB bandwidth as the difference between these frequencies. Record in table 5-8.

d. Note the passband ripple as the difference in IF output maxima and minima values between the -3 dB frequencies. Check (√) table 5-9 if ripple ≤3 dB.

e. Repeat steps b through d for the generator frequencies (f_o), IF filter modes, and BWs listed in table 5-8.

Table 5-8. IF Filter Response Test Report

Generator Reference Level Frequency f_o MHz	Mode	Filter Bandwidth, kHz		Passband Ripple	
		(Minimum)	Measured	Maximum dB	Measured dB
10.00150	USB	2.8		3	
9.99850	LSB	2.8		3	
10.0000	CW	.30		3	
10.0000	CW	1.0		3	
10.0000	AM	3.2		3	
10.0000	AM	6.8		3	
10.0000	AM	16		3	

5.7 COMPONENT DATA SHEETS

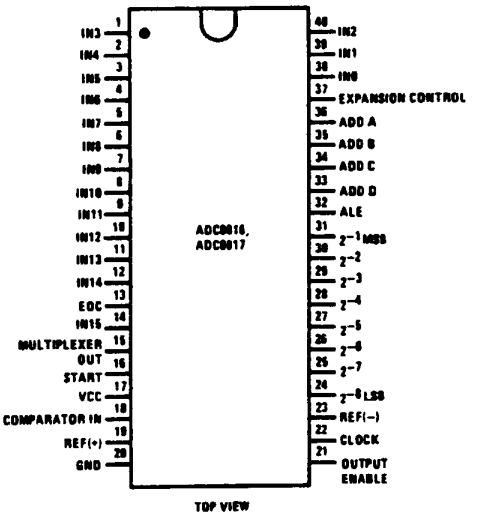
This section contains any applicable data sheets for the RF-590. They can be used for reference purposes and are listed alphabetically.

ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

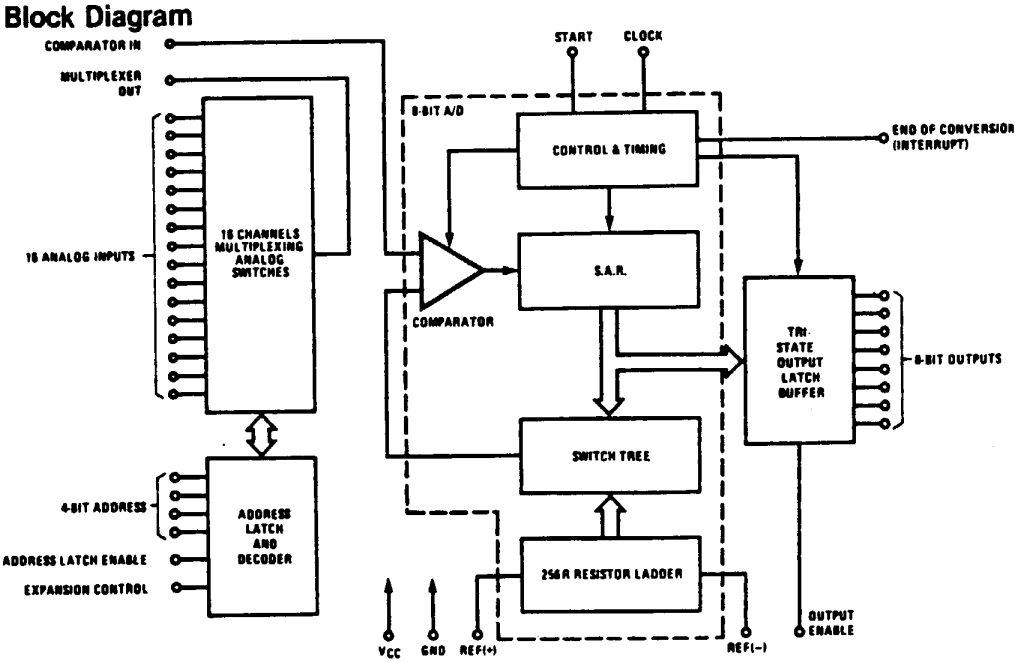
The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

Dual-In-Line Package



TOP VIEW

Block Diagram



Am26LS31

Quad High Speed Differential Line Driver

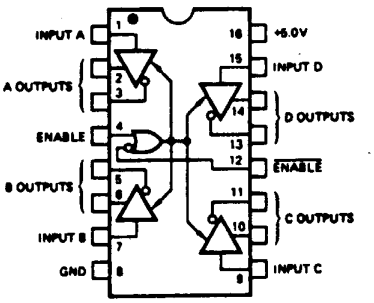
FUNCTIONAL DESCRIPTION

The Am26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The Am26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. Is is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

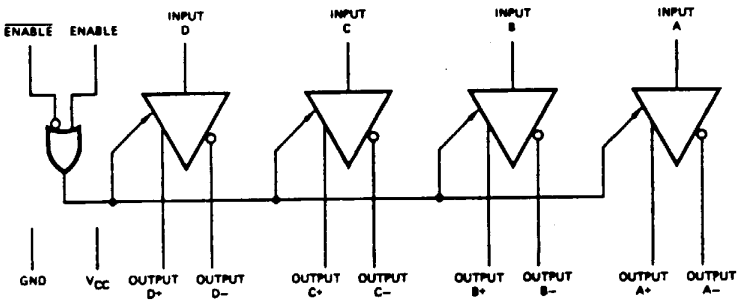
The circuit provides an enable and disable function common to all four drivers. The Am26LS31 features 3-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The Am26LS31 is constructed using advanced low-power Schottky processing.

CONNECTION DIAGRAM
(Top View)



LOGIC DIAGRAM



Am26LS33

FUNCTIONAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

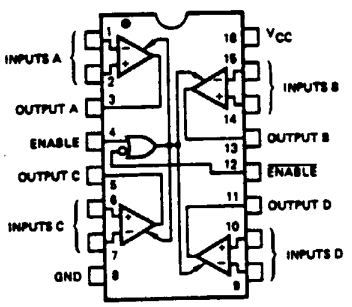
The Am26LS32 features an input sensitivity of 200mV over the input voltage range of ±7V.

The Am26LS33 features an input sensitivity of 500mV over the input voltage range of ±15V.

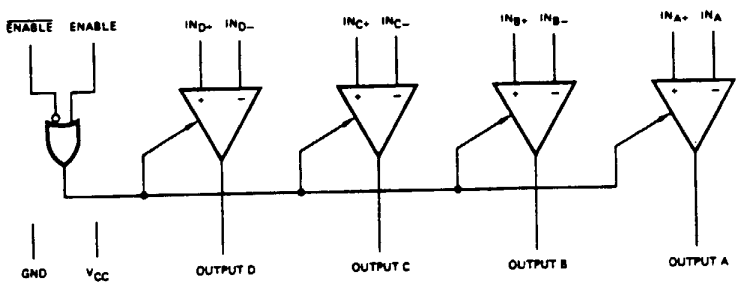
The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

CONNECTION DIAGRAM
Top View



LOGIC DIAGRAM



CA555E

Timer

The RCA-CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free-running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the waveform signal, and the output of these circuits can source or sink up to a 200-milliampere current or drive TTL circuits.

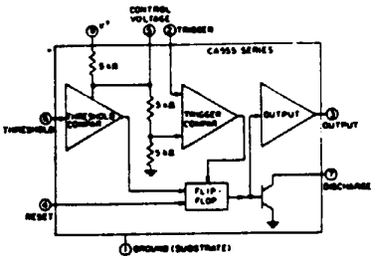


Fig. 1 – Functional diagram of the CA555 series.

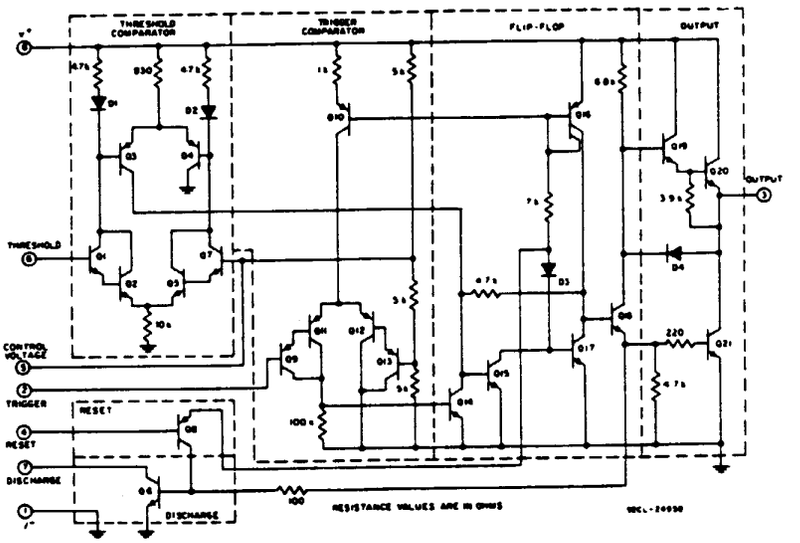
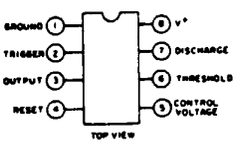
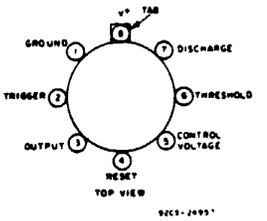


Fig. 2 – Schematic diagram of the CA555 and CA555C.



a. MINI-DIP plastic package
TO-5 style package with formed leads



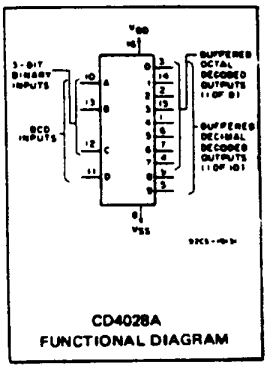
b. TO-5 style package

Fig. 3 – Terminal assignment diagrams.

CD4028A Types
COS/MOS
BCD-to-Decimal Decoder

The RCA-CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse-shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low. If unused, the D input must be connected to V_{SS}. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).



CD4028A
FUNCTIONAL DIAGRAM

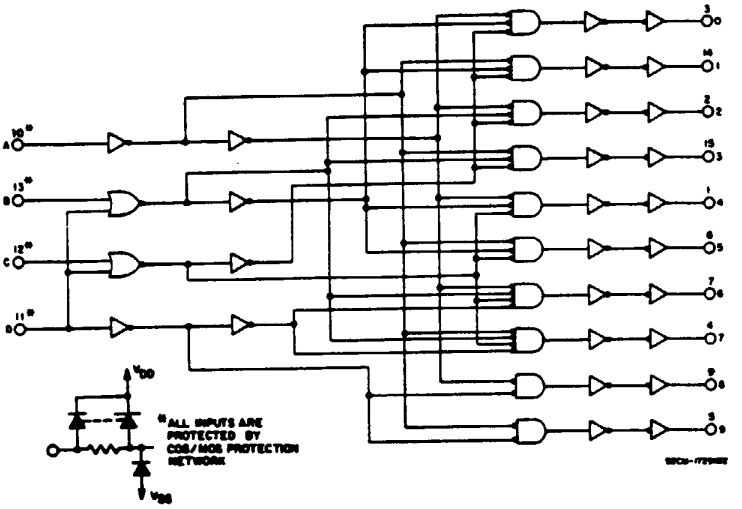


TABLE I – TRUTH TABLE

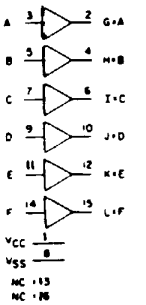
D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	*
0	0	0	1	0	1	0	0	0	0	0	0	0	0	
0	0	1	0	0	0	1	0	0	0	0	0	0	0	
0	0	1	1	0	0	0	1	0	0	0	0	0	0	
0	1	0	0	0	0	0	0	1	0	0	0	0	0	
0	1	0	1	0	0	0	0	0	1	0	0	0	0	
0	1	1	0	0	0	0	0	0	0	1	0	0	0	
0	1	1	1	0	0	0	0	0	0	0	1	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	1	0	
1	0	0	1	0	0	0	0	0	0	0	0	0	1	
1	0	1	0	0	0	0	0	0	0	0	0	1	0	**
1	0	1	1	0	0	0	0	0	0	0	0	0	1	
1	1	0	0	0	0	0	0	0	0	0	0	1	0	
1	1	0	1	0	0	0	0	0	0	0	0	0	1	
1	1	1	0	0	0	0	0	0	0	0	0	1	0	
1	1	1	1	0	0	0	0	0	0	0	0	0	1	

* WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

** EXTRAORDINARY STATES

CD4050A
COS/MOS Hex Buffer/Converters

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, V_{OL} ≥0.4 V, and I_{ON}≥3.2 mA.)



CD4050A

CD4053B

COS/MOS Analog Multiplexers/Demultiplexers

RCA-CD4051B, CD4052B, and CD4053B analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if V_{DD}-V_{SS} = 3 V, a V_{DD}-V_{EE} of up to 13 V can be controlled; for V_{DD}-V_{EE} level differences above 13 V, a V_{DD}-V_{SS} of at least 4.5 V is required). For example, if V_{DD} = +5 V, V_{SS} = 0, and V_{EE} = −13.5 V, analog signals from −13.5 V to +4.5 V can be controlled by digital inputs of 0 to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are off.

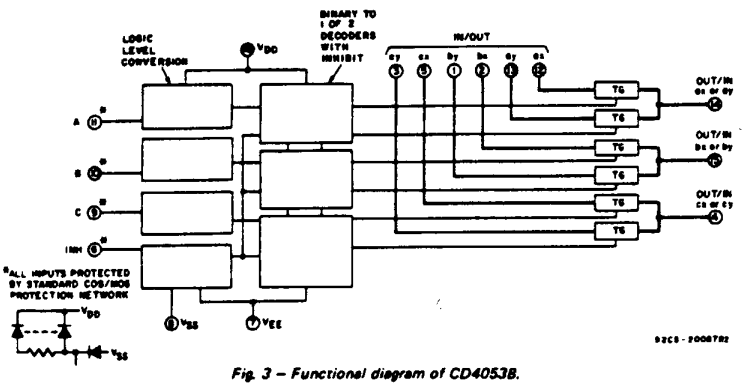
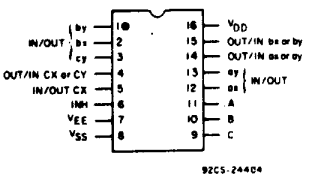


Fig. 3 – Functional diagram of CD4053B.



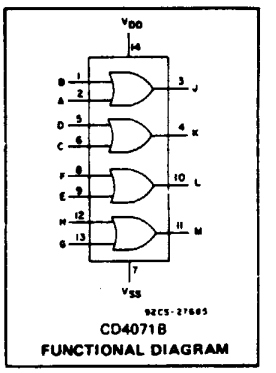
CD4053B

Terminal Assignment

CD4071B

COS/MOS QUAD 2-INPUT OR GATE

The RCA-CD4071B, CD4072B, and CD4075B OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of COS/MOS gates. The CD4071, CD4072, and CD4075 types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages(E suffix),and in chip form (H suffix).



CD4071B
FUNCTIONAL DIAGRAM

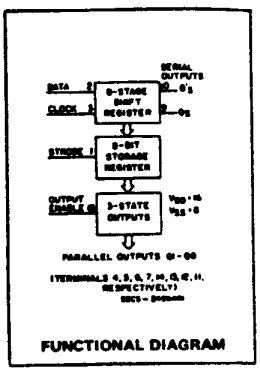
CD4094B

COS/MOS 8-Stage Shift-and-Store Bus Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.



FUNCTIONAL DIAGRAM

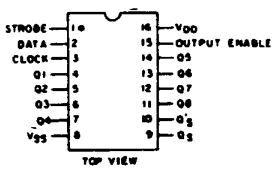


Fig. 1 – Terminal assignment.

TRUTH TABLE

CL^	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	QN	QS*	Q'S
⌐	0	X	X	OC	OC	Q7	NC
⌐	0	X	X	OC	OC	NC	Q7
⌐	1	0	X	NC	NC	Q7	NC
⌐	1	1	0	0	QN-1	Q7	NC
⌐	1	1	1	1	QN-1	Q7	NC
⌐	1	1	1	NC	NC	NC	Q7

^ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit

Logic 1 ≡ High
Logic 0 ≡ Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output

CD4098B Types

COS/MOS Dual Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

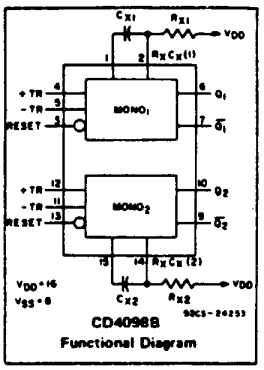
The RCA-CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X.

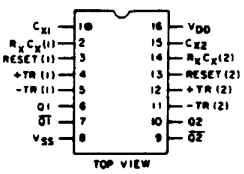
Leading-edge-triggering (+TR) and trailing edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to −TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (−TR) is used.

The time period (T) for this multivibrator can be approximated by: $T_X = \frac{1}{2} R_X C_X$ for $C_X \geq 0.01\ \mu F$.



CD4098B
Functional Diagram



TERMINALS 1, 8, 15 ARE ELECTRICALLY CONNECTED INTERNALLY

TERMINAL ASSIGNMENT

CD4514B

COS/MOS 4-Bit Latch/4-to-16 Line Decoders

High-Voltage Types (20-Volt Rating)
CD4514B Output "High" on Select

The RCA-CD4514B and -CD4515B consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD4514B) or 1(CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

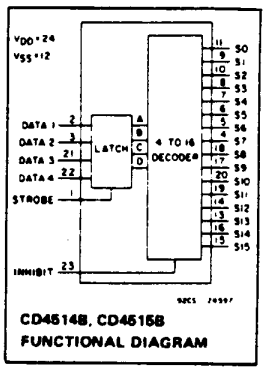
These devices are similar to industry types MC14514 and MC14515.

The CD4514B and CD4515B types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in line plastic packages (E suffix), and in chip form (H suffix).

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DECODER INPUTS				SELECTED OUTPUT CD4514B = Logic 1 (High) CD4515B = Logic 0 (Low)
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514B All Outputs = 1, CD4515B

X = Don't Care Logic 1 = high Logic 0 = low



CD4514B, CD4515B
FUNCTIONAL DIAGRAM

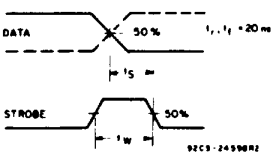
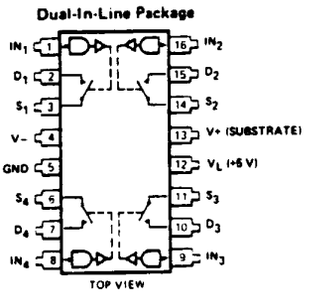


Fig. 14 — Waveforms for setup time and strobe pulse width.

DG211
Quad Monolithic SPST CMOS Analog Switch

The DG211 is a 4-channel single pole single throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0 V to 0.8 V) the switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make. Logic inputs can directly connect to op-amp output swings.

PIN CONFIGURATION



LOGIC	SWITCH
0	ON
1	OFF

SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

HM-6516

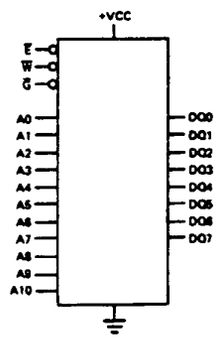
2K x 8 CMOS RAM

Description

The HM-6516 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, and also give fast access times.

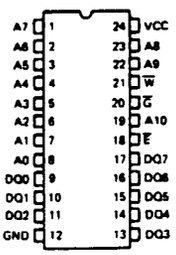
The HM-6516 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design, and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus, such as the 8085. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independant of the chip enable.

Logic Symbol



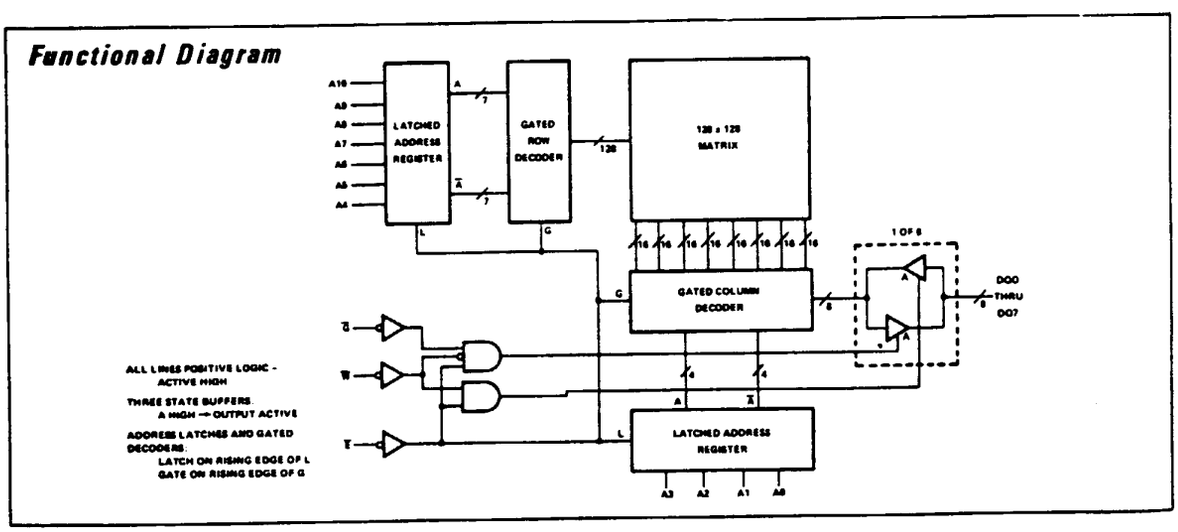
Pinout

TOP VIEW



A	Address Input
DQ	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable

Functional Diagram



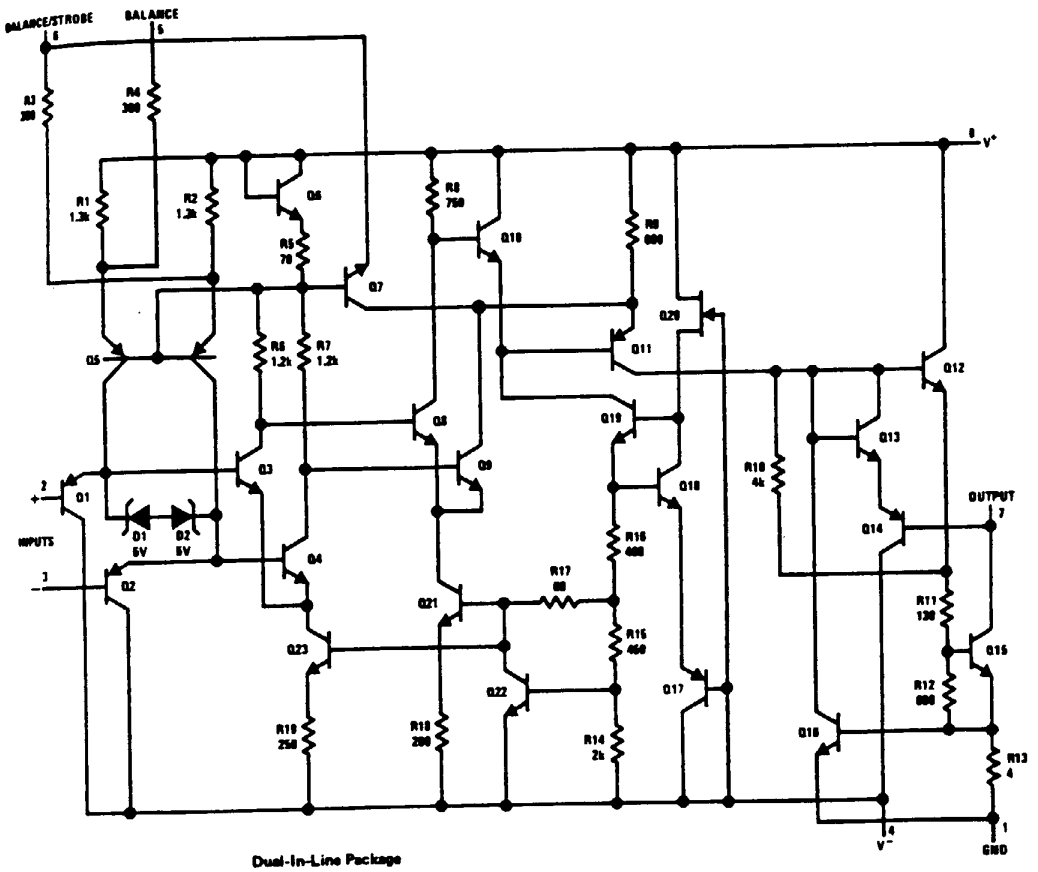
LM211 Voltage Comparator

General Description

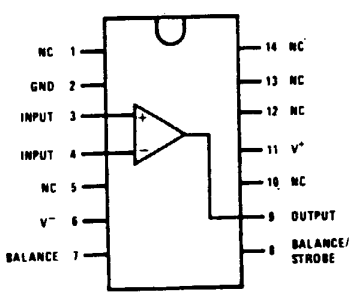
The LM111 and LM211 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA. Outstanding characteristics include:

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Both the inputs and the outputs of the LM111 or the LM211 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed.



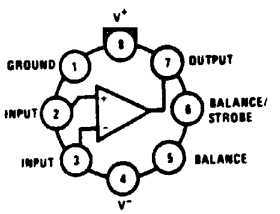
Dual-In-Line Package



Note: Pin 6 connected to bottom of package.

TOP VIEW

Metal Can Package



NOTE: Pin 4 connected to case.

TOP VIEW

LM324
Low Power Quad Operational Amplifiers

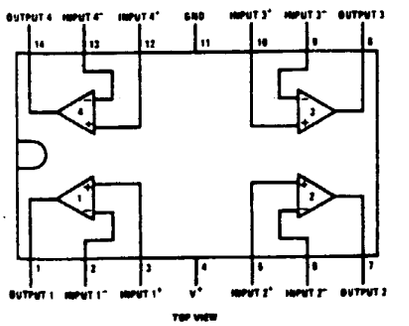
General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

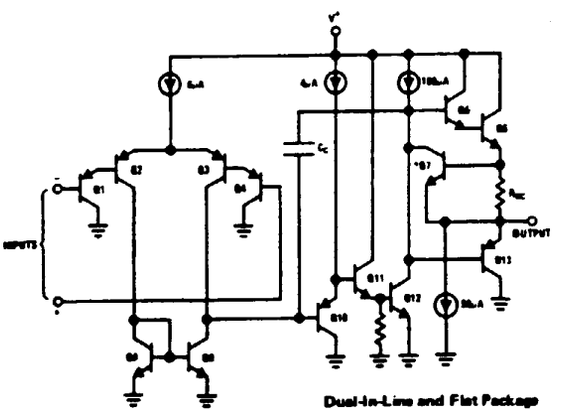
Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Connection Diagram

Dual-In-Line and Flat Package



Schematic Diagram (Each Amplifier)



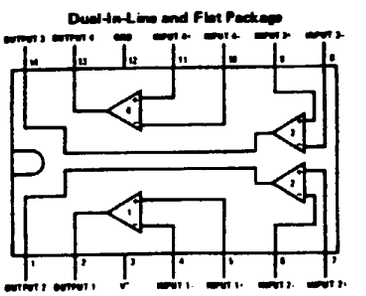
LM339
Low Power Low Offset Voltage Quad Comparators

General Description

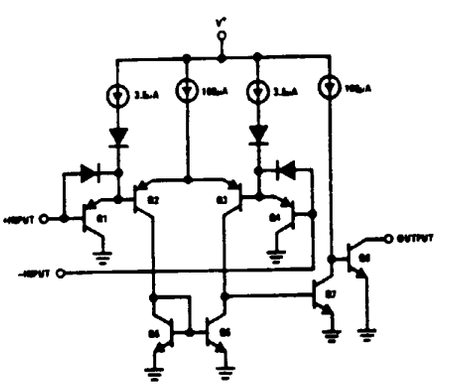
The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic– where the low power drain of the LM339 is a distinct advantage over standard comparators.

Dual-In-Line and Flat Package



Schematic and Connection Diagrams

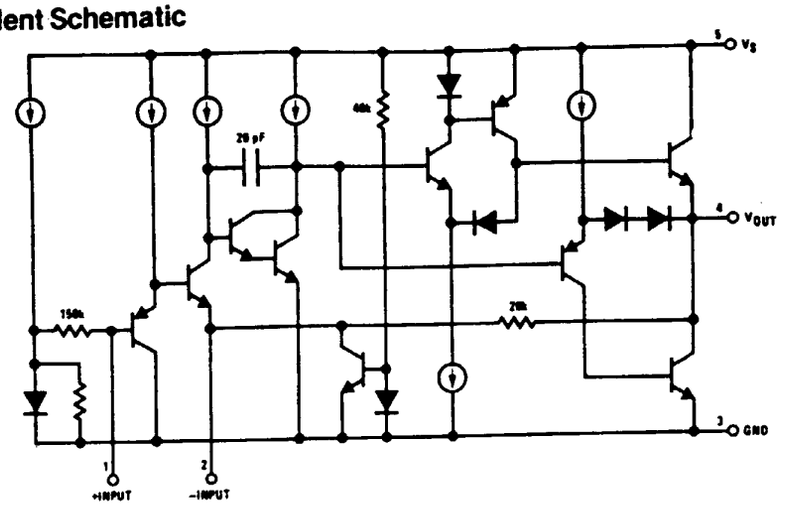


LM383/LM383A 8 Watt Audio Power Amplifier

General Description

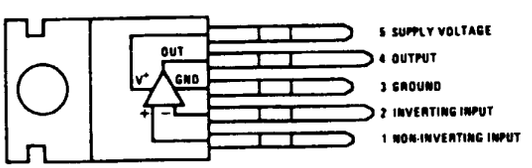
The LM383 is a high power amplifier. High current capability (3.5A) enables the device to drive low impedance loads with low distortion. The LM383 is current limited and thermally protected. High voltage protection is available (LM383A) which enables the amplifier to withstand 40V transients on its supply. The LM383 comes in a 5-pin TO-220 package.

Equivalent Schematic



Connection Diagram

TO-220 Plastic Package



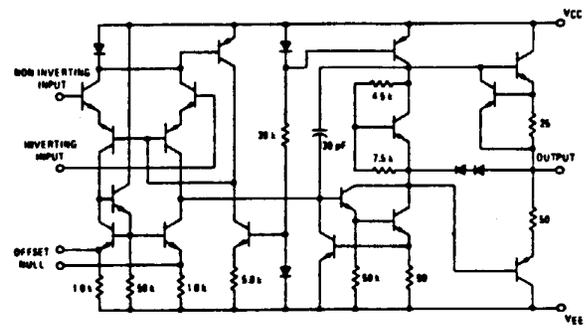
LM1458
Dual Operational Amplifier/Buffer

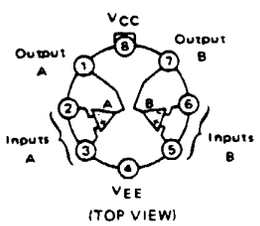
general description

The LM1558 and the LM1458 are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent. Features include:

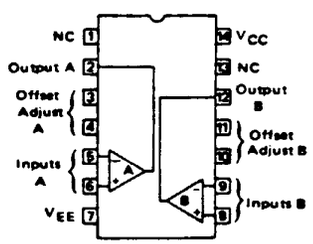
- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead TO-5 and 8-lead mini DIP
- No latch up when input common mode range is exceeded

EQUIVALENT CIRCUIT SCHEMATIC





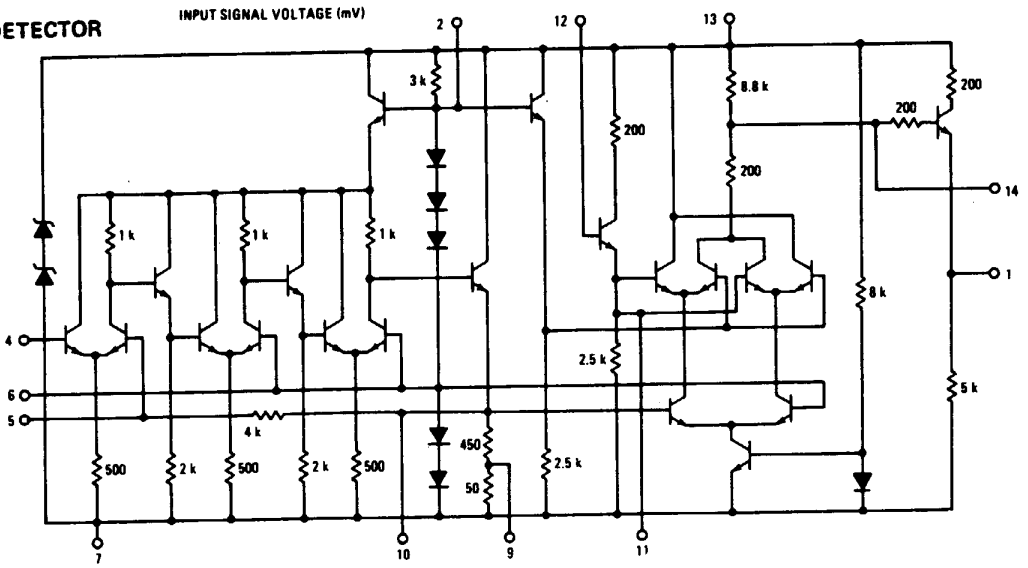
(TOP VIEW)



MC1357

QUADRATURE DETECTOR

FIGURE 1 – CIRCUIT SCHEMATIC



- A Direct Replacement for the ULN2111A
- Greatly Simplified FM Demodulator Alignment

Typical Performance:
2 Watts Output
2% Distortion
250 μV Sensitivity (3 dB Lim.)

C1 = 120 pF
L1 = 14 μH
R1 = 20 kΩ
Q = 30

MC1458

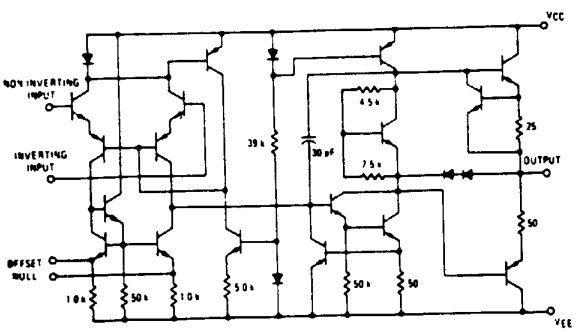
- Excellent Performance at V_{CC} = 8.0 Vdc

DUAL OPERATIONAL AMPLIFIERS

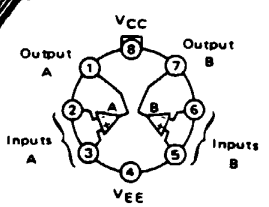
. . . designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- Low-Power Consumption
- No Latch Up
- Low Noise Selections Offered – N Suffix

EQUIVALENT CIRCUIT SCHEMATIC



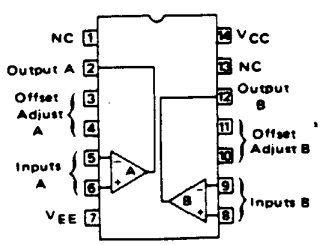
G SUFFIX
METAL PACKAGE
CASE 601



(TOP VIEW)

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P2 SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1458,MC1458C,MC1458N)



MC1488

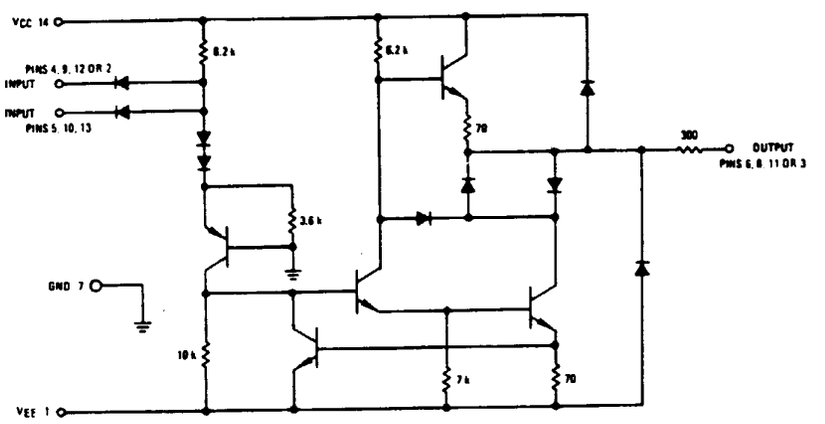
QUAD LINE DRIVER

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

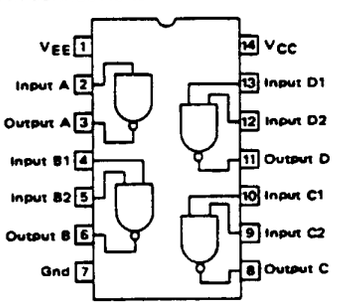
Features:

- Current Limited Output
  ±10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



PIN CONNECTIONS

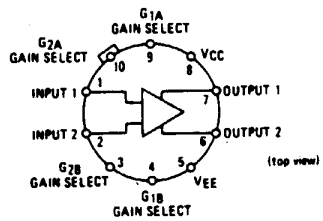


MC1733

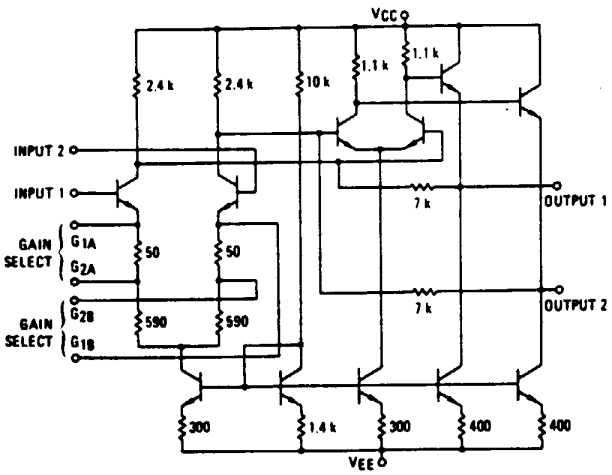
DIFFERENTIAL VIDEO AMPLIFIER

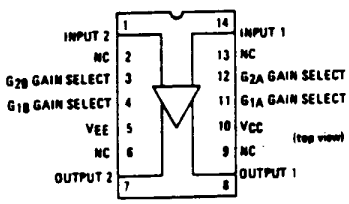
. . . a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

- Bandwidth – 120 MHz typical @ A_{vd} = 10
- Rise Time – 2.5 ns typical @ A_{vd} = 10
- Propagation Delay Time – 3.6 ns typical @ A_{vd} = 10



EQUIVALENT CIRCUIT SCHEMATIC



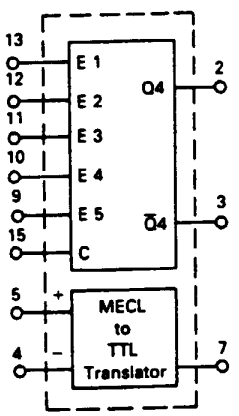


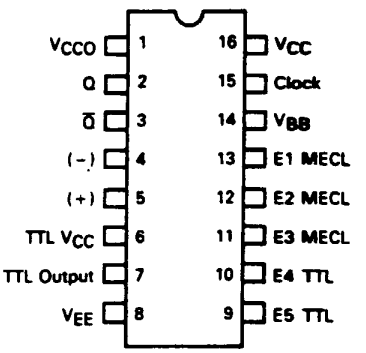
MC12013

TWO-MODULUS PRESCALER

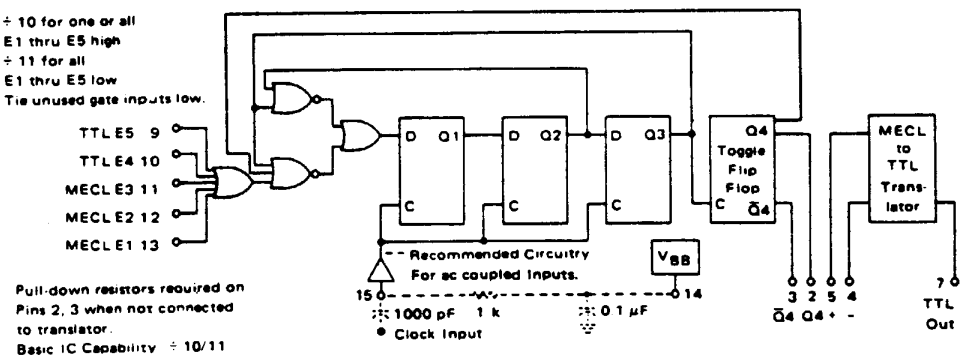
These devices are two-modulus prescalers which will divide by 5 and 6, 8 and 9, and 10 and 11, respectively. A MECL-to-TTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

LOGIC DIAGRAM





V_{CCO} = pin 1
V_{CC} = pin 16
V_{EE} = pin 8



MC14094B

8-STAGE SHIFT/STORE REGISTER WITH THREE-STATE OUTPUTS

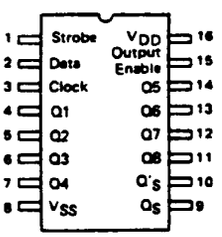
The MC14094B combines an 8-stage shift register with a data latch for each stage and a three-state output from each latch.

Data is shifted on the positive clock transition and is shifted from the seventh stage to two serial outputs. The Q_S output data is for use in high-speed cascaded systems. The Q'_S output data is shifted on the following negative clock transition for use in low-speed cascaded systems.

Data from each stage of the shift register is latched on the negative transition of the strobe input. Data propagates through the latch while strobe is high.

Outputs of the eight data latches are controlled by three-state buffers which are placed in the high-impedance state by a logic Low on Output Enable.

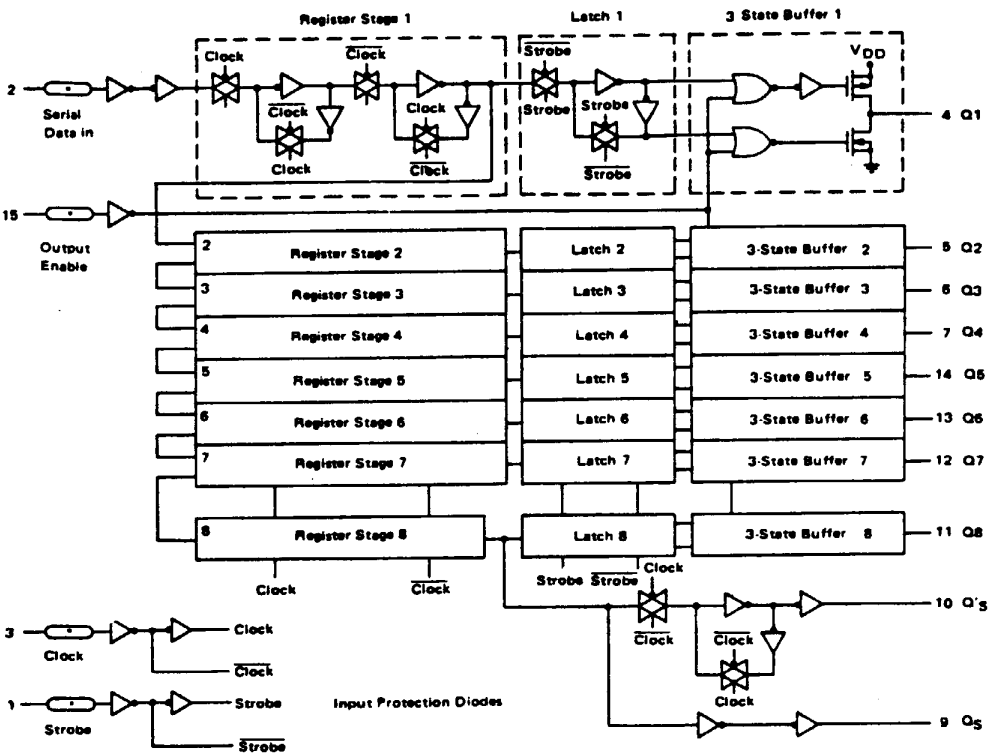
- Three-State Outputs
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTTL Loads Over the Rated Temperature Range
- Input Diode Protection
- Data Latch
- Dual Outputs for Data Out on Both Positive and Negative Clock Transitions
- Useful for Serial-to-Parallel Data Conversion
- Three-State Bus Compatible
- Pin-for-Pin Compatible with CD4094B



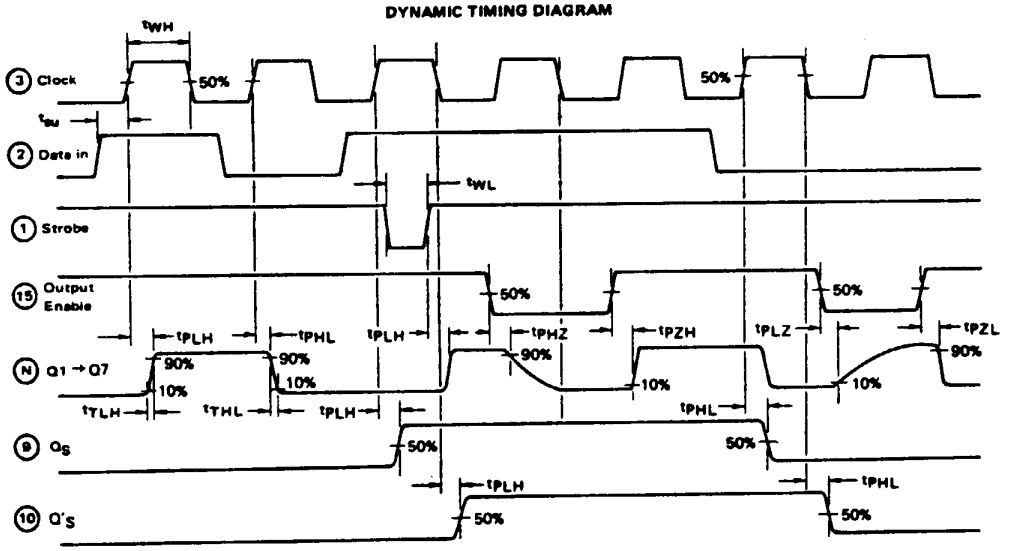
Clock	Output Enable	Strobe	Data	Parallel Outputs Q1	Parallel Outputs Q_N	Serial Outputs Q_S*	Serial Outputs Q'_S
↑	0	X	X	3S	3S	Q7	No Chg.
↓	0	X	X	3S	3S	No Chg.	Q7
↑	1	0	X	No Chg.	No Chg.	Q7	No Chg.
↑	1	1	0	0	Q_N-1	Q7	No Chg.
↑	1	1	1	1	Q_N-1	Q7	No Chg.
↓	1	1	1	No Chg.	No Chg.	No Chg.	Q7

3S = Three-State
X = Don't Care
*At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

BLOCK DIAGRAM



DYNAMIC TIMING DIAGRAM



MC145156

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

The MC145156 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

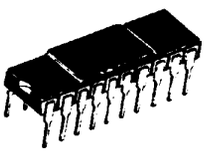
The MC145156 is programmed by a clocked, serial input, 19-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit programmable ÷ A counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145156 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145156.

- General Purpose Applications –
  CATV — TV Tuning
  AM/FM Radios — Scanning Receivers
  Two-Way Radios — Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values – 8, 64, 128, 256, 640, 1000, 1024, 2048
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Dual Modulus/Serial Programming
- ÷N Range = 3 to 1023
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options –
  Single Ended (Three-State)
  Double Ended

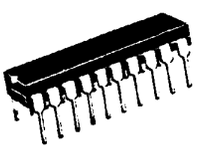
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

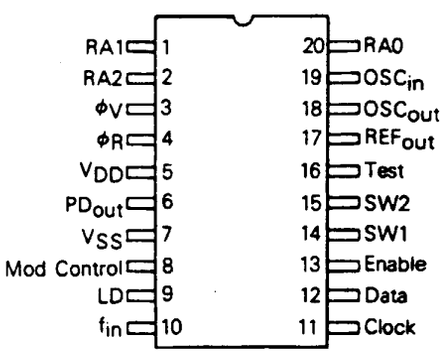


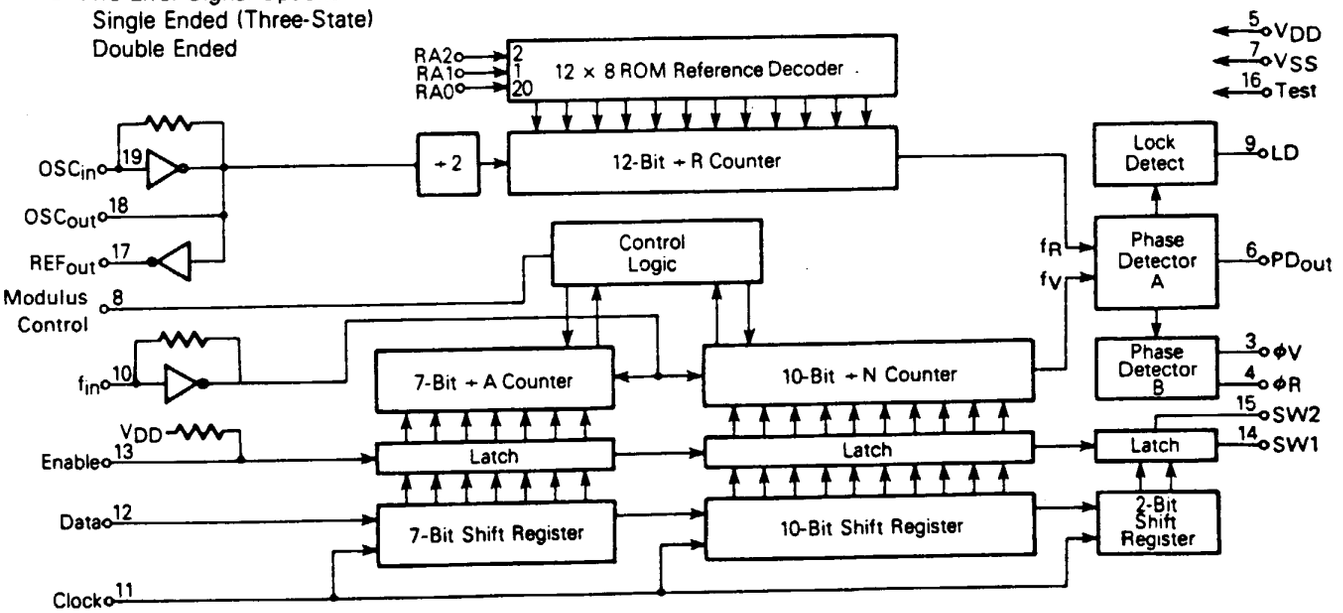
L SUFFIX
CERAMIC PACKAGE
CASE 729-01



P SUFFIX
PLASTIC PACKAGE
CASE 738-02

PIN ASSIGNMENT



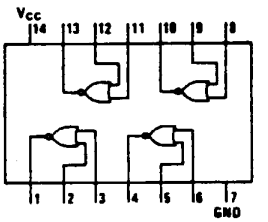


MM74C02 Quad 2-Input NOR Gate

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

MM54C02/MM74C02

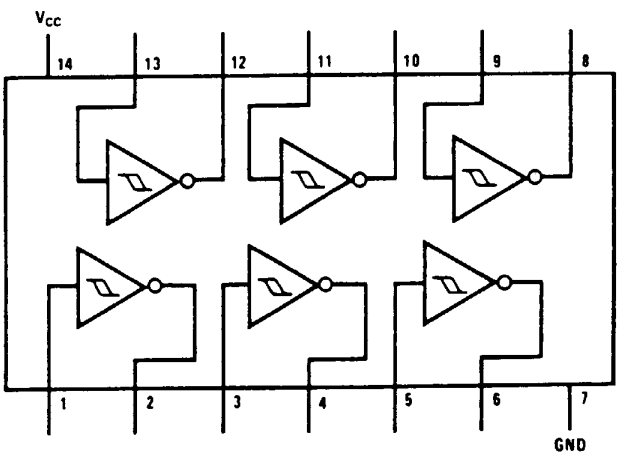


TOP VIEW

MM74C14 Hex Schmitt Trigger

The MM54C14/MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ. 0.0005 V/°C at $V_{CC} = 10$ V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2V_{CC}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.



TOP VIEW

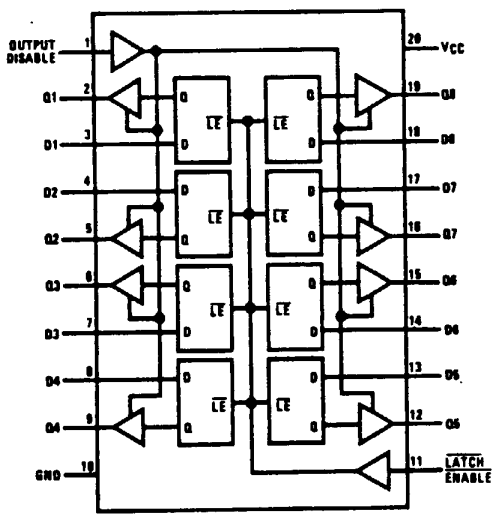
MM74C373
Octal Latch

General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads, such as one might find when driving a bus, and to have a fan-out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When $\overline{\text{LATCH ENABLE}}$ is high, the Q outputs will follow the D inputs. When $\overline{\text{LATCH ENABLE}}$ goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until $\overline{\text{LATCH ENABLE}}$ returns high again.

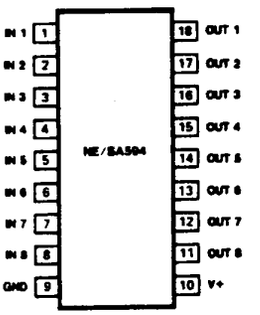
Connection Diagram



TOP VIEW

NE-SA594
VACUUM FLUORESCENT DISPLAY DRIVER

N, F PACKAGE

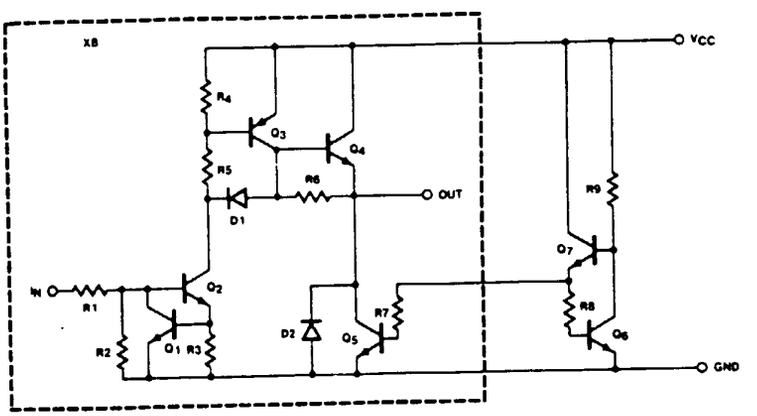


DESCRIPTION

The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.



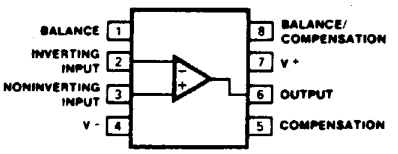
NE-5534
SINGLE AND DUAL LOW NOISE OPERATIONAL AMPLIFIER

DESCRIPTION

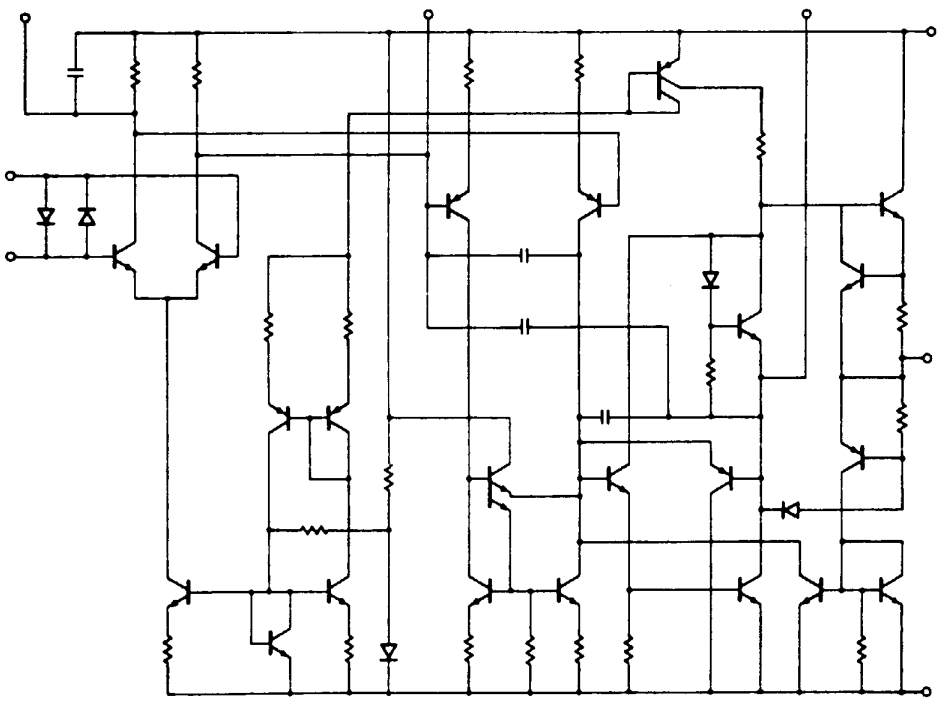
The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.)

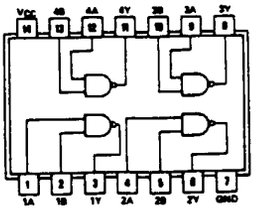
D,N,FE PACKAGE



EQUIVALENT SCHEMATIC



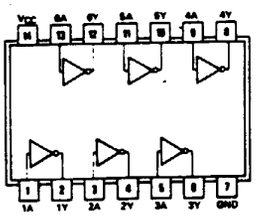
SN74LS00



QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS

$Y = \overline{AB}$

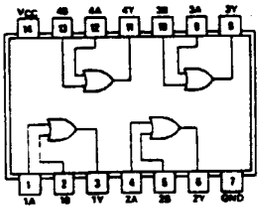
SN74LS04



HEX INVERTERS

$Y = \overline{A}$

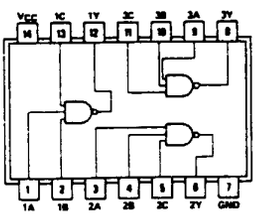
SN74LS08



QUADRUPLE 2-INPUT
POSITIVE-AND GATES

$Y = \overline{AB}$

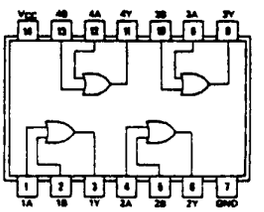
SN74LS27



TRIPLE 3-INPUT
POSITIVE-NOR GATES

$Y = \overline{A+B+C}$

SN74LS32

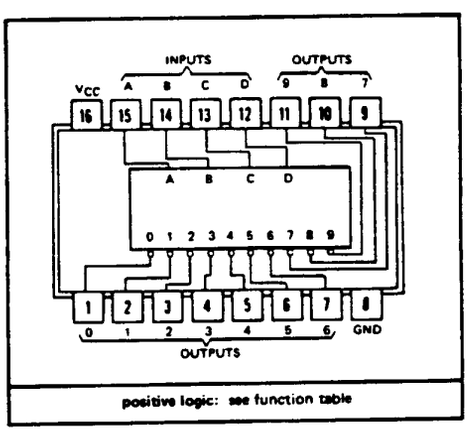


QUADRUPLE 2-INPUT
POSITIVE-OR GATES

$Y = A+B$

SN74LS42

4-LINE-TO-10-LINE DECODERS (1-OF-10)



positive logic: see function table

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A, 'L42, and 'LS42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 excess-3-gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. D-c noise margins are typically one volt.

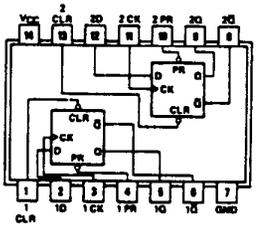
ALL TYPES									
DECIMAL OUTPUT									
0	1	2	3	4	5	6	7	8	9
L	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H
H	H	H	H	L	H	H	H	H	H
H	H	H	H	H	L	H	H	H	H
H	H	H	H	H	H	L	H	H	H
H	H	H	H	H	H	H	L	H	H
H	H	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	L
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H

SN74LS74N

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$



SN74L90
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTER

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

'90A, 'L90, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

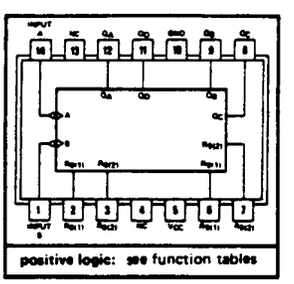
'90A, 'L90, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'L90, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant



positive logic: see function tables

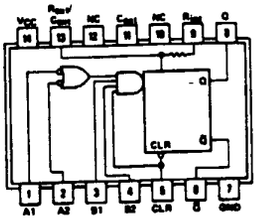
SN74LS122

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.



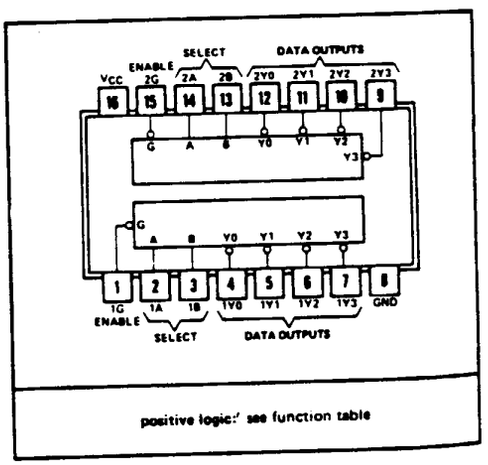
SN54122 (J, W) **SN74122 (J, N)**
SN54L122 (J, T) **SN74L122 (J, N)**
SN54LS122 (J, W) **SN74LS122 (J, N)**
'122 . . . R_{int} = 10 kΩ NOM
'L122 . . . R_{int} = 20 kΩ NOM
'LS122 . . . R_{int} = 10 kΩ NOM

SN74LS138
DECODER/DEMULIPLEXER

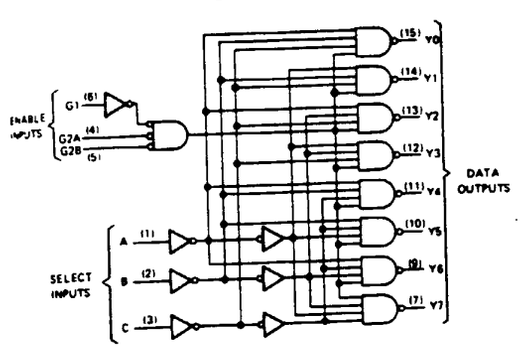
description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.



'LS138, 'S138



'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

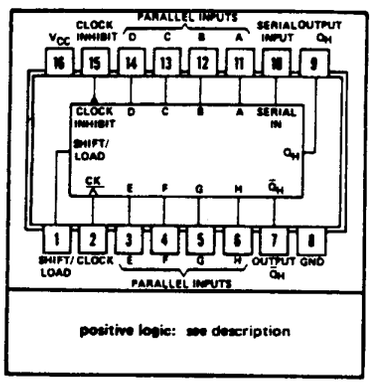
*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

SN74165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'165	26 MHz	210 mW
'LS165	35 MHz	105 mW

(TOP VIEW)



description

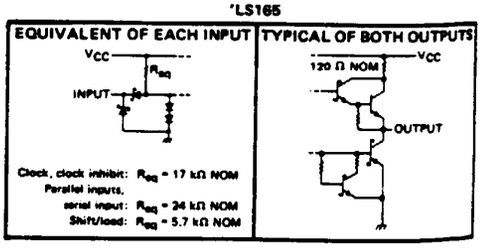
The '165 and 'LS165 are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

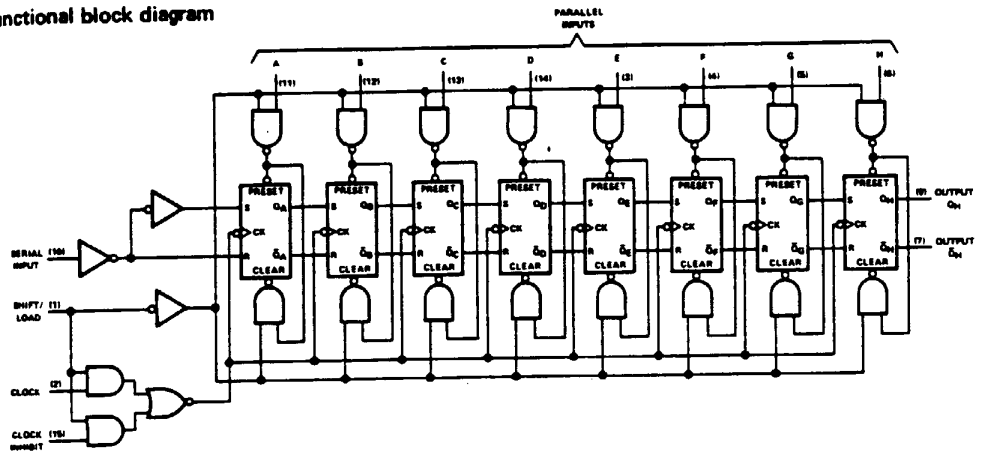
FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

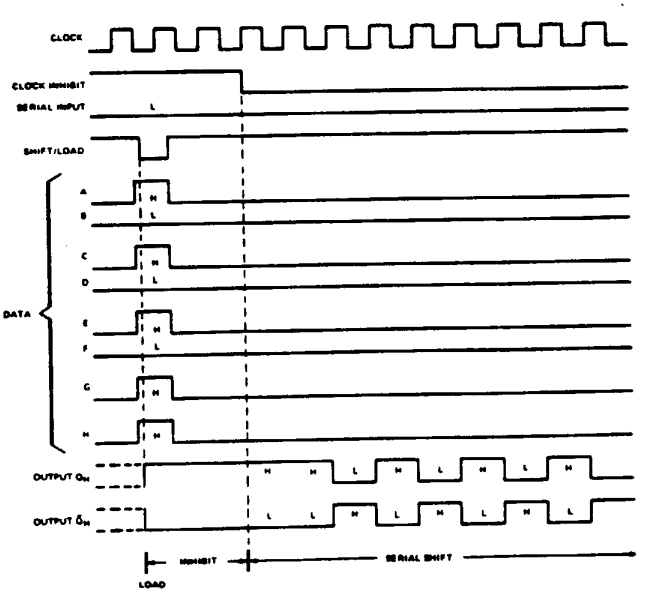
'LS165



functional block diagram



typical shift, load, and inhibit sequences



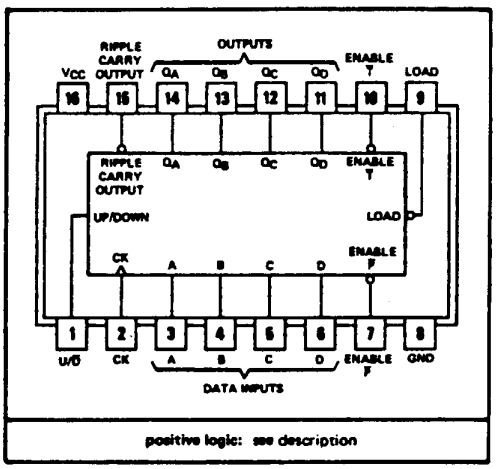
SN74LS168A
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

Programmable Look-Ahead Up/Down
Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS168A, 'LS169A	35 MHz	35 MHz	100 mW
'S168, 'S169	70 MHz	55 MHz	500 mW

(TOP VIEW)



positive logic: see description

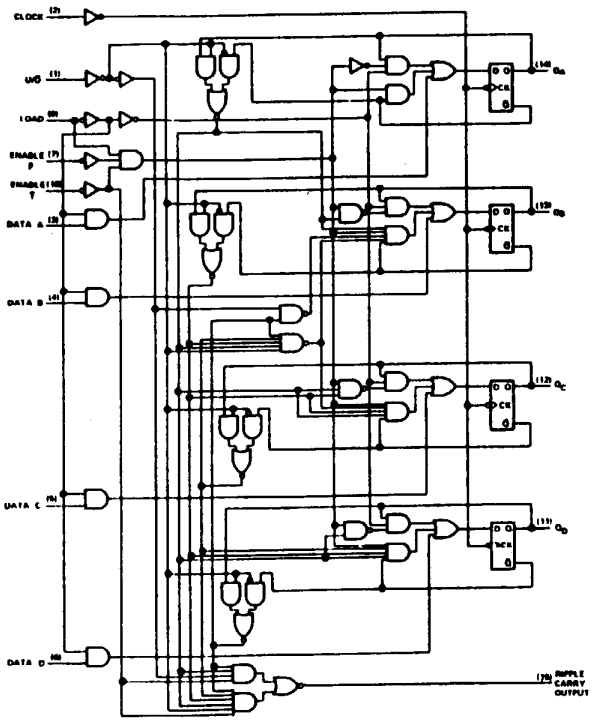
description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS168A and 'S168 are decade counters and the 'LS169A and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

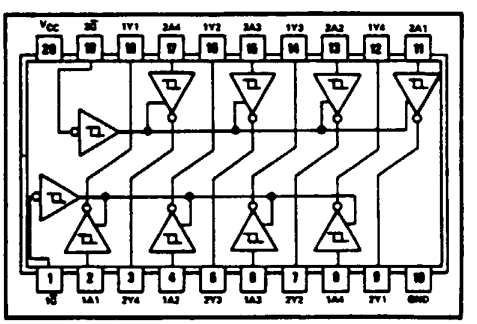
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.



SN74LS244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

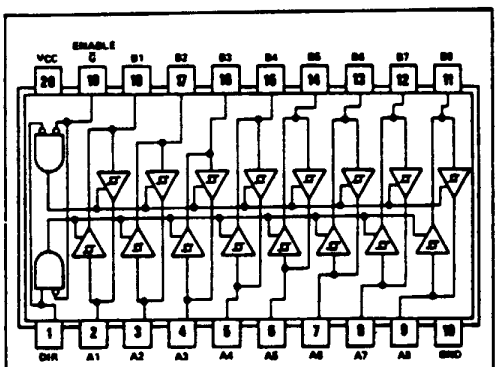


SN74LS245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.



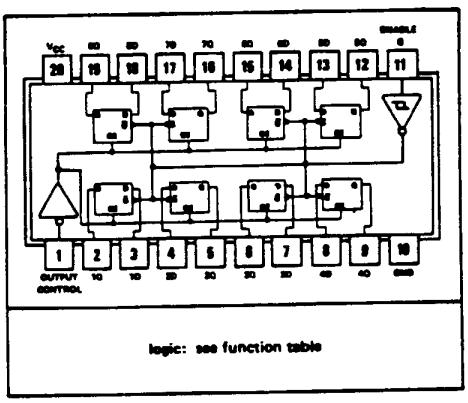
positive logic: see function table

FUNCTION TABLE

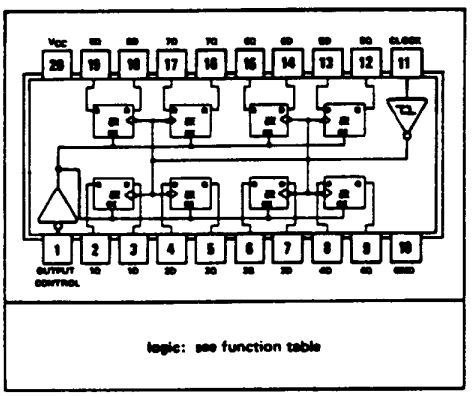
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

SN74LS373, SN74LS374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS



logic: see function table



logic: see function table

'LS373, 'S373
FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'LS374, 'S374
FUNCTION TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

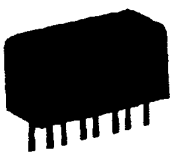
These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

SAY–1

Super High Level (+23 dBm LO) DOUBLE-BALANCED MIXERS

SAY SERIES



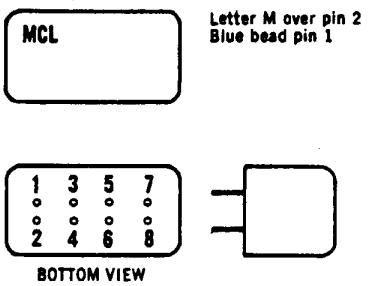
DESCRIPTION — High-level RF input capability coupled with ultra-low distortion, octaves of bandwidth, and reasonably good conversion loss make the SAY series obvious choices for applications in ECM receivers, spectrum analyzers, and field radios.

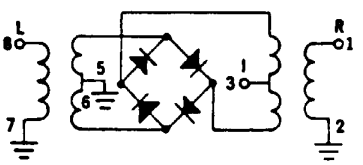
Housed in a miniature RFI shielded metal enclosure, these tiny units occupy a volume of only 0.128 cubic inches. The SAY series mixers are constructed to meet the requirements of MIL-M-28837/1A. Internally every unit is encapsulated with silicone rubber in order to withstand high shock, vibration, and acceleration environments.

These mixers offer two-tone, third order intermodulation products that are typically 70 dB below the desired IF level (each tone is set at 0 dBm and the LO drive is at +23 dBm). The 1 dB conversion compression point occurs at an RF level of +20 dBm.

CONNECTIONS

TOP VIEW

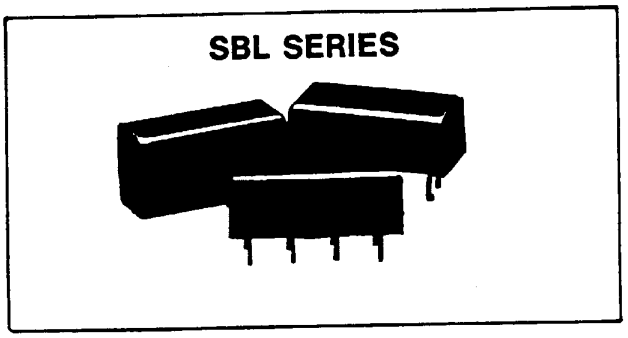




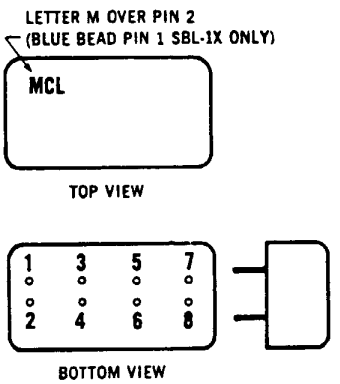
Model No.	-1 -2 -11
LO	8
RF	1
IF	3
Ground	2,5,6,7
Case Ground	2,5,6,7

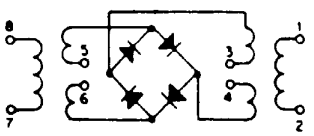
SBL-1

Standard Level (+7 dBm LO) DOUBLE-BALANCED MIXERS



CONNECTIONS





PIN LAYOUT

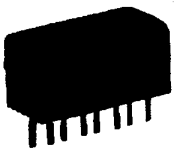
	Fig. 1	Fig. 2
Model No.	-1 *	-1X
LO	8	8
RF	1	3,4
IF	3,4	1
Ground	2,5,6,7	2,5,6,7
Case Ground	—	2,5,6,7

NOTE: PINS 3 AND 4 MUST BE CONNECTED TOGETHER

SRA-1

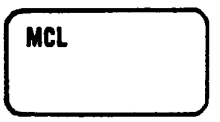
Standard Level (+7 dBm LO) DOUBLE-BALANCED MIXERS

SRA SERIES

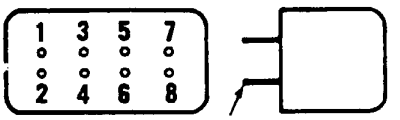


CONNECTIONS

TOP VIEW



Letter M over pin 2
Blue bead pin 1

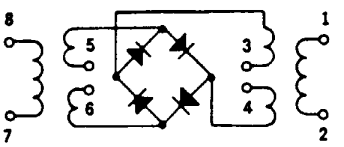


BOTTOM VIEW

DESCRIPTION — Having a volume of only .128 cu. inches, the SRA series covers a very broad frequency range from 500 Hz to 2000 MHz. These rugged units provide low conversion loss, 6 dB, high isolation, 40 dB, and exceptional unit to unit matched performance.

Packaged within an RFI shielded metal enclosure and hermetically sealed header, these high performance units have their pins oriented on a 0.2 inch grid.

Only well matched hot-carrier diodes and ruggedly constructed transmission line transformers are used. Internally, every component is bonded to the header and case with silicone rubber to provide super reliable protection against shock, vibration and acceleration.

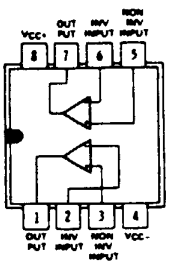


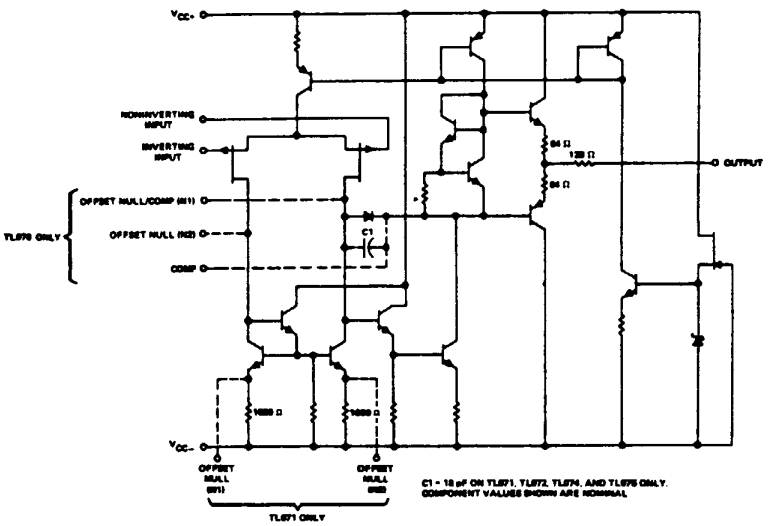
SCHEMATIC FOR FIG. 1, 2, 3 AND 4

PIN LAYOUT

	Fig. 1
Model No.	-1 -1-1 -3 -1TX
LO	8
RF	1
IF	3,4
Ground	2,5,6,7
Case Ground	2

TL072
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS





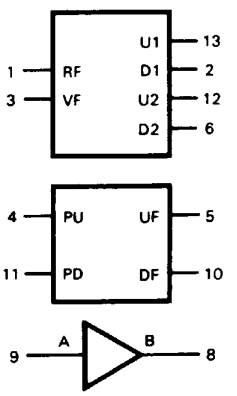
description

The JFET-input operational amplifiers of the TL071 series are designed as low-noise versions of the TL081 series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL071 series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET-inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

11C44
Phase/Frequency Detector

GENERAL DESCRIPTION — The 11C44 contains a Phase/Frequency Detector, a Phase Detector, a Charge Pump, and an Amplifier The Phase/Frequency Detector accepts TTL signals representing a Reference Frequency (RF) and a Variable Frequency (VF), compares the relative timing of their negative going transitions, and generates either an UP (U1) or a DOWN (D1) signal whose duration is equal to the RF-VF timing difference. When the RF and VF signals have the same frequency, the Phase Detector outputs U2 and D2 provide binary signals whose duty cycles are proportional to the phase angle between RF and VF. The Charge Pump can be driven from U1 and D1 or U2 and D2, and has three possible output states representing CHARGE, DISCHARGE, and HOLD instructions when applied to an integrator. The Amplifier is a Darlington transistor with grounded emitter and uncommitted collector and base. The 11C44 thus contains several of the functional elements used in phase-locked loop applications.

LOGIC SYMBOL

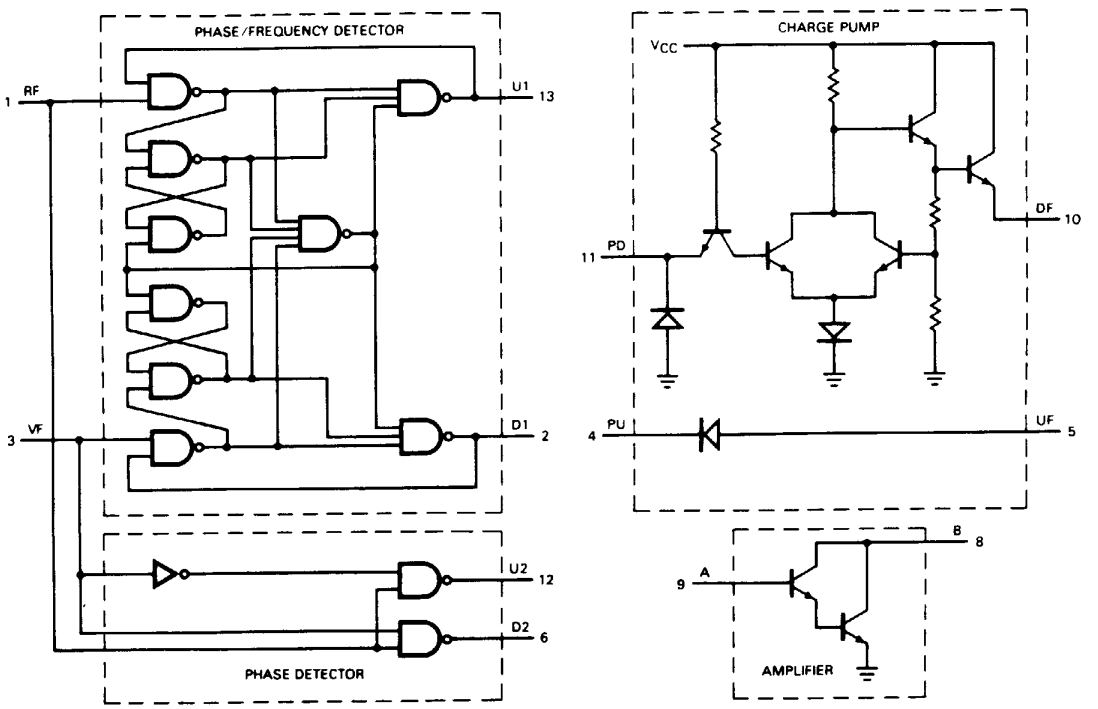


V_{CC} = Pin 14
GND = Pin 7

FUNCTIONS

RF — Reference Frequency Input
VF — Variable Frequency Input
U1, D1 — Phase/Frequency Detector Outputs
U2, D2 — Phase Detector Outputs
PU, PD — Charge Pump Inputs
UF, DF — Charge Pump Outputs
A — Amplifier Input
B — Amplifier Output

LOGIC DIAGRAM AND SCHEMATIC



ENHANCED PROGRAMMABLE COMMUNICATIONS INTERFACE (EPCI) 2661

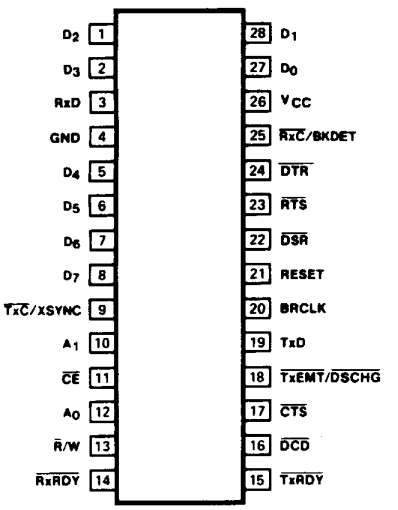
DESCRIPTION

The Signetics 2661 EPCI is a universal synchronous/asynchronous data communications controlle. chip that is an enhanced pin compatible version of the 2651. It interfaces directly to most 8-bit microprocessors and may be used in a polled or interrupt driven system environment. The 2661 accepts programmed instructions from the microprocessor while supporting many serial data communications disciplines—synchronous and asynchronous—in the full or half-duplex mode. Special support for BISYNC is provided.

The EPCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

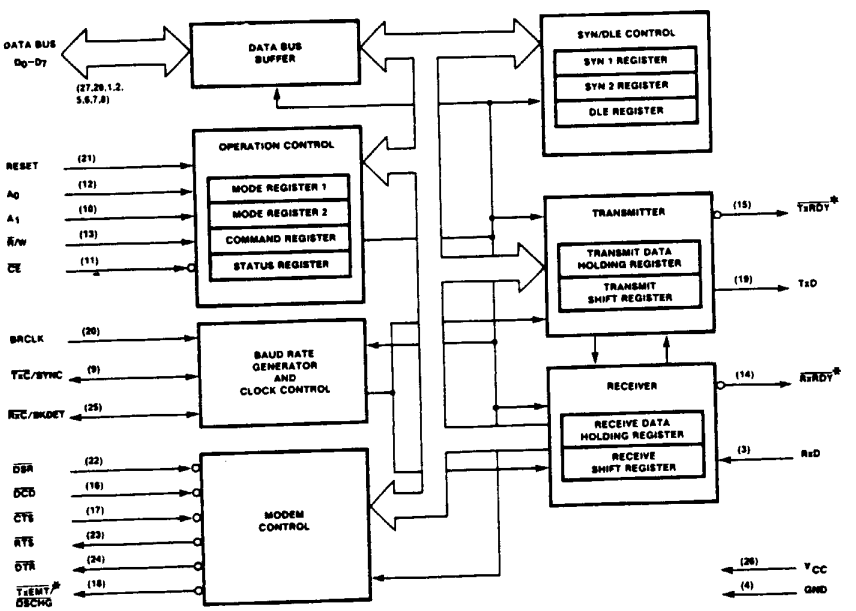
The 2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the EPCI (-1, -2, -3) has a different set of baud rates.

The EPCI is constructed using Signetics n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
27,28,1, 2,5-8	D_0-D_7	8-bit data bus	I/O
21	RESET	Reset	I
12,10	A_0-A_1	Internal register select lines	I
13	R/W	Read or write command	I
11	CE	Chip enable input	I
22	DSR	Data set ready	I
24	DTR	Data terminal ready	O
23	RTS	Request to send	O
17	CTS	Clear to send	I
16	DCD	Data carrier detected	I
18	TxEMT/DSCHG	Transmitter empty or data set change	O
9	TxC/XSYNC	Transmitter clock/external SYNC	I/O
25	RxC/BKDET	Receiver clock/break detect	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	TxRDY	Transmitter ready	O
14	RxRDY	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5V supply	I
4	GND	Ground	I



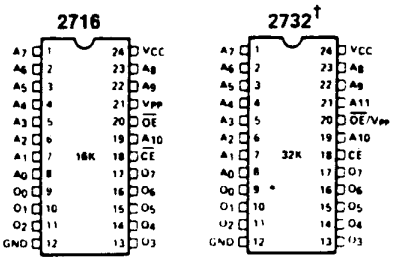
2716
16K (2K x 8) UV ERASABLE PROM

- **Fast Access Time**
  - **— 350 ns Max. 2716-1**
  - **— 390 ns Max. 2716-2**
  - **— 450 ns Max. 2716**
  - **— 650 ns Max. 2716-6**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— 525 mW Max. Active Power**
  - **— 132 mW Max. Standby Power**
- **Pin Compatible to Intel® 2732 EPROM**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50 ms Pulse**
- **Inputs and Outputs TTL Compatible during Read and Program**
- **Completely Static**

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

PIN CONFIGURATION



†Refer to 2732 data sheet for specifications

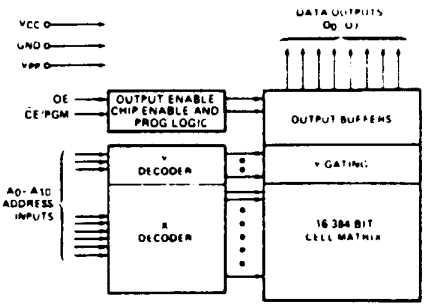
PIN NAMES

A_0- A_{10}	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



2732
32K (4K x 8) UV ERASABLE PROM

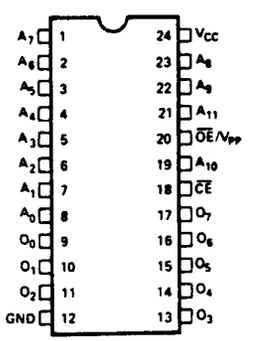
- **Fast Access Time:**
  - **— 450 ns Max. 2732**
  - **— 550 ns Max. 2732-6**
- **Single +5V ± 5% Power Supply**
- **Output Enable for MCS-85™ and MCS-86™ Compatibility**
- **Low Power Dissipation:**
  150mA Max. Active Current
  30mA Max. Standby Current
- **Pin Compatible to Intel® 2716 EPROM**
- **Completely Static**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50ms Pulse**
- **Three-State Output for Direct Bus Interface**

The Intel® 2732 is a 32,768-bit ultraviolet erasable and electrically programmable read-only memory EPROM . The 2732 operates from a single 5-volt power supply, has a standby mode, and features an output enable control.

An important 2732 feature is the separate output control, Output Enable $\overline{OE}$, from the Chip Enable control $\overline{CE}$. The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems.

The 2732 has a standby mode which reduces the power dissipation without increasing access time. The maximum active current is 150mA, while the maximum standby current is only 30mA, an 80% savings. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.

PIN CONFIGURATION



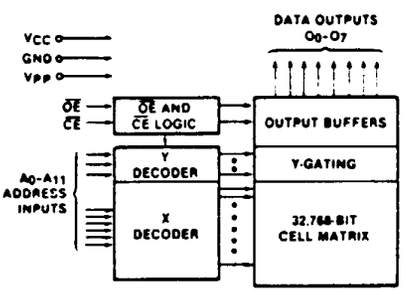
PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

BLOCK DIAGRAM



8035
SINGLE COMPONENT 8-BIT MICROCOMPUTER

***8048 Mask Programmable ROM**
***8748 User Programmable/Erasable EPROM**
***8035 External ROM or EPROM**

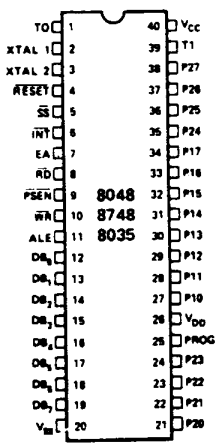
- 8-Bit CPU, ROM, RAM, I/O in Single Package
- Interchangeable ROM and EPROM Versions
- Single 5V Supply
- 2.5 µsec and 5.0 µsec Cycle Versions All Instructions 1 or 2 Cycles.
- Over 90 Instructions: 70% Single Byte
- 1K x 8 ROM/EPROM 64 x 8 RAM 27 I/O Lines
- Interval Timer/Event Counter
- Easily Expandable Memory and I/O
- Compatible with 8000 Series Peripherals
- Single Level Interrupt

The Intel® 8048/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

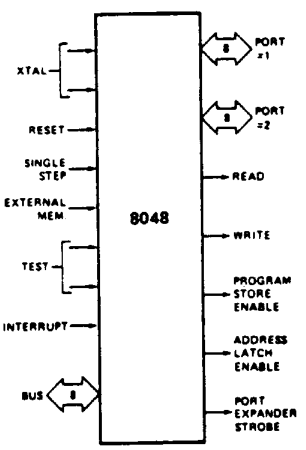
The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and 8000 series peripherals. The 8035 is the equivalent of an 8048 without program memory.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

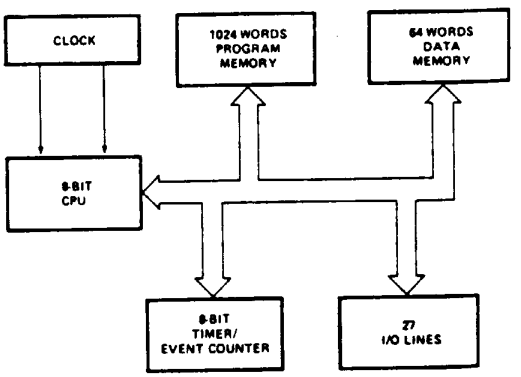
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 ROM version.
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Program pulse (+25V) input pin during 8748 programming. Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243
DB_0-DB_7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device. Used as a Read Strobe to External Data Memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low)
$\overline{WR}$	10	Output strobe during a BUS write. (Active low)(Non TTL V_{IH}) Used as write strobe to External Data Memory.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Not TTL Compatible)
XTAL2	3	Other side of crystal input.

8085A/8085A-2
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSORS

- Single +5V Power Supply
- 100% Software Compatible with 8080A
- 1.3 μs Instruction Cycle (8085A); 0.8 μs (8085A-2)
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One is non-Maskable) Plus an 8080A-compatible interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64k Bytes of Memory

The Intel® 8085A is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085A (CPU), 8156 (RAM/IO) and 8355/8755A (ROM/PROM/IO)] while maintaining total system expandability. The 8085A-2 is a faster version of the 8085A.

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allow a direct interface with the 8085A.

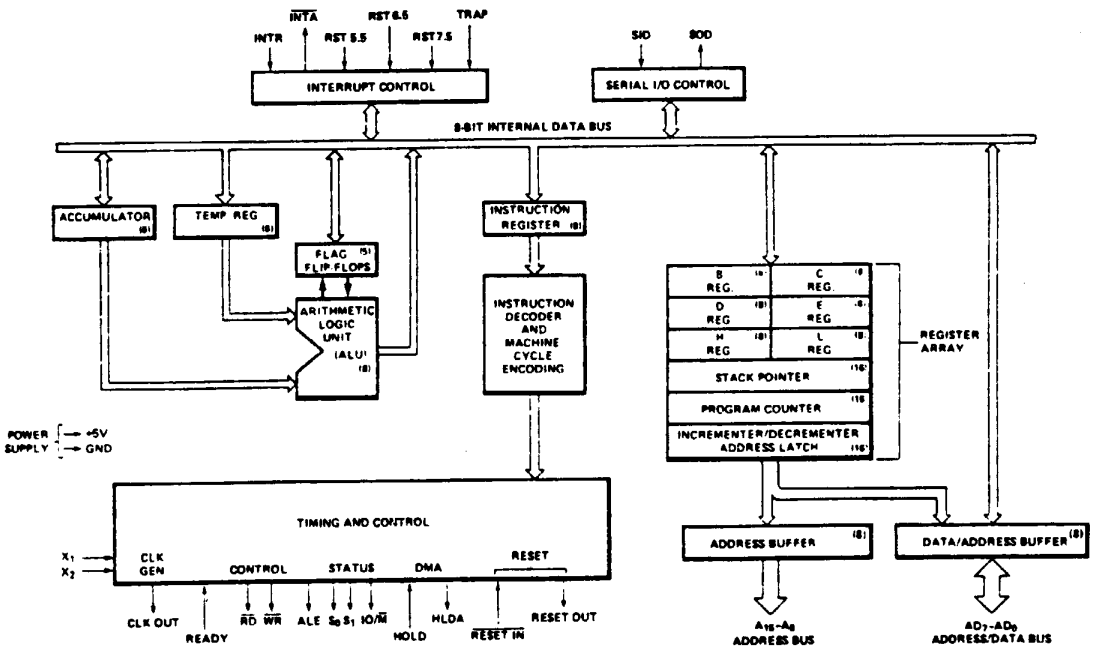


Figure 1. 8085A CPU Functional Block Diagram

8155/8156/8155-2/8156-2
2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

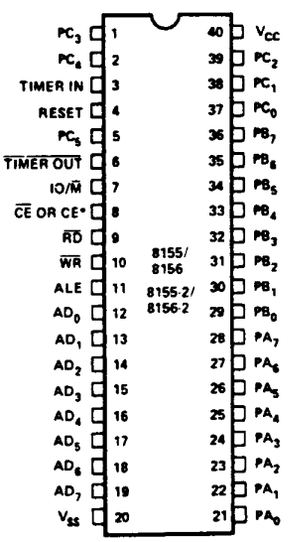
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/ Timer
- Compatible with 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 89156 are RAM and I/O chips to be used in the 8085A and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085A CPU. The 8155-2 and 8156-2 have maximum access times of 330 ns for use with the 8085A-2 and the full speed 5 MHz 8088 CPU.

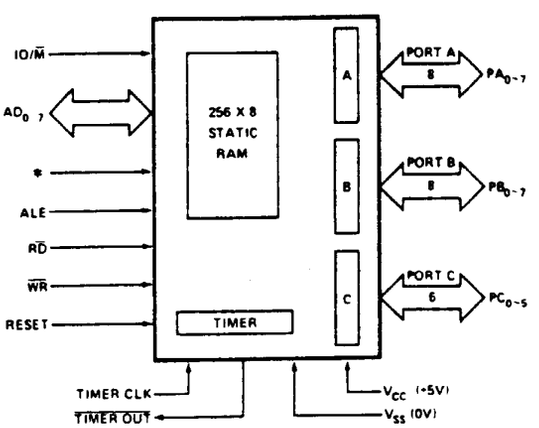
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is jalso included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



: 8155/8155-2 = $\overline{CE}$, 8156/8156-2 = CE

8155/8156 PIN FUNCTIONS

Symbol	Function
RESET (input)	Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT . Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085A clock cycle times.
AD_{0-7} (input)	3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155/56 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
CE or $\overline{CE}$ (input)	Chip Enable: On the 8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$ (input)	Read control: Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$ (input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/$\overline{M}$.

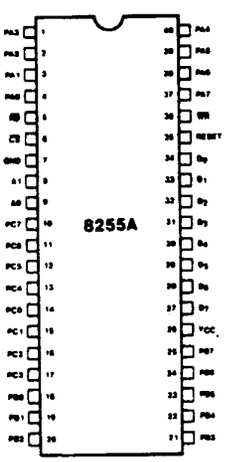
Symbol	Function
ALE input	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$ (input)	Selects memory if low and I/O and command/status registers if high.
PA_{0-7}(8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7}(8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5}(6) (input/output)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — $\overline{ABF}$ (Port A Buffer Full) PC_2 — $\overline{A\ STB}$ (Port A Strobe) PC_3 — B INTR (Port B Interrupt) PC_4 — $\overline{B\ BF}$ (Port B Buffer Full) PC_5 — B STB (Port B Strobe)
TIMER IN (input)	Input to the counter-timer.
$\overline{TIMER\ OUT}$ (output)	Timer output. This output can be either a square wave or a pulse depending on the timer mode.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255A BLOCK DIAGRAM