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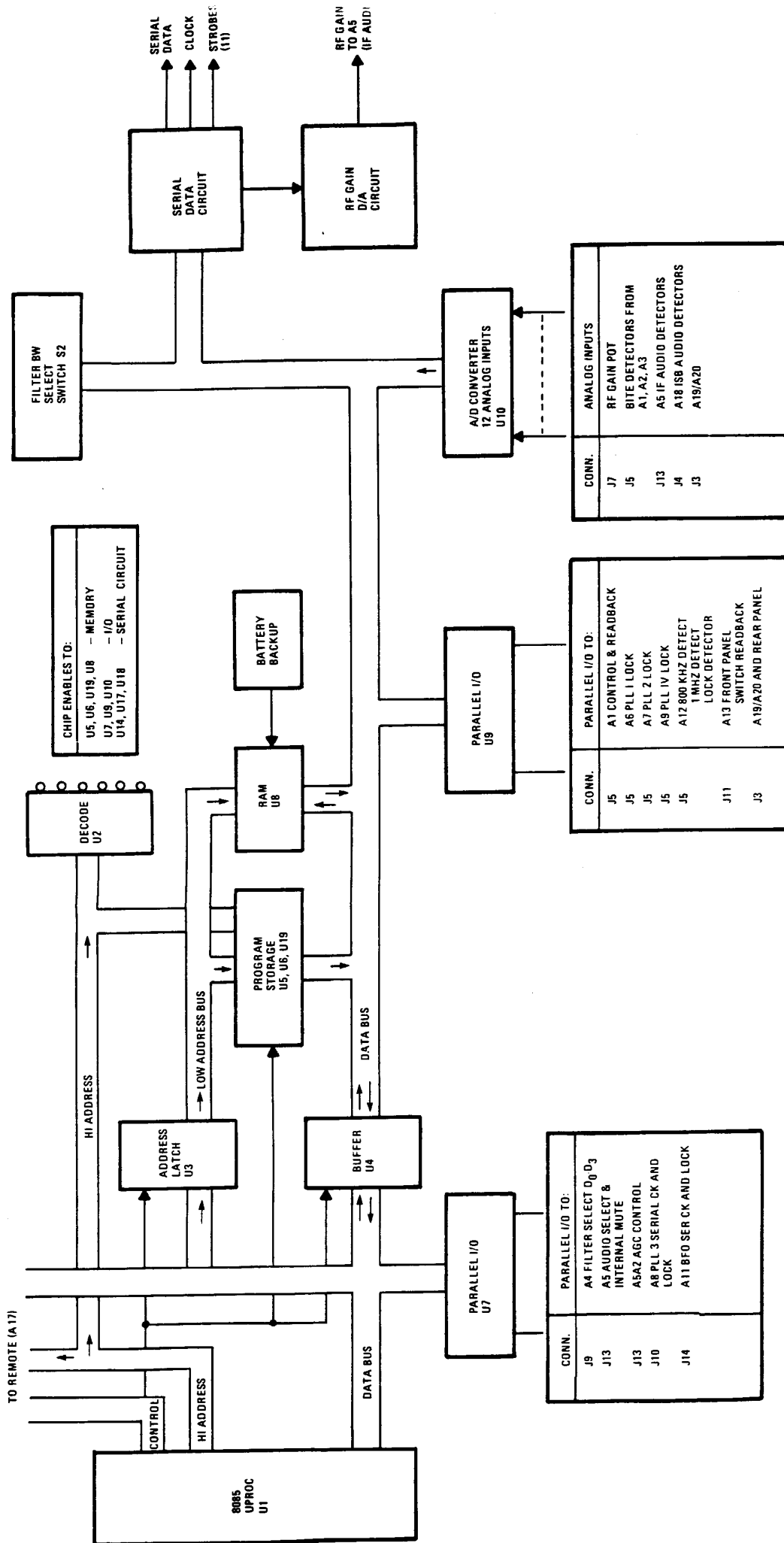
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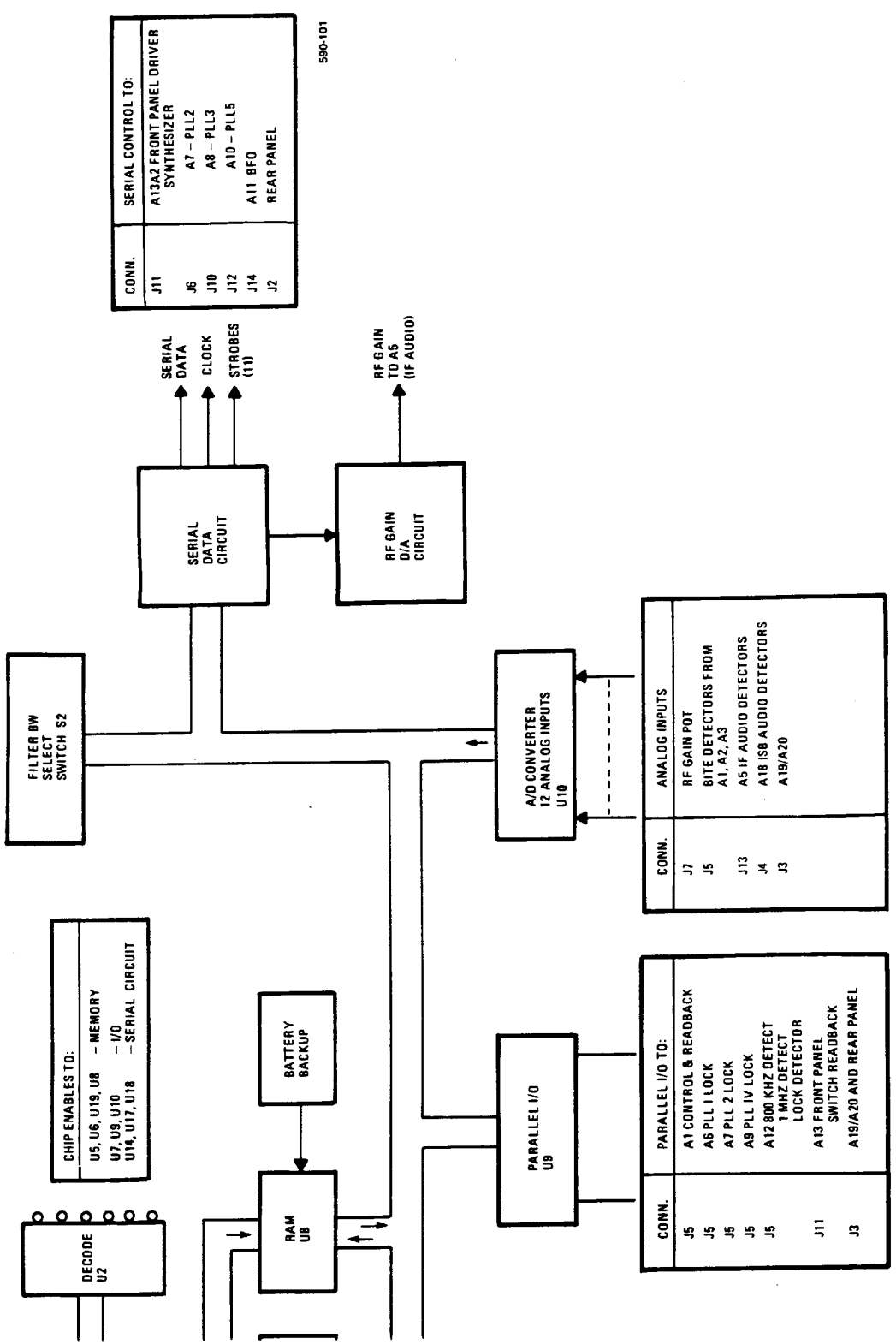


CONN.	PARALLEL I/O TO:
J9	A4 FILTER SELECT D_0, D_3
J13	A5 AUDIO SELECT & INTERNAL MUTE
J13	A5AZ AGC CONTROL
J10	A8 PLL 3 SERIAL CK AND LOCK
J14	A11 BFO SER CK AND LOCK

CONN.	PARALLEL I/O TO:
J5	A1 CONTROL & READBACK
J5	A6 PLL 1 LOCK
J5	A7 PLL 2 LOCK
J5	A9 PLL IV LOCK
J5	A12 800 KHZ DETECT 1 MHZ DETECTOR LOCK
J11	A13 FRONT PANEL SWITCH READBACK
J3	A19/A20 AND REAR PANEL

CONN.	ANALOG INPUTS
J7	RF GAIN POT
J5	BITE DETECTORS FROM A1, A2, A3
J13	A5 IF AUDIO DETECTORS
J4	A18 ISB AUDIO DETECTORS
J3	A19/A20

Control Board Assembly A14
Functional Block Diagram



590-101

CONN.	SERIAL CONTROL TO:
J11	A13A2 FRONT PANEL DRIVER SYNTHESIZER
J6	A7 - PLL2
J10	A8 - PLL3
J12	A10 - PLL5
J14	A11 BFO
J2	REAR PANEL

CONN.	ANALOG INPUTS
J7	RF GAIN POT
J5	BIT DETECTORS FROM A1, A2, A3
J13	A5 IF AUDIO DETECTORS
J4	A18 ISB AUDIO DETECTORS
J3	A19/A20

CONN.	PARALLEL I/O TO:
J5	A1 CONTROL & READBACK
J5	A6 PLL 1 LOCK
J5	A7 PLL 2 LOCK
J5	A9 PLL IV LOCK
J5	A12 800 KHZ DETECT
J5	1 MHZ DETECT
J11	LOCK DETECTOR
J3	A13 FRONT PANEL SWITCH READBACK
	A19/A20 AND REAR PANEL

CHIP ENABLES TO:
U5, U6, U19, U8 - MEMORY
U7, U9, U10 - I/O
U14, U17, U18 - SERIAL CIRCUIT

DECODE
U2

1. GENERAL DESCRIPTION

CPU PWB A14 contains the 8085A CPU and associated peripheral circuits, serial data transmission circuits, parallel I/O circuits, and analog-to-digital as well as digital-to-analog converter circuitry. Functioning as the control element of the RF-590, this assembly is responsible for accepting input from the front panel and receiver assemblies as well as generating the digital signals necessary to control the receiver. Software contained within the three, 4K byte EPROMs is executed to supervise, control, and in the BITE process, test the display, control, and radio circuitry. Random access read/write memory (RAM) is used for temporary storage by the software program and for battery backed storage of receiver setups, programmed channels, and channel groups.

2. INTERFACE CONNECTIONS

All Control PWB interface connections are shown in table 1 and schematic diagram.

Table 1. Control Board Assembly A14 Interface Summary

Connector	Function	To	From
A14J1-1	N/C	—	—
-2	Index Key	—	—
-3	+5V	—	A15J3-9
-4	+5V	—	A15J3-21
A14J2-1	Remote Out 1	J7-1	—
-2	Serial Strobe 2	J7-20	—
-3	Gnd	J7-2	—
-4	N/C	—	—
-5	Scan Step	—	J7-3
-6	Remote Out 2	J7-22	—
-7	Remote Out 0	J7-4	—
-8	Serial Strobe 1	J7-23	—
-9	Stop Scan	—	J7-5
-10	Serial Clock	J7-24	—
-11	N/C	—	—
-12	Serial Data	J7-25	—
-13	Ext. Mute	—	J7-7
-14	Fault	J7-16	—
A14J3-1	Noise Bank	—	A19J1-1
-2	Filter Id	—	A19J1-2
-3	Overload	—	A19J1-3
-4	Conv. Id	—	A19J1-4
-5	Osc. Enable	A19J1-5	—
-6	Index Key	—	—

HARRIS
RF COMMUNICATIONS

Table 1. Control Board Assembly A14 Interface Summary (Cont.)

Connector	Function	To	From
A14J3-7 -8 -9 -10	Ext. Mute Enable Serial Data Serial Clock	A19J1-7 A19J1-8 A19J1-9 A19J1-10	— — — —
A14J4-1 -2 -3 -4 -5 -6 -7 -8 -9 -10	N/C Int. Mute Det. IF Input Det. Line Audio AGC Line Audio Adj. Ext. Mute Index Key ISB Audio Meter ISB AGC Meter	— A18J1-9 — — — A18J1-5 A18J1-4 — — —	— — A18J1-8 A18J1-7 A18J1-6 — — — A18J1-2 A18J1-1
A15J5-1 -2 -3 4 -5 -6 -7 -8 -9 -10 -11 -12 -13 -14	N/C A3 Det. A2 Det. A1 Ext. Mute A1 Relay Control A1 Relay Test A1 BITE Osc. Enab. A1 Ant. Overload A1 BITE Det. Out A6 PLL I Lock Det A9 PLL IV Lock Det A12 800 kHz Det A12 1 MHz Det A12 40 MHz PLL Lock Det	— — — A16A3J3-1 A16A3J3-4 A16A3J3-5 A16A3J3-6 — — — — — — —	— A16A2J2-3 A16A2J2-4 — — — — A16A3J3-7 A16A3J3-8 A16A3J1-1 A16A3J1-3 A16A3J1-4 A16A3J1-5 A16A3J1-6
A14J6-1 -2 -3 -4 -5 -6 -7 -8	Serial Data Serial Clock Index Key Serial Check Enable PLL II Lock Det Gnd N/C	A7J1-1 A7J1-2 — — A7J1-5 — A7J1-7 —	— — — A7J1-4 — A7J1-6 — —

Table 1. Control Board Assembly A14 Interface Summary (Cont.)

Connector	Function	To	From
A14J7-1	LSB Select	—	A13A3J1-1
-2	ISB AGC Meter	A13A3J1-2	—
-3	RF Gain	—	A13A3J1-3
-4	ISB Audio	A13A3J1-4	—
-5	-15V	A13A3J1-5	—
-6	LSB Audio Adj.	—	A13A3J1-6
-7	N/C	—	—
-8	+5V Ref.	A13A3J1-8	—
-9	Gnd	A13A3J1-9	—
-10	+15V	A13A3J1-10	—
A14J8-1	BITE P/S	—	A15J3-22
-2	N/C	—	—
-3	+15V	—	A15J3-23
-4	-15V	—	A15J3-11
-5	Index Key	—	—
-6	+8.5V	—	A15J3-12
-7	Gnd	—	A15J3-25
-8	Gnd	—	A15J3-13
A14J9-1	N/C	—	—
-2	N/C	—	—
-3	D3	A4J5-9	—
-4	D0	A4J5-8	—
-5	D2	A4J5-7	—
-6	Index Key	—	—
-7	D1	A4J5-5	—
-8	Gnd	A4J5-4	—
A14J10-1	Serial Data	A8J4-1	—
-2	Serial Clock	A8J4-2	—
-3	Index Key	—	—
-4	Serial Check	—	A8J4-4
-5	Enable	A8J4-5	—
-6	PLL III Lock Det	—	A8J4-6
-7	Gnd	A8J4-7	—
-8	N/C	—	—
A14J11-1	Twhl Int	—	A13A2J1-1
-2	Serial Data	A13A2J1-2	—
-3	Twhl Direction	—	A13A2J1-3

HARRIS
RF COMMUNICATIONS

Table 1. Control Board Assembly A14 Interface Summary (Cont.)

Connector	Function	To	From
A14J11-4	Serial Clock	A13A2J1-4	—
-5	Twhl Reset	A13A2J1-5	—
-6	-15V	A13A2J1-6	—
-7	+5V	A13A2J1-7	—
-8	BITE P/S	A13A2J1-8	—
-9	PB3	A13A2J1-9	—
-10	Kybd Strobe	A13A2J1-10	—
-11	PB2	A13A2J1-11	—
-12	Fault	—	A13A2J1-12
-13	PB1	A13A2J1-13	—
-14	Display Strobe	A13A2J1-14	—
-15	PB0	A13A2J1-15	—
-16	Reset	A13A2J1-16	—
-17	N/C	—	—
-18	Gnd	A13A2J1-18	—
-19	+8.5V	A13A2J1-19	—
-20	Gnd	A13A2J1-20	—
A14J12-1	Serial Data	A10J1-1	—
-2	Serial Clock	A10J1-2	—
-3	Index Key	—	—
-4	Serial Check	—	A10J1-4
-5	Enable	A10J1-5	—
-6	PLL V Lock Det	—	A10J1-6
-7	Gnd	A10J1-7	—
-8	N/C	—	—
A14J13-1	Gnd	A5J6-1	—
-2	RF Gain 0-10V	A5J6-2	—
-3	Data AGC	—	—
-4	AGC Off	A5J6-4	—
-5	C Audio Select	A5J6-5	—
-6	Int. Mute	A5J6-6	—
-7	B Audio Select	A5J6-7	—
-8	AGC Fast	A5J6-8	—
-9	A Audio Select	A5J6-9	—
-10	AGC Medium	A5J6-10	—
-11	Ext. Mute	A5J6-11	—
-12	Line Audio	—	A5J6-12
-13	Line Audio Gnd	—	A5J6-13

Table 1. Control Board Assembly A14 Interface Summary (Cont.)

Connector	Function	To	From
A14J13-14	Line Audio Det Out	—	A5J6-14
-15	IF Input Det	—	A5J6-15
-16	Second IF AGC	—	A5J6-16
A14J14-1	Serial Data	A11J4-1	—
-2	Serial Clock	A11J4-2	—
-3	Index Key	—	—
-4	Serial Check 1	—	A11J4-4
-5	Enable	A11J4-5	—
6	BFO Lock Detect	—	A11J4-6
-7	Gnd	A11J4-7	—
-8	BFO On/Off	A11J4-8	—
A14J15-1	+8.5V	A17J1-1	—
-2	+8.5V	A17J1-2	—
-3	Reset Out	A17J1-3	—
-4	HOLD	—	A17J1-4
-5	Line Audio	A17J1-5	—
-6	HLDA	A17J1-6	—
-7	Line Audio Gnd	A17J1-7	—
-8	CPU Clk Out	A17J1-8	—
-9	+15V	A17J1-9	—
-10	Gnd	A17J1-10	—
-11	Ready	—	A17J1-11
-12	-15V	A17J1-12	—
-13	RST 5.5	—	A17J1-13
-14	IO/M	A17J1-14	—
-15	INTR	—	A17J1-15
-16	S1	A17J1-16	—
-17	WR	A17J1-17	—
-18	RD	A17J1-18	—
-19	INTA	A17J1-19	—
-20	ALE	A17J1-20	—
-21	N/C	—	—
-22	N/C	—	—
-23	AD0	A17J2-3	Bi direc
-24	N/C	—	—
-25	AD1	A17J2-5	Bi direc
-26	A15	A17J2-6	—
-27	AD2	A17J2-7	Bi direc
-28	A14	A17J2-8	—

Table 1. Control Board Assembly A14 Interface Summary (Cont.)

Control	Function	To	From
A14J15-29	AD3	A17J2-9	Bi direc
-30	A13	A17J2-10	—
-31	AD4	A17J2-11	Bi direc
-32	A12	A17J2-12	—
-33	AD5	A17J2-13	Bi direc
-34	A11	A17J2-14	—
-35	AD6	A17J2-15	Bi direc
-36	A10	A17J2-16	—
-37	AD7	A17J2-17	Bi direc
-38	A9	A17J2-18	—
-39	Gnd	A17J2-19	—
-40	A8	A17J2-20	—

3. FUNCTIONAL DESCRIPTION

3.1 CPU and Interface

The 8085A microprocessor (U1) executes the application program. The 6.0 MHz frequency of crystal Y1 is divided by two within U1 to yield the 3.0 MHz processor timing (333 nanosecond cycle time). The high order address bits of the CPU are inputs to address decoder U2, producing one of ten, active low chip selects to peripheral circuits. The multiplexed low address/data (AD) bus from U1 is input to low address latch U3 and bidirectional buffer U4. The control lines \overline{RD} and \overline{WR} are buffered by two gates of U23, with highest address line A15 and interrupt lines gated through U22 to control direction of U4. The \overline{RD} and \overline{WR} signals are combined with several of the enable outputs of U2 through U24 to produce chip selects for several devices. The major outputs of the microprocessor are also run to connector J15 for access to the installed remote; with R22, R23, R24, and R37 holding the lines at their proper logic levels. R26 and R36 act as pullup termination to the address and data busses, respectively. The high active interrupt lines of the CPU are dedicated as follows.

- RST 7.5 uses the real-time clock
- RST 6.5 handles the tune knob encoder interrupt
- RST 5.5 is used by the remote control option

3.2 Reset and Trap

When the receiver power is turned on, the RC network (formed by R10 and C26) holds the processor RESET IN input low for about 100 milliseconds. This allows the power supplies time to stabilize before the

CPU starts running. Diode CR4 and Q2 detect a falling +5 V supply and pull the $\overline{\text{RESET IN}}$ input low to avoid spurious operation on receiver power down or power loss. At such times, the chip select to CMOS RAM U8 is disabled by FET Q5, before the RAM enters its battery-backed condition.

During normal program execution, the microprocessor SOD output sends a low active pulse to the re-triggerable one-shot U20 every millisecond. If the CPU is so affected by noise on the busses or some other failure that it fails to do this, the one-shot will time out and restart the microprocessor through the 8085A TRAP input. Components C20 and R9 set this one-shot timeout to 50 milliseconds. The one-shot is also reset on powerup.

3.3 Memory

The firmware program is stored in the three 2732 4K byte EPROMS U5, U6, and U19. The program steps and data contained in these devices are accessed by the chip selects from U2 to each EPROM, gated onto the data bus with an output enable from the RD signal.

The information stored in the EPROMS is part of the RF-590 software and cannot be altered by the customer.

CAUTION

EPROMs are ultraviolet erasable over extended periods of exposure to fluorescent light or sunlight which can erase the memory information. Do not remove the opaque protective shield on these devices.

The 8155 circuit (U7) contains 256 bytes of RAM which are used for temporary storage by the software program. This device also contains a programmable timer which is conditioned to output a 1 kHz square wave to the RST 7.5 interrupt input of the CPU. This signal is the real time clock which is used to time and coordinate many RF-590 processes.

CAUTION

Do not short out the memory backup battery terminals. This could result in severe circuit damage.

The 6516 2K byte static CMOS RAM (U8) contains the channel storage. A fully charged battery BT1 in the backup power supply should maintain channel storage for one month. In normal receiver operation, the trickle charge circuit will recharge a dead battery in 24 hours. Terminals E1-E2 left unjumped, isolate the battery from the board circuitry for prolonged storage without maintaining channel memory to prevent battery discharge. However, E1 and E2 must be connected prior to operating the receiver to provide the battery backup provision, and to avoid damage to U8.

3.4 Parallel Input/Output

The 8155 (U7) provides 22 lines of parallel I/O, one eight-bit output port, another six-bit output port, and the eight-bit input port. The 8255 I/O device (U9) provides another 24 lines, configured as two eight-bit input ports and one, eight-bit output port. Both of these circuits provide a means of monitoring as well as controlling signal lines from both the receiver and front panel sections of the RF-590.

The modules associated with these parallel ports are shown in table 2.

Table 2. Control Board Port-to-Module Correlation

Port	Associated Modules
U7 port A:	Rear panel, BFO, PLL III, PLL IV
U7 port B:	IF/Audio, BFO assemblies
U7 port C:	IF filter assembly
U9 port A:	Rear panel and input assemblies
U9 port B:	Reference generator and input assemblies, PLL I, PLL IV, preselector option
U9 port C:	Front panel, PLL II, Meter

Additionally, DIP switch S2 is read by the processor through buffer U21 to determine the filter types used in the particular receiver (see section 4.0).

3.5 Serial I/O

Control Board A14 sends most of its control signals out as serial data. The serial data transmission circuit consists of U16, U17, and U18. Dual flip-flop U16 divides the processor output clock by four and clocks U18 and U17, producing the synchronous 750 kHz serial clock signal sent throughout the receiver. Parallel data written to U17 is shifted out onto the serial data line (high order bit first), while U18 counts eight bits transmitted before clearing U16 and ending the serial transmission. The address then written to decoder U14 produces a 1-of-16, high-active strobe to the module which must use the newly transmitted serial data.

3.6 Analog I/O

A/D converter (U10) handles analog inputs. Most inputs come from BITE circuits. One input comes from the RF gain potentiometer on the front panel, which in local mode is sampled every 50 milliseconds. The result is sent serially to the D/A converter made up of U11, R28, and the low pass U13 buffer. This two step process is done to enable full control of RF gain through the optional remote control as well as the front panel control. The U13 output should track local rotation of the RF gain potentiometer over the range of 0 to 9 volts. A reference voltage of +5 volts is provided to the A/D and D/A components from regulator VR1. Dual flip-flop U15 divides the CPU 3 MHz clock by four for converter U10, whose end-of-conversion output is output to an input port of U9.

4. BANDWIDTH SELECTION

The RF-590 Receiver can support a variety of IF filters (with several bandwidth and configuration options available). For CW, AM, and sideband modes, several bandwidths may be scrolled through from the front panel depending on customer ordered setup. In order to support the many combinations possible, the selected option is indicated to the microprocessor by switch S2 on Control PWB A14. Thirty-two combinations are presently supported, and the one used is indicated by the setting of the five switch sections S2-4 through S2-8. The last three IF filter board positions are used for filter combinations for AM, CW, or FSK modes and may be empty in a given application. Switch positions S2-1 through S2-3 on the A14 PWB are used to indicate such a condition. When the switch is OPEN, it indicates a filter present and when it is CLOSED, it shows the slot is empty.

Table 3 lists a typical filter complement for the RF-590.

Table 3. Typical Filter Complement

Mode	IF Bandwidths
LSB	2.8 kHz
USB	2.8 kHz
CW	0.3 kHz
CW	1.0 kHz
AM	3.2 kHz
AM	6.8 kHz
AM	16.0 kHz
FM	16.0 kHz

This setup uses configuration number 30, and leaves the last IF BW slot empty. The configuration number is expressed as a binary number with OPEN switch sections representing bit = 1. Therefore,

Configuration 30 = 11110 binary (S2-4 through 8)

Final filter slot empty, S2-1 CLOSED

Result:

S2-1	CLOSED
S2-2, S2-3	OPEN
S2-4 through S2-7	OPEN
S2-8	CLOSED

The configuration for a given receiver is factory set, and should not have to be altered by the customer. If S2 is to be replaced, its pattern should be recorded and the replacement set similarly after installation.

5. MAINTENANCE

5.1 Alignment

Control PWB Assembly A14 requires no adjustment for proper operation.

5.2 Troubleshooting

Although most of the circuitry on this assembly is controlled directly or indirectly by the microprocessor, a practice of standard digital troubleshooting methods will isolate most faults to the component level. A logic HIGH is the level between 3 and 5 volts, and a proper logic LOW typically is between 0 and 1 volt. The circuit area involved in minor faults can typically be determined by BITE fault codes, or by using paragraph 3, Functional Description in this section. More general or major failures are best handled by proceeding in order through the checks outlined below.

5.2.1 CPU

If the microprocessor is running, it is capable of debugging several circuits on the A14 PWB by itself. However, it must first be determined if the 8085A is operating.

These inputs must be present in order for the device to run. Table 4 lists the operational inputs for the CPU.

Table 4. Operational Inputs for CPU

Pin	Signal
U1-1, 2	Crystal inputs - 6 MHz
U1-36	Reset input - HIGH
U1-6	Trap input - LOW
U1-35	Ready - HIGH
U1-39	Hold - LOW

A14 PWB +5 V supply should be between +4.75 and +5.1 volts. Table 5 lists the CPU outputs that should be present.

Table 5. Operational Outputs for CPU

Pin	Signal
U1-37	Clock out - 3 MHz square wave
U1-3	Reset out - LOW
U1-31	Write - active low pulses
U1-32	Read - active low pulses
U1-30	Address latch enable - active high pulses
U1-4	SOD - active low pulses at 1 millisecond intervals

When the CPU is running and executing the application software, its outputs will only be active a portion of each millisecond. The rest of the time it will be halted, waiting for a real time clock interrupt from U7.

5.2.2 Trap and Reset Circuits

The trap circuit is provided to restart the CPU in the software if the device loses synchronization due to high noise levels on its busses. One-shot U20 is retriggered before timeout from U1, pin 4, the SOD output. The software will generate a low active pulse every millisecond if it is executing properly and if it gets the real time clock interrupt. Low voltage on the +5 supply to this board will cause a reset of the processor due to the reset circuit Q2-Q4.

5.2.3 Device Selection

Address decoder U2 aids the access of devices through the data bus by outputting low active chip enable signals corresponding to the address on the high order bits of the CPU. During normal operation, the enables from U2 should be seen on pin 18 of U5, U6, U8, and U19, as well as U7-8. The select on U9-6 should be active immediately following changes in the frequency entered through keyboard or tune knob. Active high selection pulses on A/D converter U10 are visible at least every 50 milliseconds in local receiver operation.

5.2.4 Memory Circuits

It can be very difficult to troubleshoot memory problems if the 8085A is not operating. If the CPU is running, it can find some problems itself. If the BITE routine indicates a PROM checksum fault, the fact that it is running indicates that the data bus buffers are operating and the PROMs are accessed. However, invalid data in these devices would require replacement of PROMs U5, U6, and U19.

If the BITE routine indicates a CMOS RAM fault, check that the enable pulse is getting to RAM U8 and check the voltage on U8-24. FET Q5 is driven by an enable from U2 as a switch to select U8. The chip enable should put Q5's gate at 8.5 Vdc to turn on the switch. The CMOS RAM is not connected directly to the +5 volt supply and E1-E2 must be jumpered to avoid damaging the RAM when the power is turned on.

5.2.5 Real Time Clock

As mentioned before, the 1 kHz square wave output from 8155 (U7) is used to interrupt the CPU to synchronize and time many RF-590 processes including the processor reset of the TRAP one-shot circuit U20. If this digital clock is not seen at U1-7, it should be checked at U7-6. The 3 MHz input to U7-3 from U1-37 should also be present. Any improper real time clock operation can be traced to U1, U7, or their interconnection.

5.2.6 Serial I/O

Control PWB A14 communicates with the display control board through its serial output circuit (U14, U16, U17, and U18). If this circuit fails the display will light up but will never change from its power up lamp test.

When the control board is operating normally, it will attempt to update the complete display once every second. Every second there will be a burst of 64 bytes to the display control board (two bytes of serial data sent every millisecond for a 32 millisecond total duration). There will be a strobe pulse (following every two bytes) to the display control board from U14-5.

The BITE routine tests the serial output circuit by sending a test pattern to four PLLs and reading back a test bit from each. If it can set (high) and reset (low) all four test bits, it assumes that the serial output circuit on the A14 PWB is operating. If any one test bit cannot be set and reset, it assumes a problem with that PLL.

Signals of interest in the serial data transmission circuit are listed in table 6.

Table 6. Significant Serial Data Transmission Circuits

Component	Function
U16-3	Clock in -3 MHz, square wave
U16-1, 13	Serial clock enable - High while data shifting out, 11 microseconds
U15-5, 11	1.5 MHz, square wave
U16-8, 9	750 kHz, square waves, opposite polarity
U17, 18 - 1	Serial port enable, narrow low active pulse
U17-9	Serial data

Table 6. Significant Serial Data Transmission Circuits (Cont.)

Component	Function
U16-8	Serial clock
U14-5	Display control board strobe, 30 narrow high active pulses every second

5.3 Parallel I/O

Parallel I/O is centralized through the ports on U7 and U9. If there is a BITE or operational problem concerning the modules (listed above) that are controlled by the lines from these parallel circuits, but the module in question is not at fault, port failure may be indicated. Improper operation of front panel scanned keypad, A/D converter output U10-13, or tune knob may be caused by defective U9.

5.4 Analog I/O

5.4.1 Analog Inputs

If not in remote or test, the control board tries to update the RF gain every 50 milliseconds, using A/D converter U10. Starting the conversion consists of two writes to U10, narrow high-active pulses on U10-16. Ten microseconds later the end of conversion (EOC) line will go low. It will stay low for 100 microseconds and after it goes high again there will be one narrow high active pulse on U10-21. The above is true for all the other analog inputs sampled during the execution of BITE. Signals of interest in the analog input circuit are listed in table 7.

Table 7. Significant Analog Input Circuits

Component	Function
U15-3	Clock in -3 MHz, square wave
U15-5, 11	1.5 MHz
U15-9	Clock out - 750 kHz, square wave
U10-22	Clock in - 750 kHz, square wave
U10-16, 32	Start conversion. Two narrow high going pulses, every 50 milliseconds
U10-13	End of conversion. 85 microseconds low, every 50 milliseconds
U10-21	Output enable narrow high going pulse, every 50 milliseconds
U10-15, 18	Multiplexer out, comparator in

5.4.2 Analog Outputs

During normal receiver operation, the D/A converter will track the RF gain potentiometer. U11 is a serial in/parallel out shift register. When the A/D finds a changed value for the RF gain, the digital value will be shifted into U11. The resulting bit pattern on the resistor network will cause R28, pin 16, output to track the RF gain potentiometer from 0-5 volts. U13 buffers and filters this voltage and its output will vary from 0-9 volts.

5.5 Faults Detected Through BITE

The four fault areas on A14 detectable through BITE are listed in table 8.

Table 8. Fault Areas on Control Board A14

Fault	Failure
Fault 01:	PROM failure - The binary checksum calculated from the contents of programmed U5, U6, and U19 do not match value programmed by the factory. Validity of firmware is doubtful, and all three devices should be replaced.
Fault 02:	8155 RAM failure - Errors are found in the ability to store and retrieve data in the 256 byte RAM of U7. Replace U7.
Fault 03:	CMOS RAM failure - Errors are found in the ability to store and retrieve data in U8. Replace U8. Check E1-E2 jumpering, BT1, Q5, and associated circuits.
Fault 04:	Serial data failure - Faulty serial transmission is detected. Check U14 and U16 through U18.

6. PARTS LIST

Table 9 is a comprehensive parts list of all replaceable components in Control Board Assembly A14. When ordering parts from the factory, include a full description of the part. Use figure 1, Control Board Assembly A14 Component Location Diagram to identify parts.

7. SCHEMATIC DIAGRAM

Figure 2 is the Control Board Assembly A14 schematic diagram.

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Table 9. Control Board Assembly A14 Parts List (PL 10073-2800)

Ref. Desig.	Part Number	Description
	10073-2800	PWB, CONTROL BOARD
BT1	B41-0009-004	BAT NICAD 3.6V -20/ + 70C
C1	M39014/01-1535	CAP .01UF 20% 100V CER
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	C26-0010-680	CAP 68UF 20% 10V TANT
C6	C26-0010-680	CAP 68UF 20% 10V TANT
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	C26-0010-680	CAP 68UF 20% 10V TANT
C9	M39014/02-1310	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310	CAP .1UF 10% 100V CER-R
C12	C26-0050-109	CAP 1.0UF 20% 50V TANT
C13	C26-0016-479	CAP 4.7UF 20% 16V TANT
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310	CAP .1UF 10% 100V CER-R
C17	M39014/02-1310	CAP .1UF 10% 100V CER-R
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	C26-0010-680	CAP 68UF 20% 10V TANT
C20	C26-0050-109	CAP 1.0UF 20% 50V TANT
C21	M39014/02-1310	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310	CAP .1UF 10% 100V CER-R
C26	C26-0016-150	CAP 15UF 20% 16V TANT
C28	M39014/02-1310	CAP .1UF 10% 100V CER-R
C29	M39014/02-1310	CAP .1UF 10% 100V CER-R
C30	C26-0010-221	CAP 220UF 20% 10V TANT
C31	C26-0010-221	CAP 220UF 20% 10V TANT
C32	M39014/02-1310	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	M39014/02-1318	CAP .33UF 10% 50V CER-R
C39	C25-0001-313	CAP 100UF 20% 20V TANT
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C42	C26-0010-221	CAP 220UF 20% 10V TANT
C43	C26-0010-221	CAP 220UF 20% 10V TANT
C44	C26-0016-479	CAP 4.7UF 20% 16V TANT
CR1	1N4454	DIODE 200mA 75V SW
CR2	1N4454	DIODE 200mA 75V SW
CR3	1N4454	DIODE 200mA 75V SW
CR4	1N4454	DIODE 200mA 75V SW

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Table 9. Control Board Assembly A14 Parts List (PL 10073-2800) (Cont.)

Ref. Desig.	Part Number	Description
CR5	1N4454	DIODE 200mA 75V SW
CR6	1N4454	DIODE 200mA 75V SW
E1	SE23XC02	TRM
E2	SE23XC02	TRM
J1	J46-0032-004	HDR 4 PIN 0.100" SR
J2	J46-0013-014	HDR 14 PIN 0.100" DR SHRD
J3	J46-0032-010	HDR 10 PIN 0.100" SR
J4	J46-0032-010	HDR 10 PIN 0.100" SR
J5	J46-0013-014	HDR 14 PIN 0.100" DR SHRD
J6	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J7	J46-0031-010	HDR 10 PIN 0.100" RT ANG
J8	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J9	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J10	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J11	J46-0031-020	HDR 20 PIN 0.100" RT ANG
J12	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J13	J46-0031-016	HDR 16 PIN 0.100" RT ANG
J14	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J15	J46-0013-040	HDR 40 PIN 0.100" DR SHRD
L1	10073-7034	INDUCTOR, 440UH
L2	L-0644	COIL 220UH 10% FXD RF
L3	10073-7034	INDUCTOR, 440UH
L4	MS75085-5	INDUCTOR
L5	10073-7029	INDUCTOR, FILTER CHOKE
L6	10073-7034	INDUCTOR, 440UH
Q1	2N2222	XSTR SS/GP NPN TO-18
Q2	2N2907	XSTR SS/GP PNP TO-18
Q3	2N2222	XSTR SS/GP NPN TO-18
Q4	2N2907	XSTR SS/GP PNP TO-18
Q5	3N170	XSTR MOSFET
Q8	2N2222	XSTR SS/GP NPN TO-18
R1	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R2	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R9	R65-0003-114	RES 110K 5% 1/4W CAR FILM
R10	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R11	R65-0003-122	RES 1.2K 5% 1/4W CAR FILM
R12	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R13	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R14	R65-0003-243	RES 24K 5% 1/4W CAR FILM
R15	R65-0003-204	RES 200K 5% 1/4W CAR FILM
R16	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R17	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R18	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R21	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R22	R65-0003-103	RES 10K 5% 1/4W CAR FILM

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Table 9. Control Board Assembly A14 Parts List (PL 10073-2800) (Cont.)

Ref. Desig.	Part Number	Description
R23	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R24	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R26	R50-0010-103	RES,10SIP, 10K,2.0%, 9RES
R27	R50-0010-103	RES,10SIP, 10K,2.0%, 9RES
R28	R53-0001-001	RES,DIP NETWORK R/2R
R29	R65-0003-393	RES 39K 5% 1/4W CAR FILM
R30	R65-0003-363	RES 36K 5% 1/4W CAR FILM
R31	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R32	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R33	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R35	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R36	R50-0010-103	RES,10SIP, 10K,2.0%, 9RES
R37	R50-0010-103	RES,10SIP, 10K,2.0%, 9RES
R38	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R39	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R40	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R41	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R42	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R43	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R44	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R45	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R46	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R47	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R48	R65-0003-363	RES 36K 5% 1/4W CAR FILM
S1	S06-0002-100	SW PB SPST NO MOM BLK PCT
S2	S50-0001-008	SW SPST 8SEC .1A SLD DIP
U1	I27-0006-002	IC 8085A MICRO 8-BIT CER
U2	I05-0000-042	IC 74LS42 PLASTIC TTL
U3	I05-0000-373	IC 74LS373 PLASTIC TTL
U4	I05-0000-245	IC 74LS245 PLASTIC TTL
U5**	SEE NOTE	IC SOFTWARE PROM
U6**	SEE NOTE	IC SOFTWARE PROM
U7	I26-0003-001	IC 8155-2 STAT RAM 256X8
U8	I26-0010-001	IC STATIC RAM CMOS 2048X8
U9	I59-0008-001	IC 8255 PLASTIC
U10	I40-0010-001	IC ADC0817 PLASTIC CMOS
U11	I01-0000-156	IC 4094B PLASTIC CMOS
U13	I30-0018-000	IC 1458 OP AMP PLASTIC
U14	I01-0000-202	IC 4514B PLASTIC CMOS
U15	I05-0000-074	IC 74LS74 PLASTIC TTL
U16	I05-0000-074	IC 74LS74 PLASTIC TTL
U17	I05-0000-165	IC 74LS165 PLASTIC TTL
U18	I05-0000-165	IC 74LS165 PLASTIC TTL
U19**	SEE NOTE	IC SOFTWARE PROM
U20	I05-0000-122	IC 74LS122 PLASTIC TTL

**NOTE: When ordering U5, U6, or U19, refer to the number located on the PROM label.

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Table 9. Control Board Assembly A14 Parts List (PL 10073-2800) (Cont.)

Ref. Desig.	Part Number	Description
U21	I05-0000-244	IC 74LS244 PLASTIC TTL
U22	I05-0000-000	IC 74LS00 PLASTIC TTL
U23	I01-0017-000	IC 7432 PLASTIC TTL
U24	I05-0000-032	IC 74LS32 PLASTIC TTL
U25	I05-0000-004	IC 74LS04 PLASTIC TTL
U27	I05-0000-004	IC 74LS04 PLASTIC TTL
VR1	I11-0008-005	IC VR 340 + 5V 0.1A 2%
XU1	J77-0008-007	SKT IC MACH 40 PIN
XU5	J77-0008-005	SKT IC MACH 24 PIN
XU6	J77-0008-005	SKT IC MACH 24 PIN
XU19	J77-0008-005	SKT IC MACH 24 PIN
Y1	Y15-0004-060	CRYSTAL, 6MHZ.

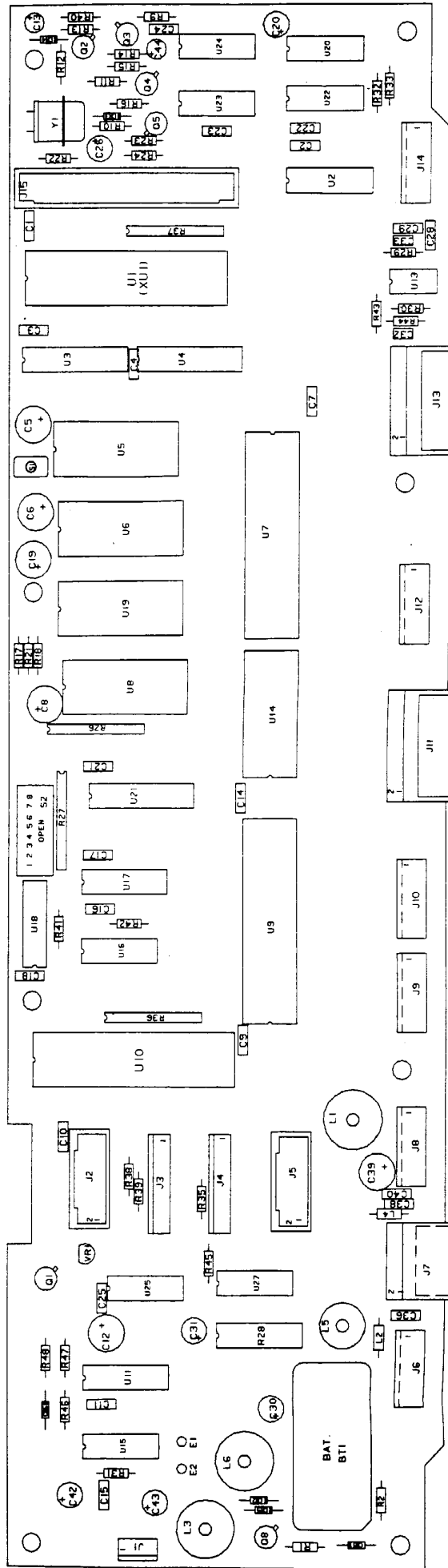
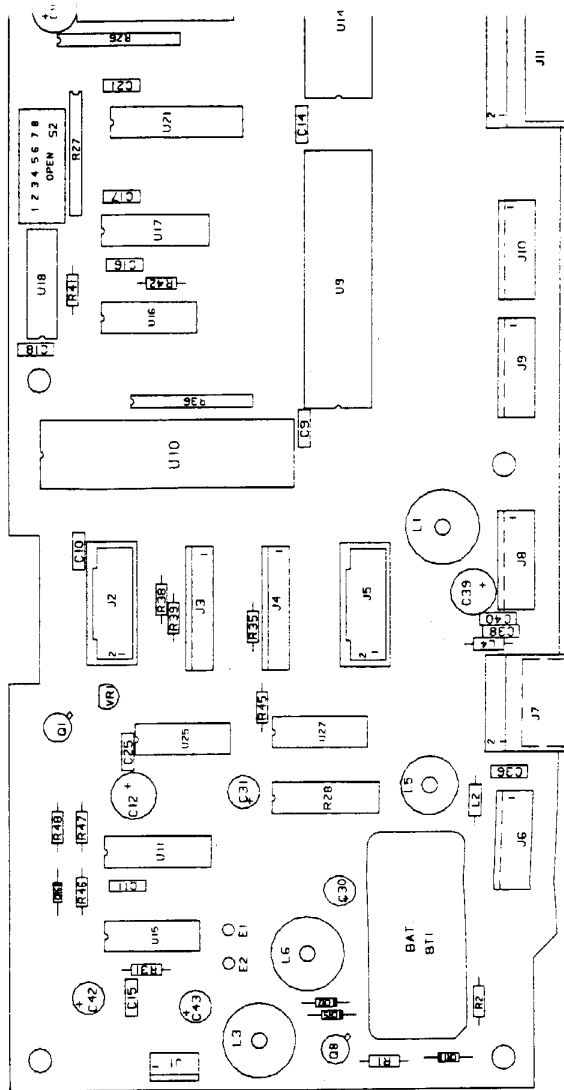


Figure 1. Control Board Assembly A14
Component Location Diagram
(10073-2800, Rev. G)



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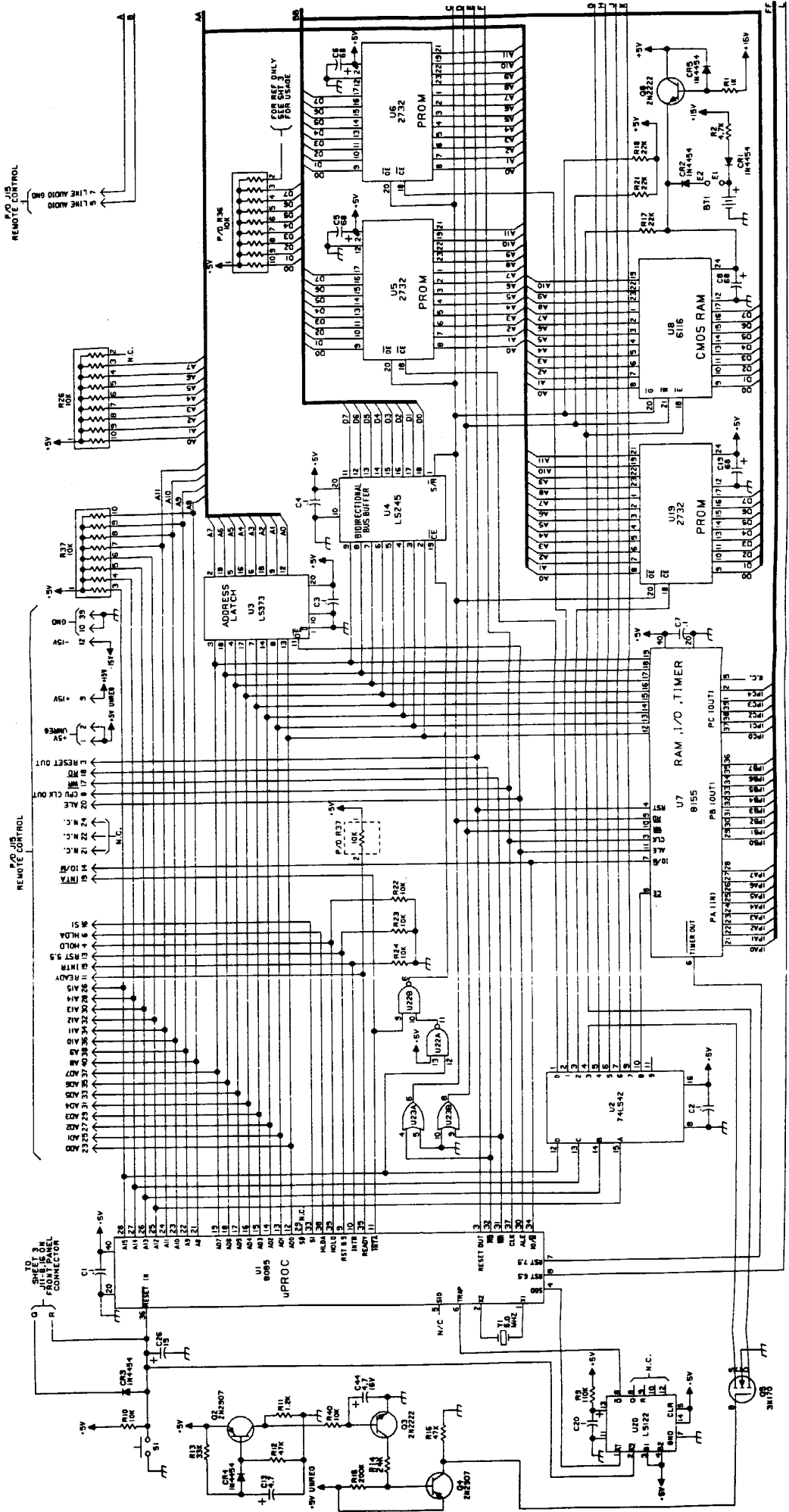


Figure 2. Control Board Assembly A14
Schematic Diagram (10073-2801, Rev. L)
(Sheet 1 of 3)

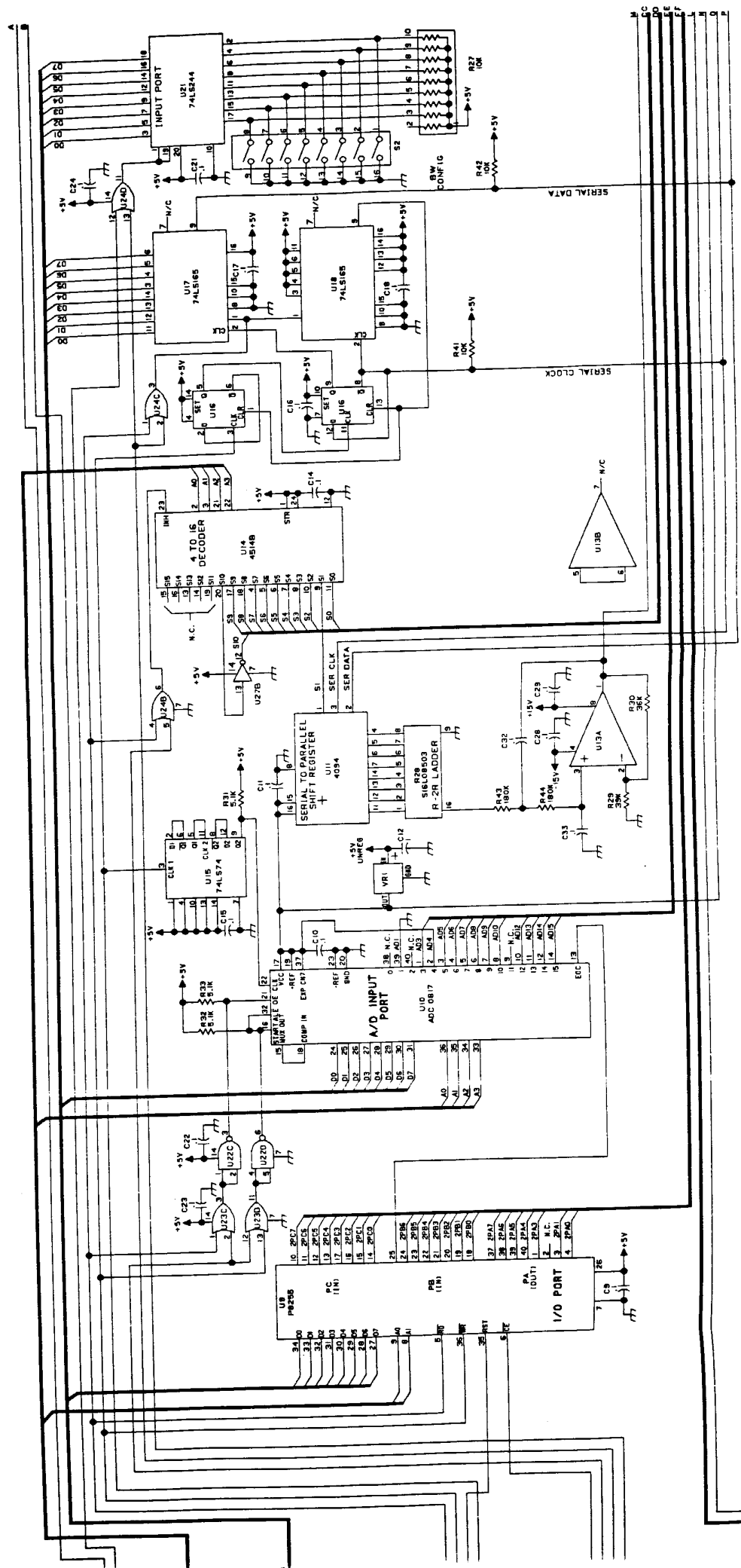
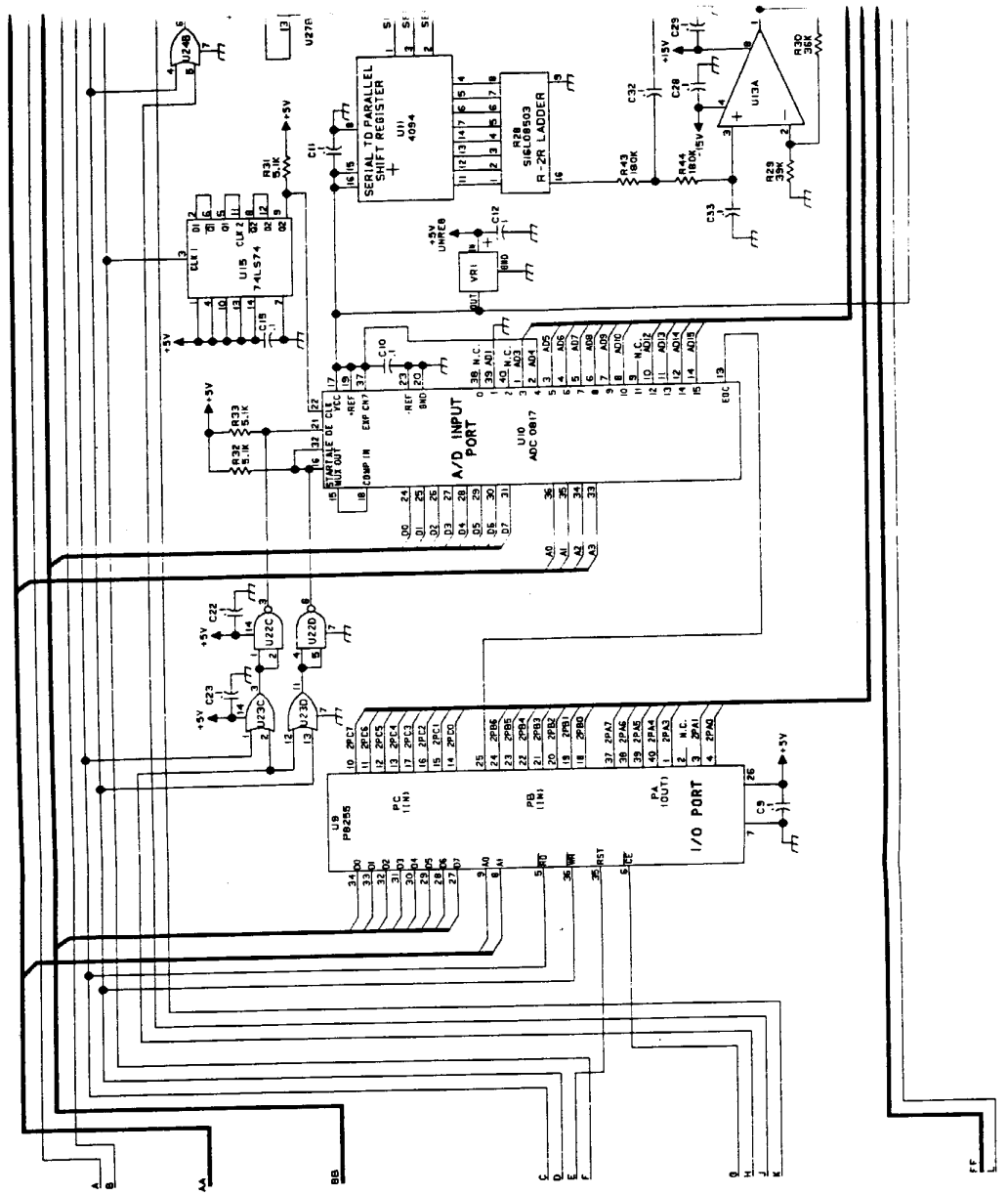


Figure 2. Control Board Assembly A14
Schematic Diagram (10073-2801, Rev. L)
(Sheet 2 of 3)



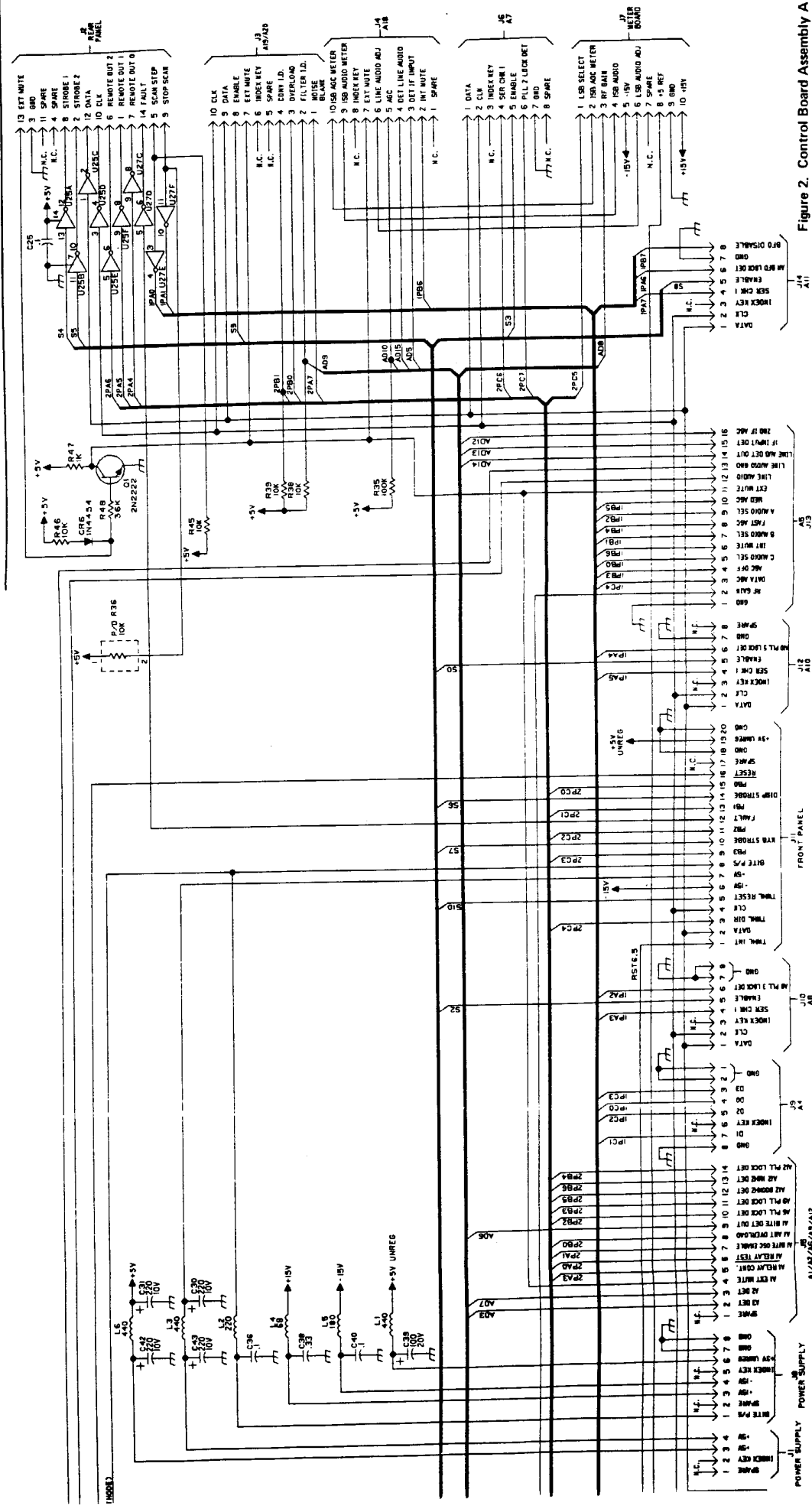
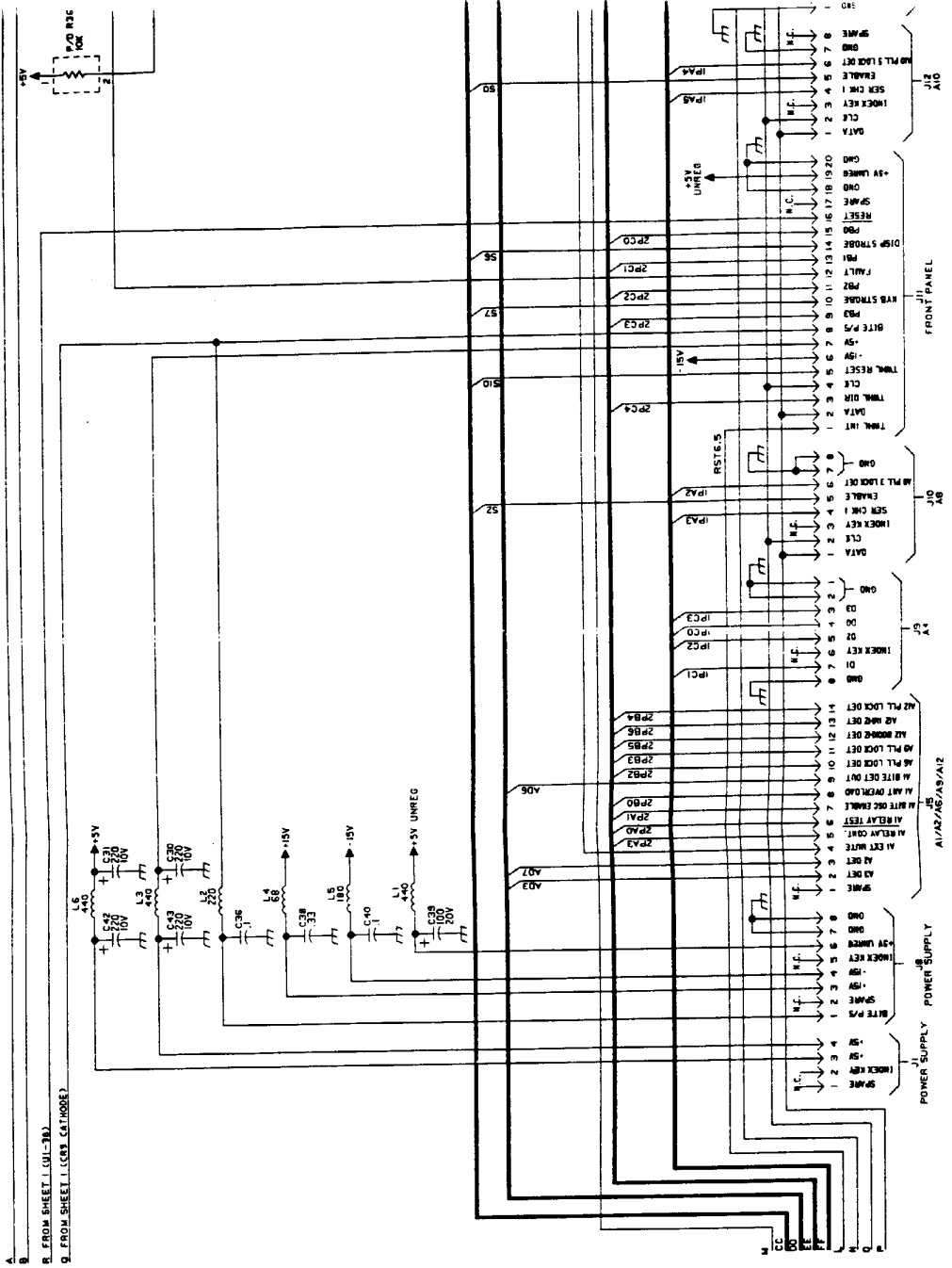


Figure 2. Control Board Assembly A14
Schematic Diagram (10073-2801, Rev. L)
(Sheet 3 of 3)



B. FROM SHEET I (01-78D)
 G. FROM SHEET I (08T CAT.MODE)