A23
+24-VOLT POWER SUPPLY ASSEMBLY

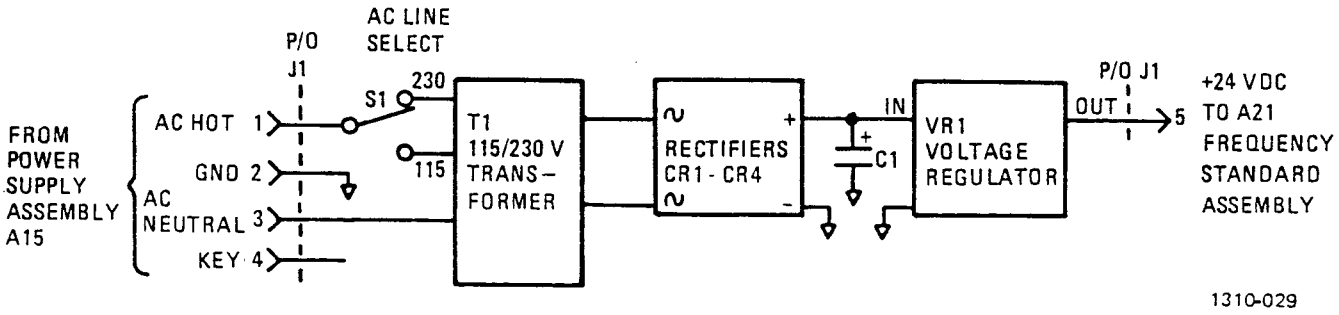


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

+ 24-VOLT POWER SUPPLY ASSEMBLY A23

WARNING

115 Vac or 230 Vac is applied to the A23 assembly whenever the exciter ac input line cord is connected to an ac source, regardless of the exciter ON/OFF power switch setting.

Do not attempt to remove this assembly or replace its input line fuse until the exciter ac power line cord is disconnected. Setting the ON/OFF power switch to OFF is insufficient to prevent a shock hazard.

Be certain that the protective cover over J1's mating connector is properly installed, since 115/230 Vac is present on that connector.

See paragraph 1 for 115/230 Vac selection and/or fuse replacement instructions.

1. GENERAL DESCRIPTION

Power Supply Assembly A23 provides + 24 Vdc at up to 300 mA to power the Frequency Standard Assembly A21. Figure 1 shows the position of Power Supply Assembly A23 in the chassis.

Ac input to this assembly comes directly from the exciter ac input connector that is part of Power Supply Assembly A15 line filter FL1. The power is tapped off before the exciter main fuse and power ON/OFF switch. Ac voltage is present at the assembly's input at all times when the exciter is plugged in. Frequency Standard Assembly A21 will always receive + 24 Vdc power, and remain constantly on, even when the exciter ON/OFF power switch is OFF. Frequency standard warm up and setting times are eliminated.

Switch S1 allows selection of 115 Vac or 230 Vac. An in-line fuse located in main Power Supply Assembly A15 must be changed when operating at 115 Vac, 230 Vac, or when replacing a blown fuse.

To select 115 Vac, 230 Vac, and/or replace fuse, follow the procedure listed below:

a. Disconnect exciter ac line cord.

b. Select desired ac line voltage to A23 Assembly with A23 switch S1 (115 Vac or 230 Vac), if not already selected.

c. Remove top cover of main Power Supply Assembly A15.

d. Locate the A15 assembly in line fuseholder W4F1.

e. Replace fuse as follows:

   1. For 115 Vac operation, use 1/4 ampere, 125 Vac slow-blow fuse.

   2. For 230 Vac operation, use 1/8 ampere, 250 Vac slow-blow fuse.

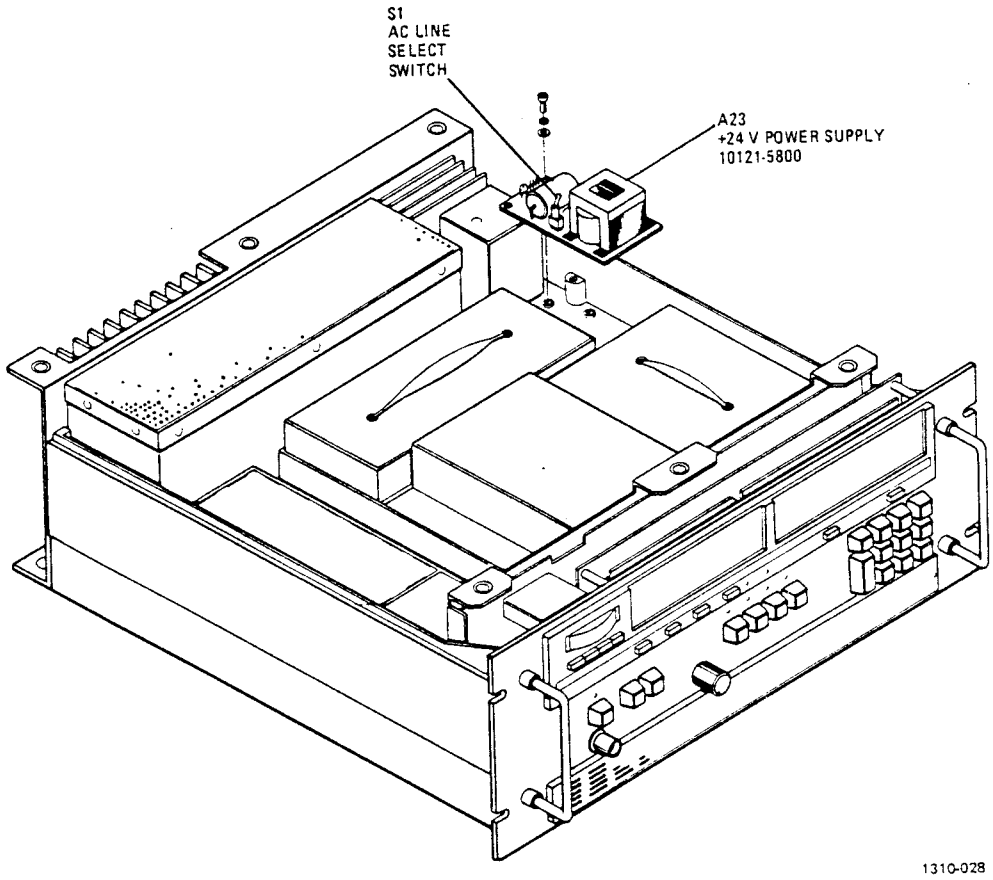


Figure 1. Power Supply Assembly A23 Location

f. Replace the A15 assembly cover and hardware.

g. Select desired ac line voltage to main Power Supply Assembly A15 (same value as step b), if not already selected. This is accomplished via respositioning the pc card and using the correct fuse in A15 assembly line filter FL1. Refer to subsection A15 of this manual.

h. Reconnect exciter ac line cord. Ac power will now be applied to the A23 assembly, regardless of the exciter ON/OFF switch position. Power for the rest of the exciter will be applied when the ON/OFF switch is set to ON.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. Power Supply Assembly A23 Interface Interconnections

Connector	Function	Characteristics
J1-1	Ac Hot	115 Vac or 220 Vac
J1-2	Ground	
J1-3	Ac Neutral	
J1-4	Index Key	Not used
J1-5	Dc Power	+ 24 Vdc at 300 mA maximum

3.CIRCUIT DESCRIPTIONS

Ac line voltage from J1 is supplied to ac line select switch S1 prior to application to the primary of transformer. The voltage across the T1 secondary is 28 V_{rms} under nominal line voltage. The ac signal is rectified by CR1 through CR4 to produce approximately 34 Vdc across filter capacitor C1. Voltage regulator VR1 regulates the output voltage to + 24 Vdc, over a wide range of ac line input voltages.

Note that generally, the full 300 mA capability is required only until the Frequency Standard Assembly has warmed up and stabilized. After that, current draw typically falls to about one-third of its warmup value of approximately 100 mA.

4. MAINTENANCE

4.1 General Information

In order to remove the A23 assembly for servicing:

a. Disconnect the exciter ac line cord.

b. Disconnect the J1 mating connector.

c. Remove the assembly's four mounting screws and heatsink block screw.

See paragraph 1, General Description, for replacement of fuses and/or 115/230 Vac line input selection.

WARNING

The heatsink block under VR1 should be secured to the chassis (or similar heatsink) whenever power is applied to the A23 assembly.

4.2 Output Voltage Test

a. Disconnect exciter ac line cord, and disconnect Reference Generator Assembly A12 connector J8.

b. Connect an 80-ohm, 7.5 watt (minimum) load to J1-5. At 24 Vdc output, the supply will then deliver 300 mA.

c. Configure FL1, A23 assembly, and fuses for 115 Vac as described in paragraph 1. Plug exciter into 115 Vac source.

d. With ac power applied, A23 assembly output should be 24 Vdc.

e. Configure FL1, A23 assembly, and fuses for 230 Vac as described in paragraph 1. Plug exciter into 230 Vac source.

f. With ac power applied, the output should be 24 Vdc.

g. Disconnect line cord, reconfigure FL1, A23 assembly, and fuses to desired operational input ac level.

h. Reconnect A12 J8 connector.

i. Test is now complete.

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components of Power Supply Assembly A23 are listed in table 2. Component locations are shown in figure 2. The schematic is shown in figure 3.

Table 2. Power Supply Assembly A23 Parts List

Ref. Desig.	Part Number	Description
A23	10121-5800	+ 24 VOLT POWER SUPPLY
	10121-5804	SHIELD, POWER SUPPLY
	X-0814	INSULATOR, TRANSISTOR
	M10-0006-000	WSHR SHLDR NYLON .12X.06L
C1	C17-0063-521	CAP 520UF 63V ELEC
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	C26-0050-159	CAP 1.5UF 20% 50V TANT
CR1	1N4007	DIODE 1A 1000V RECT GP
CR2	1N4007	DIODE 1A 1000V RECT GP
CR3	1N4007	DIODE 1A 1000V RECT GP
CR4	1N4007	DIODE 1A 1000V RECT GP
J1	J46-0032-005	HEADER, 5 PIN DISCRETE
R1	RN55D4421F	RES,4420 1% 1/8W MET FLM
R2	RN55D2430F	RES,243.0 1% 1/8W MET FLM
R3	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
S1	S10-0011-111	SW SP ON-NONE-ON TOG PCMT
T1	T40-0003-001	TRANSFORMER
VR1	IC-0358	IC VR 317 ADJ V 1.5A

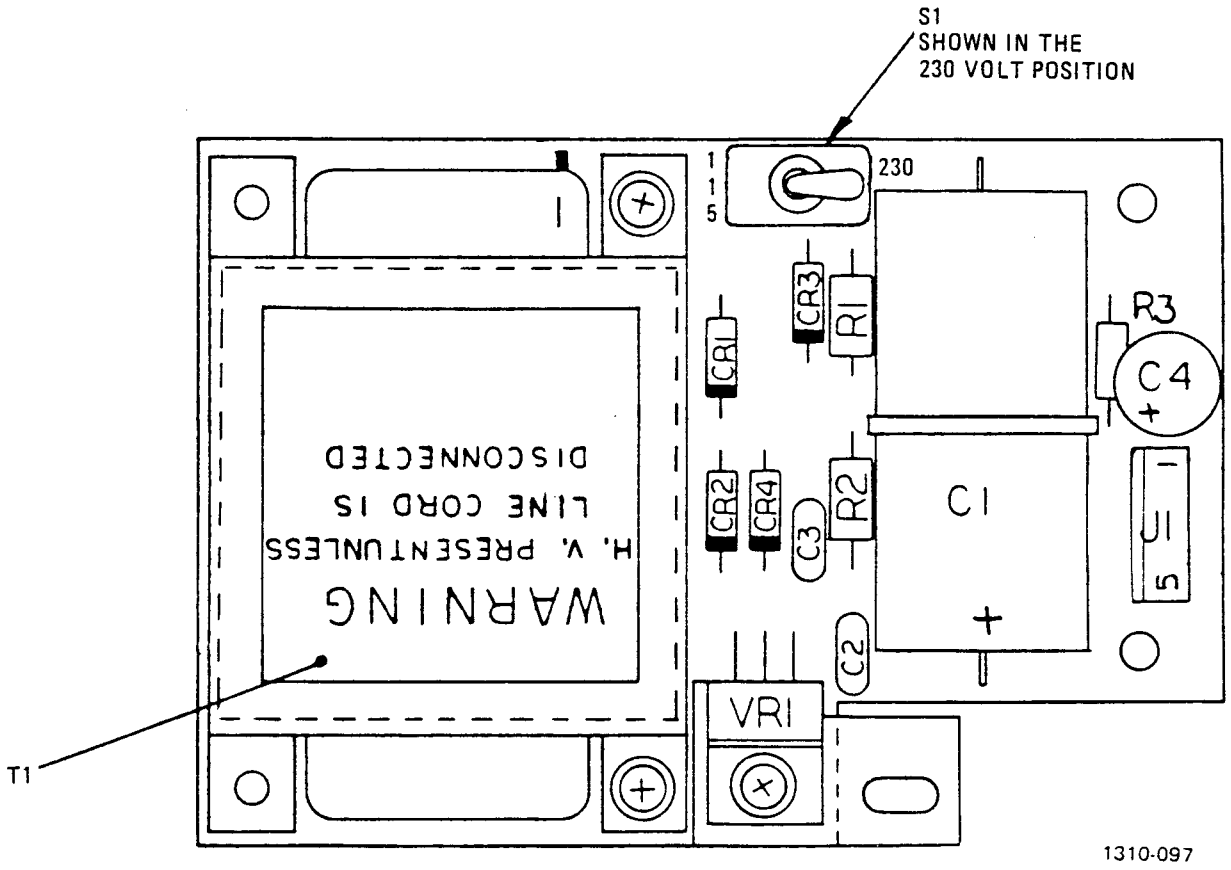


Figure 2. Power Supply Assembly A23 Component Location Diagram (10121-5800)

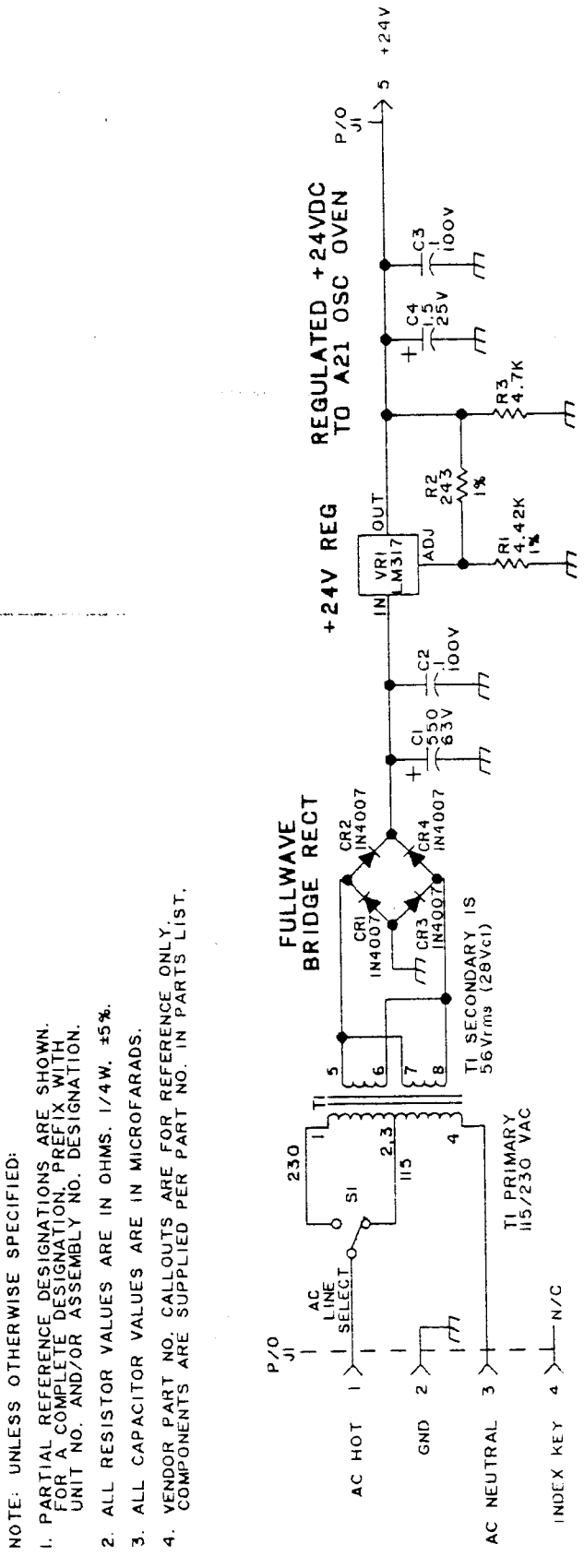


Figure 3. Power Supply Assembly A23 Schematic Diagram (10121-5801 Rev. A)

APPENDIX

DATA SHEETS

Data sheets are listed in alphanumeric order in table A-1.

Table A-1. Data Sheets

Table A-1. Data Sheets (Cont.)

Table A-1. Data Sheets

AD7523
8-BIT MONOLITHIC MULTIPLYING D/A CONVERTERS

FEATURES

- **8, 9 and 10 bit linearity**
- **Low gain and linearity Tempcos**
- **Full temperature range operation**
- **Full input static protection**
- **DTL/TTL/CMOS compatible**
- **+5 to +15 volts supply range**
- **Fast settling time: 100 nS**
- **Four quadrant multiplication**
- **883B Processed versions available**

GENERAL DESCRIPTION

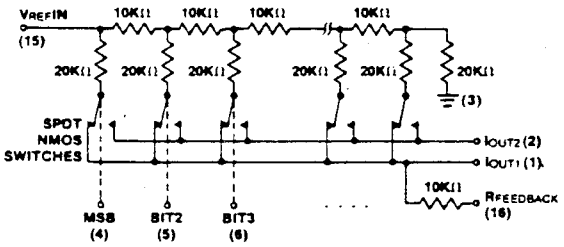
The Intersil AD7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

Intersil's thin-film resistors on CMOS circuitry provide 8-bit resolution (8, 9 and 10-bit accuracy), with DTL/TTL/CMOS compatible operation.

Intersil AD7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND and very low power dissipation make it a very versatile converter.

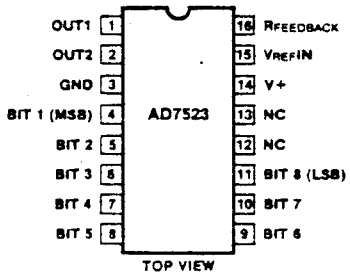
Low noise audio gain control, motor speed control, digitally controlled gain and attenuators are a few of the wide number of applications of the 7523.

FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

PIN CONFIGURATION



TOP VIEW

OUTLINE DRAWINGS
DE,PE

ADC0801 – ADC0804
8-BIT MICROPROCESSOR COMPATIBLE A/D CONVERTERS

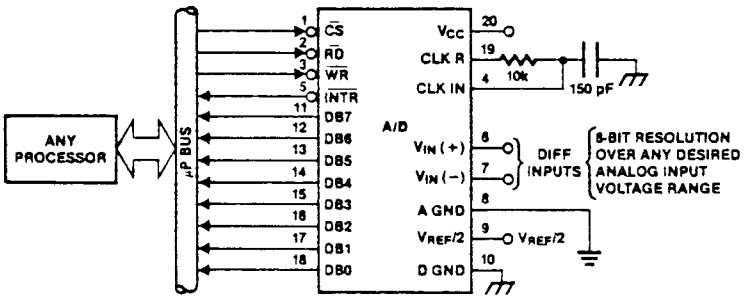
GENERAL DESCRIPTION

The ADC0801 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, hence no interfacing is required.

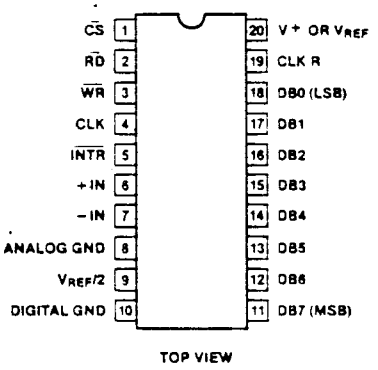
A differential analog voltage input allows increasing the common-mode-rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution. .

The ADC0801 family is available in the industry standard 20 pin CERDIP packages.

TYPICAL APPLICATION



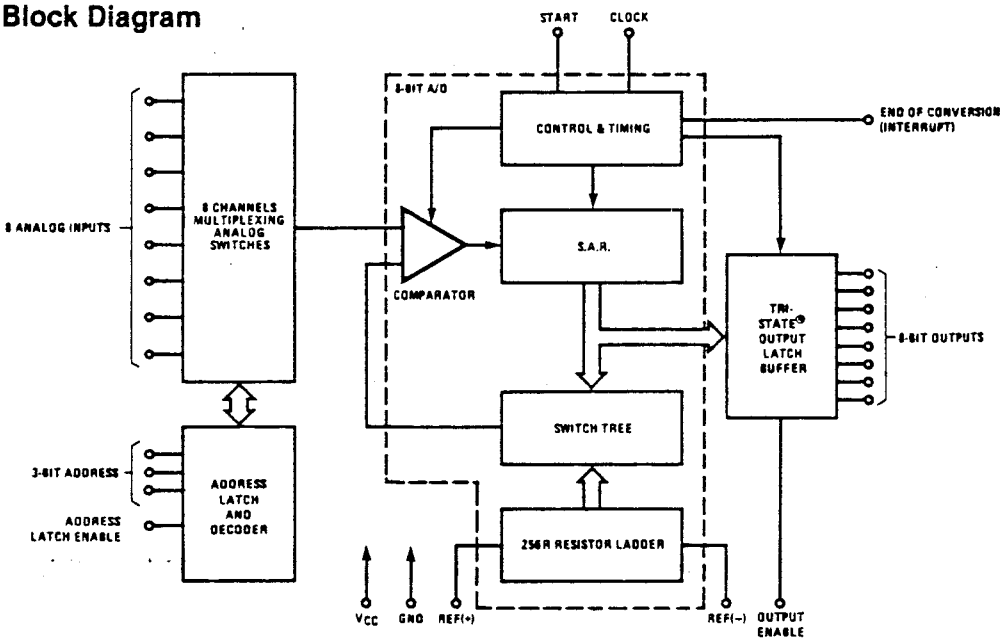
PIN CONFIGURATION



TOP VIEW

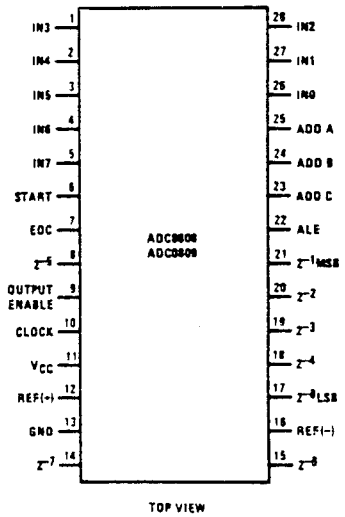
ADC0809
8-BIT uP COMPATIBLE AD/ CONVERTERS WITH 8-CHANNEL MULTIPLEXER

Block Diagram



SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

Dual-In-Line Package



TOP VIEW

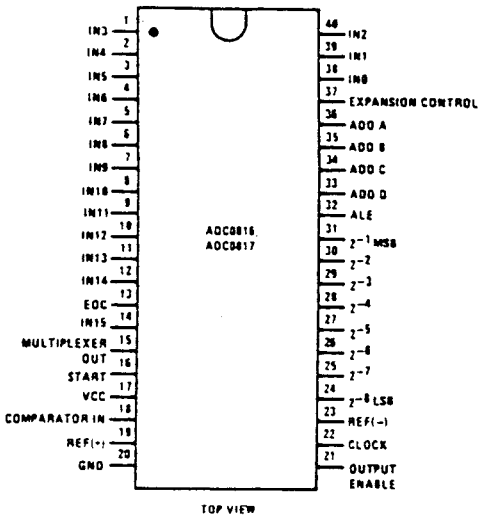
ADC0817
8-BIT uP COMPATIBLE A/D CONVERTERS WITH 16-CHANNEL MULTIPLEXER

General Description

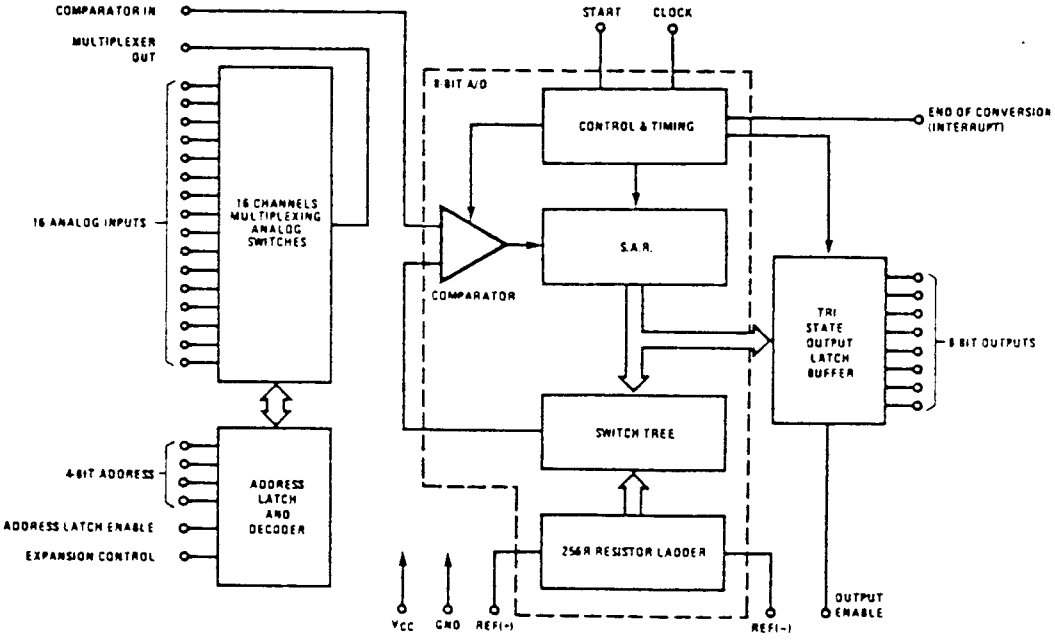
The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

Dual-In-Line Package



Block Diagram



CA3083
GENERAL-PURPOSE HIGH-CURRENT N-P-N TRANSISTOR ARRAY

RCA-CA3083 is a versatile array of five high-current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design. The CA3083 is supplied in a 16-lead dual-in-line plastic package, and the CA3083F in a 16-lead dual-in-line frit-seal ceramic package.

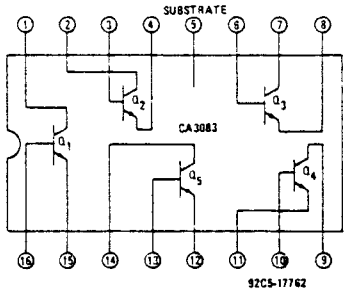
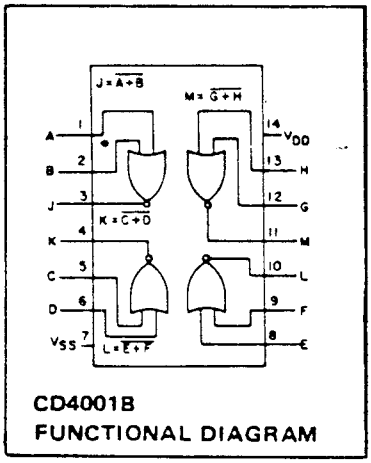


FIG. 1 – FUNCTIONAL DIAGRAM OF THE CA3083

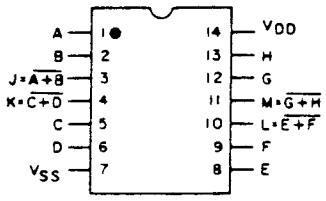
CD4001B TYPES
COS/MOS NOR GATES

High Voltage Types (20-Volt Rating)



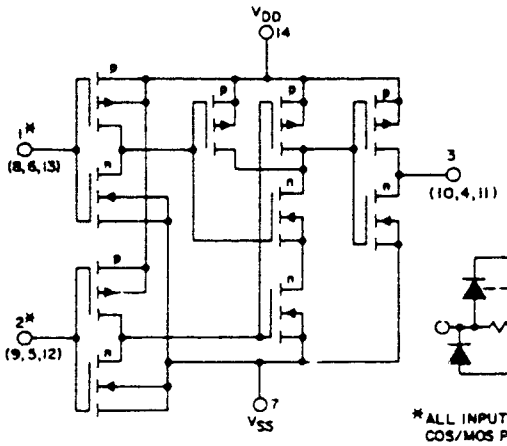
CD4001B
FUNCTIONAL DIAGRAM

TERMINAL ASSIGNMENTS (TOP VIEW)

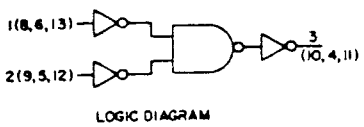


NC = NO CONNECTION

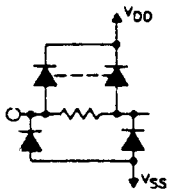
CD4001B



1 OF 4 GATES
(NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)



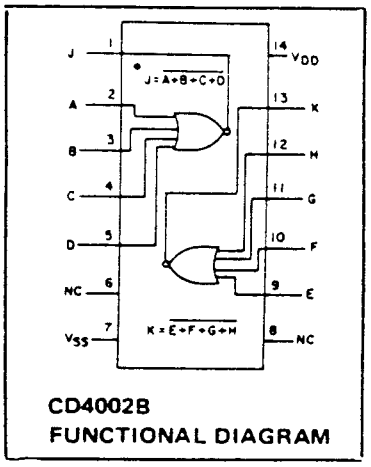
LOGIC DIAGRAM



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

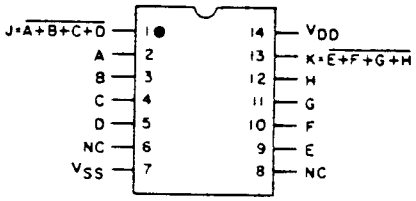
Schematic and logic diagrams for CD4001B.

CD4002B TYPES
COS/MOS NOR GATES



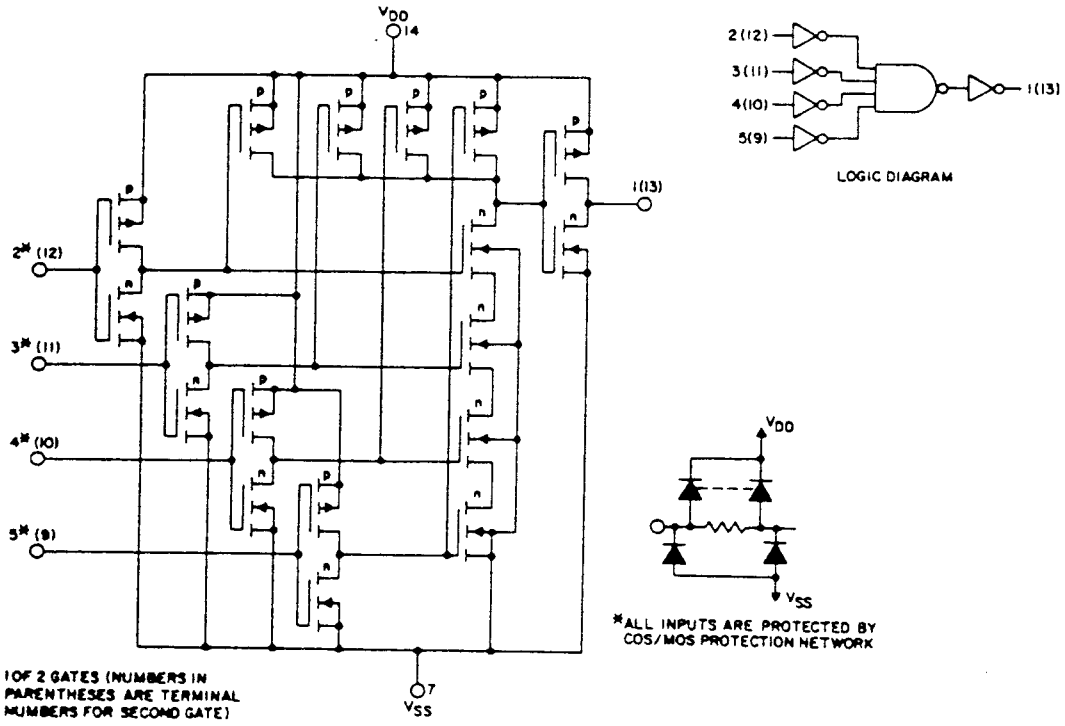
CD4002B
FUNCTIONAL DIAGRAM

TERMINAL ASSIGNMENTS (TOP VIEW)



NC = NO CONNECTION

CD4002B



1 OF 2 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR SECOND GATE)

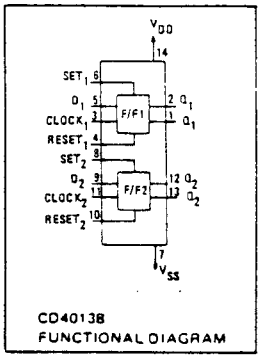
Schematic and logic diagrams for CD4002B.

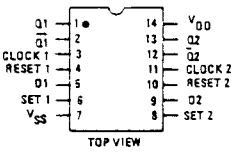
CD4013B TYPES
COS/MOS DUAL
'D'-TYPE FLIP-FLOP

High-Voltage Types (20-Volt Rating)

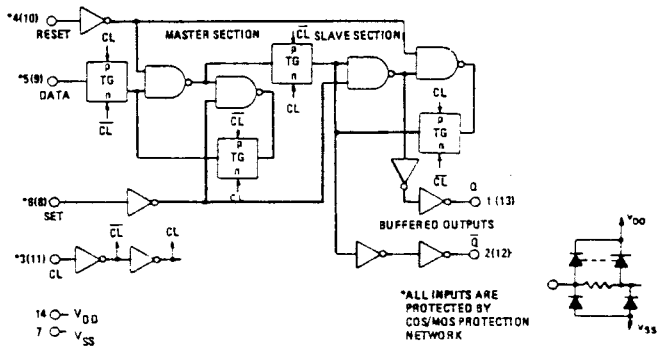
The RCA-CD40138 consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



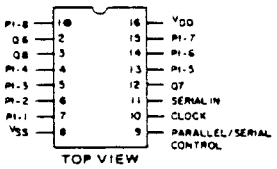


TERMINAL ASSIGNMENT

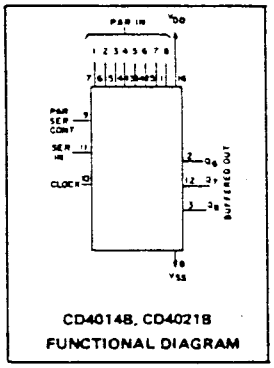


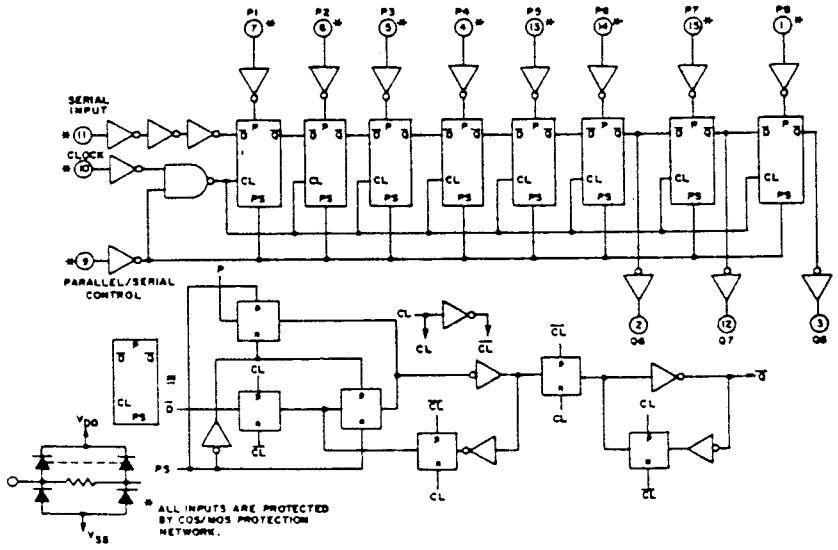
CD4021B TYPE
COS/MOS 8-STAGE
STATIC SHIFT REGISTERS

Asynchronous Parallel Input or
Synchronous Serial Input/Serial Output



TERMINAL DIAGRAM



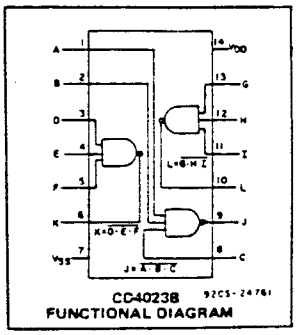


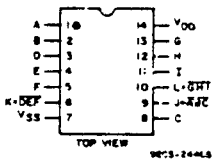
TRUTH TABLE – CD4021B

CL	Serial Input	Parallel/Serial Control	P1-8	P1-n	Q1 (internal)	Qn
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
↑	0	0	X	X	0	Qn-1
↑	1	0	X	X	1	Qn-1
↓	X	0	X	X	Q1	Qn

X = DON'T CARE CASE

CD4023B TYPES
COS/MOS NAND GATES
TRIPLE 3 INPUT



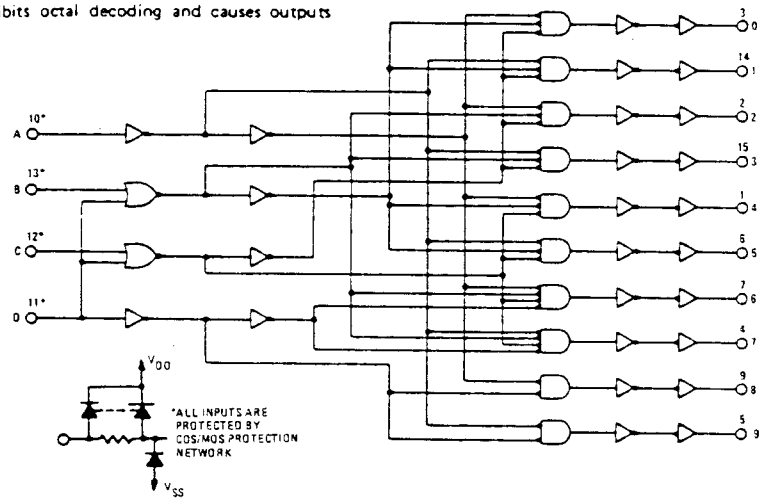


TERMINAL ASSIGNMENTS

CD4028A TYPES
COS/MOS
BCD-TO-DECIMAL DECODER

The RCA-CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse-shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low. If unused, the D input must be connected to V_{SS}. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).



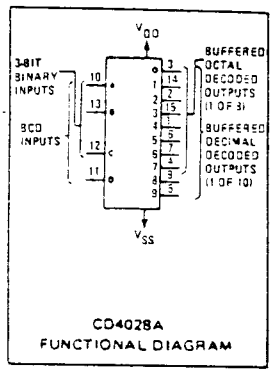


TABLE I – TRUTH TABLE

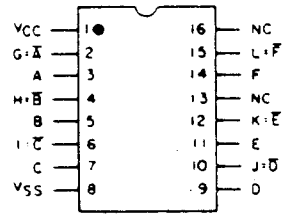
D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	*
0	0	0	1	0	1	0	0	0	0	0	0	0	0	*
0	0	1	0	0	0	1	0	0	0	0	0	0	0	*
0	0	1	1	0	0	0	1	0	0	0	0	0	0	*
0	1	0	0	0	0	0	0	1	0	0	0	0	0	*
0	1	0	1	0	0	0	0	0	1	0	0	0	0	*
0	1	1	0	0	0	0	0	0	0	1	0	0	0	*
0	1	1	1	0	0	0	0	0	0	0	1	0	0	*
1	0	0	0	0	0	0	0	0	0	0	0	1	0	*
1	0	0	1	0	0	0	0	0	0	0	0	0	1	*
1	0	1	0	0	0	0	0	0	0	0	0	1	0	**
1	0	1	1	0	0	0	0	0	0	0	0	0	1	**
1	1	0	0	0	0	0	0	0	0	0	0	1	0	**
1	1	0	1	0	0	0	0	0	0	0	0	0	1	**
1	1	1	0	0	0	0	0	0	0	0	0	1	0	**
1	1	1	1	0	0	0	0	0	0	0	0	0	1	**

* WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

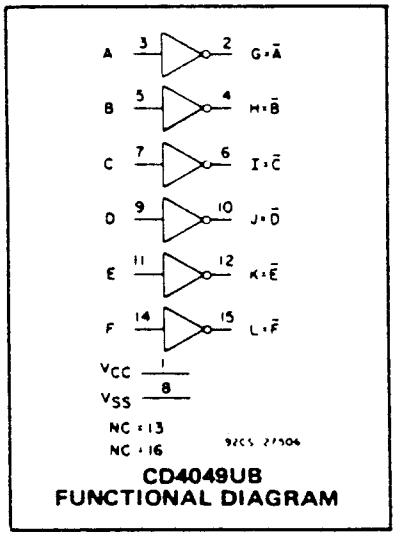
** EXTRAORDINARY STATES

CD4049B TYPE
INVERTING
COS/MOS HEX BUFFER/CONVERTER

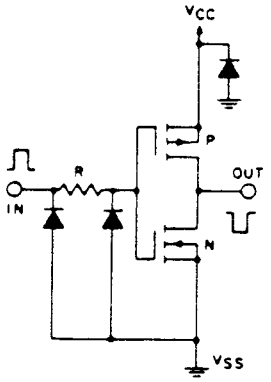
TERMINAL ASSIGNMENTS



NC = NO CONNECTION 92CS-24480R1



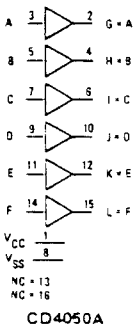
CD4049UB
FUNCTIONAL DIAGRAM



Schematic diagram of CD4049UB, 1 of 6 identical units

CD4050A
COS/MOS HEX BUFFER/CONVERTERS

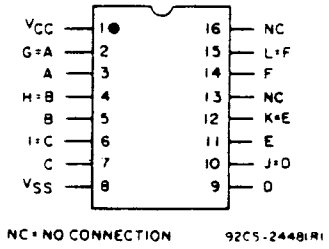
The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, V_{OL} ≤0.4 V, and I_{ON} ≥3.2 mA.)



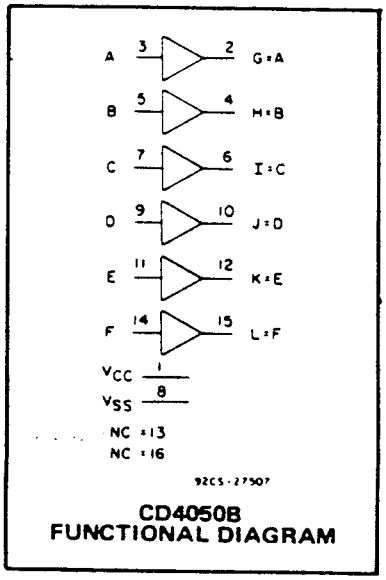
CD4050A

CD4050B TYPES
COS/MOS HEX BUFFER/CONVERTERS

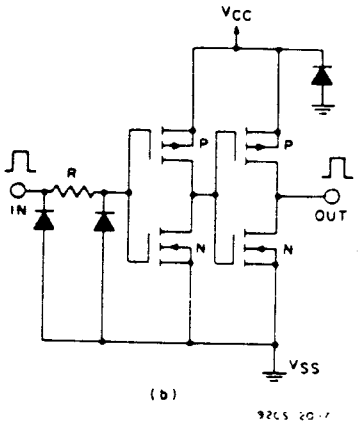
TERMINAL ASSIGNMENTS



CD4050B

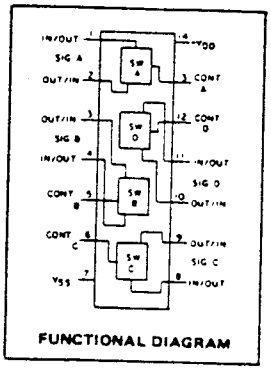


CD4050B
FUNCTIONAL DIAGRAM



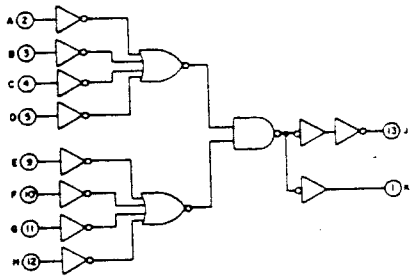
CD4066B TYPES
COS/MOS QUAD BILATERAL SWITCH
(For transmission or multiplexing of Analog or Digital Signals)

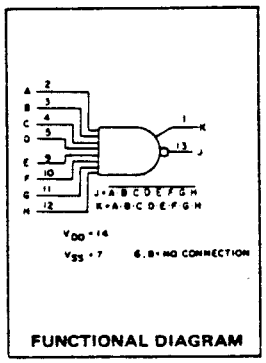
The CD4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. The well of the n-channel device on each switch is either tied to the input when the switch is on or to V_{SS} when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

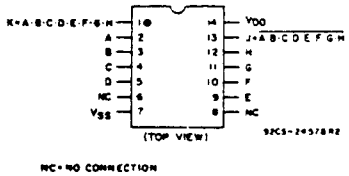


FUNCTIONAL DIAGRAM

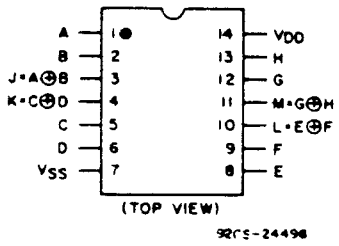
CD4068B TYPES
COS/MOS 8-INPUT
NAND/AND GATE



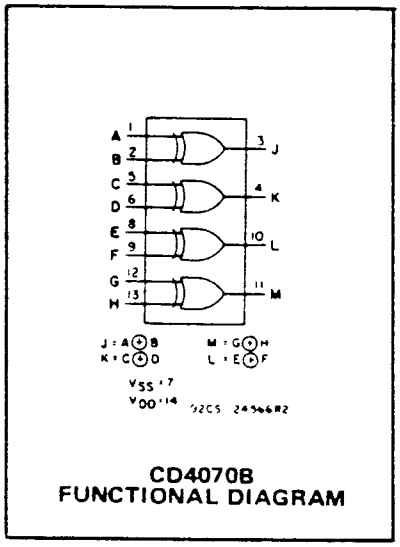




CD4070B TYPES
COS/MOS QUAD EXCLUSIVE–OR AND
EXCLUSIVE–NOR GATES



TERMINAL ASSIGNMENT
CD4070B



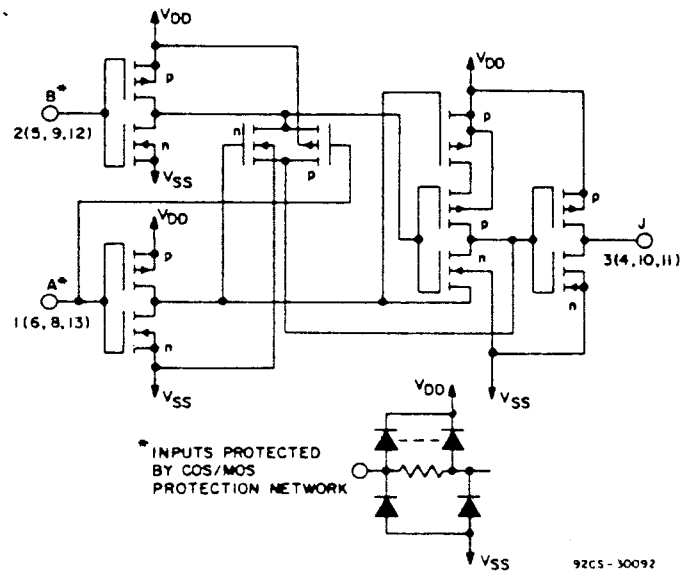


Fig. 1 – Schematic diagram for CD4070B (1 of 4 identical gates).

TRUTH TABLE CD4070B
1 of 4 Gates

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = HIGH LEVEL
0 = LOW LEVEL
J = A ⊕ B

CD4094B
COS/MOS
8-STAGE SHIFT-AND-STORE BUS REGISTER

High-Voltage Types (20-Volt Rating)

The RCA-CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

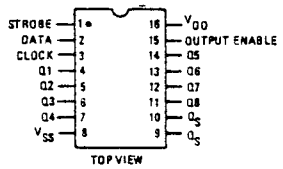
TRUTH TABLE

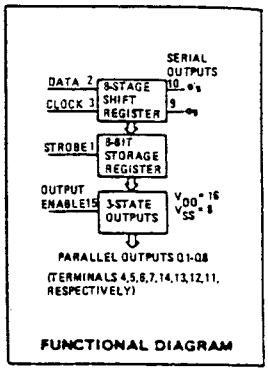
CL▲	OUTPUT ENABLE	STROBE	DATA	PARALLEL OUTPUTS Q1	PARALLEL OUTPUTS QN	SERIAL OUTPUTS QS	SERIAL OUTPUTS QS
⌐⌙	0	x	x	OC	OC	Q7	NC
⌙⌐	0	x	x	OC	OC	NC	Q7
⌐⌙	1	0	x	NC	NC	Q7	NC
⌙⌐	1	1	0	0	Q_{N-1}	Q7	NC
⌐⌙	1	1	1	1	Q_{N-1}	Q7	NC
⌙⌐	1	1	1	NC	NC	NC	Q7

▲= LEVEL CHANGE
X = DON'T CARE
NC = NO CHANGE
OC = OPEN CIRCUIT

LOGIC 1 = HIGH
LOGIC 0 = LOW

AT THE POSITIVE CLOCK EDGE INFORMATION IN THE 7TH SHIFT REGISTER STAGE IS TRANSFERRED TO THE 8TH REGISTER STAGE AND THE Q_S OUTPUT





FUNCTIONAL DIAGRAM

CD4098B TYPES
COS/MOS DUAL MONOSTABLE MULTIVIBRATOR

High-Voltage Types (20-Volt Rating)

The RCA-CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X.

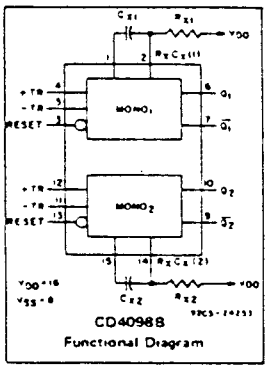
Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused −TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4098B is not used, its RESET should be tied to V_{SS}.

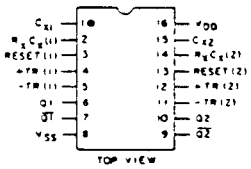
In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to −TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (−TR) is used.

The time period (T) for this multivibrator can be approximated by: $T_X = \frac{1}{2} R_X C_X$ for $C_X \geq 0.01\ \mu F$.

Values of T vary from unit to unit and as a function of voltage, temperature, and $R_X C_X$.

The minimum value of external resistance, R_X, is 5 kΩ. The maximum value of external capacitance, C_X, is 100 μF.

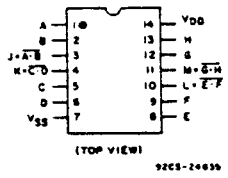




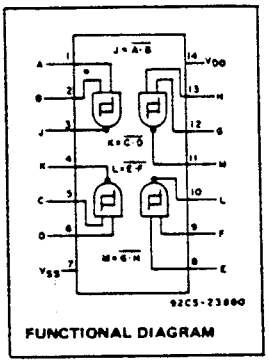
TERMINALS 1, 8, 15 ARE ELECTRICALLY CONNECTED INTERNALLY

TERMINAL ASSIGNMENT

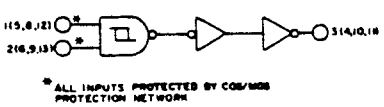
CD4093B TYPES
COS/MOS
QUAD 2-INPUT NAND
SCHMITT TRIGGERS

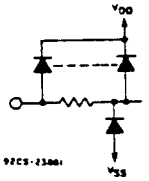


TERMINAL ASSIGNMENT



FUNCTIONAL DIAGRAM





High-Voltage Types (20 Volt Rating)

The RCA-CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H).

The CD4093B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

CD4514B
COS/MOS 4-BIT LATCH/4-TO-16 LINE DECODERS

The RCA-CD45148 and -CD45158 consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD45148) or 1(CD45158) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

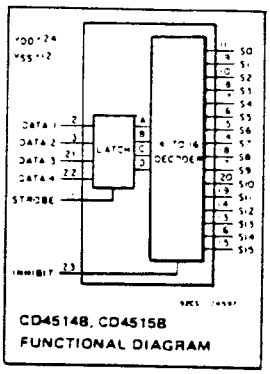
These devices are similar to industry types MC14514 and MC14515.

The CD4514B and CD4515B types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in line plastic packages (E suffix), and in chip form (H suffix).

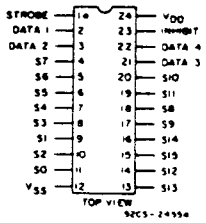
DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DECODER INPUTS				SELECTED OUTPUT CD45148 = Logic 1 (High) CD45158 = Logic 0 (Low)
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD45148 All Outputs = 1, CD45158

X = Don't Care Logic 1 = high Logic 0 = low



CD45148, CD45158
FUNCTIONAL DIAGRAM



CD4514B

TERMINAL ASSIGNMENT

CD4538B TYPES
COS/MOS DUAL PRECISION MONOSTABLE MULTIVIBRATOR

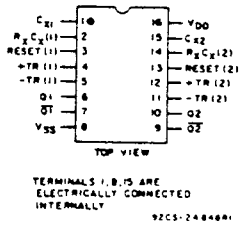
High-Voltage Types (20-Volt Rating)

The RCA-CD4538B dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

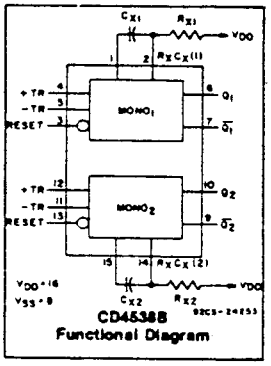
An external resistor (R_X) and an external capacitor (C_X) control the timing and accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X. Precision control of output pulse widths is achieved through linear CMOS techniques.

Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused −TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4538B is not used, its inputs must be tied to either V_{DD} or V_{SS}.

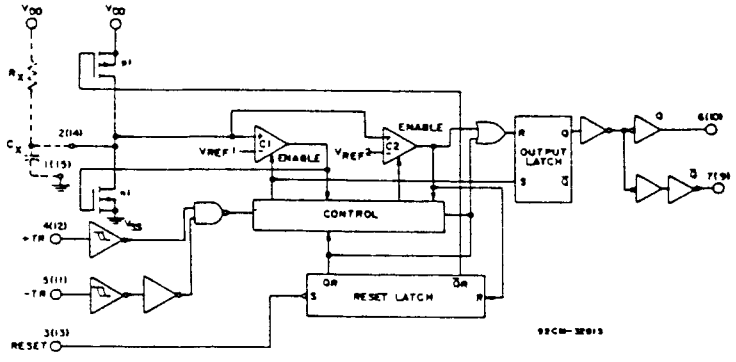
In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse.



TERMINAL ASSIGNMENT



CD4538B
Functional Diagram

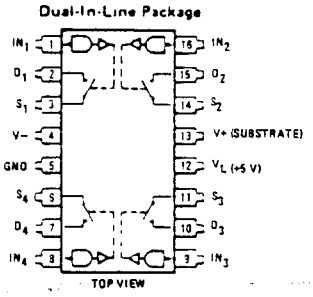


Logic diagram (½ of device shown).

DG211
QUAD MONOLITHIC SPST CMOS ANALOG SWITCH

The DG211 is a 4-channel single pole single throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0 V to 0.8 V) the switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make. Logic inputs can directly connect to op-amp output swings.

PIN CONFIGURATION



LOGIC	SWITCH
0	ON
1	OFF

SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

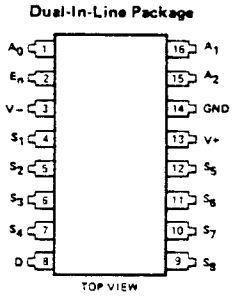
DG508
8-CHANNEL/4-CHANNEL DIFFERENTIAL CMOS ANALOG MULTIPLEXER

DESCRIPTION

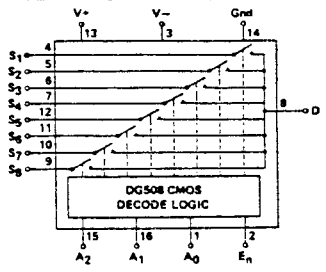
The DG508 is a single-pole 8-position (plus OFF) electronic switch array [DG509 double-pole, 4-position (plus OFF)], which employs 8 pairs of complementary MOS (CMOS) field-effect transistors designed to function as analog switches. In the ON condition each switch will conduct current in either direction, and in the OFF position each switch will block voltages up to 30 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word input plus an Enable-Inhibit input. The truth table below shows the binary word required to select any one of the 8 switch positions, provided a positive logic "1" is present at the Enable Input. With logic "0" at the Enable input all switches will be OFF. The logic decoder and the Enable inputs will recognize as logic "0" any voltage between 0 and 0.8 V, and any voltage between 2.4 and 15 V as logic "1" inputs. The inputs can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Delays are designed into logic decode and driver circuits to insure that switch action is break-before-make.

DECODE TRUTH TABLE

	A_2	A_1	A_0	E_N	ON SWITCH	DG509
DG508	X	X	X	0	NONE	
	0	0	0	1	1	
	0	0	1	1	2	
	0	1	0	1	3	
	0	1	1	1	4	
	1	0	0	1	5	Logic "1" = $V_{AH} \geq 2.4$ V
	1	0	1	1	6	
	1	1	0	1	7	Logic "0" = $V_{AL} \leq 0.8$ V
	1	1	1	1	8	



FUNCTIONAL DIAGRAM DG508

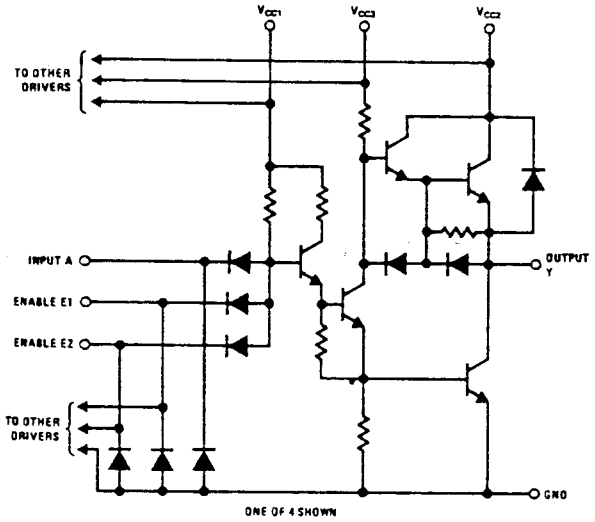


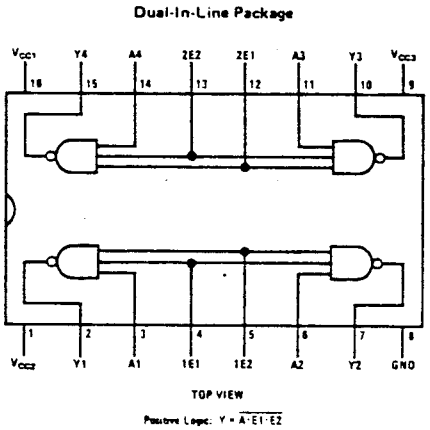
DS75365
QUAD TTL-TO-MOS DRIVER

General Description

The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

Schematic and Connection Diagrams





LF347
WIDE BANDWIDTH QUAD JFET INPUT OPERATIONAL AMPLIFIER

General Description

The LF347 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF347 is pin compatible with the standard LM348. This feature allows designers to immediately upgrade the overall performance of existing LM348 and LM324 designs.

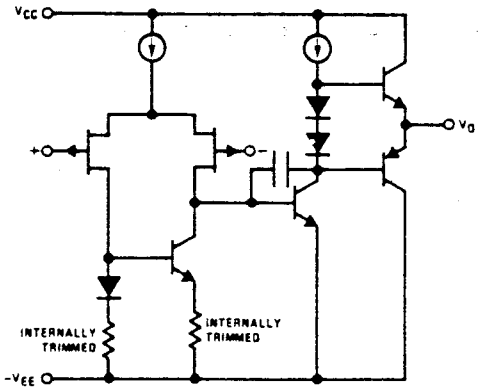
The LF347 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

■ Internally trimmed offset voltage	2 mV
■ Low input bias current	50 pA
■ Low input noise voltage	16 nV/$\sqrt{Hz}$
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	7.2 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

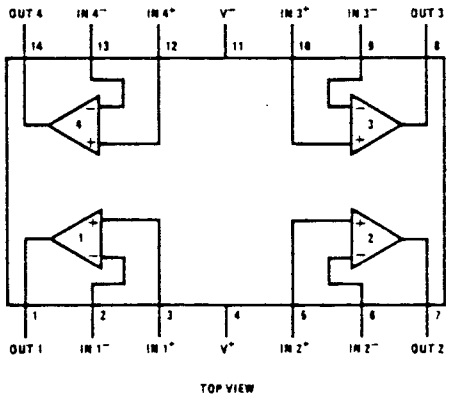
Simplified Schematic

1/4 Quad



Connection Diagram

Dual-In-Line Package



TOP VIEW

LM211
VOLTAGE COMPARATOR

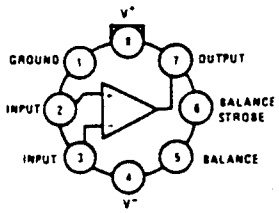
The LM111 and LM211 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA. Outstanding characteristics include:

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Both the inputs and the outputs of the LM111 or the LM211 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

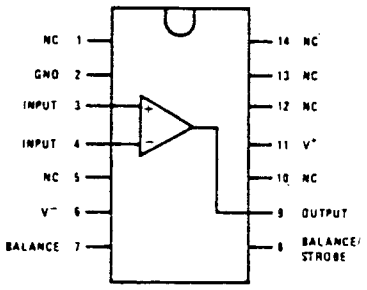
The LM211 is identical to the LM111, except that its performance is specified over a −25°C to 85°C temperature range instead of −55°C to 125°C.

Metal Can Package



NOTE: Pin 4 connected to case.
TOP VIEW

Dual-In-Line Package



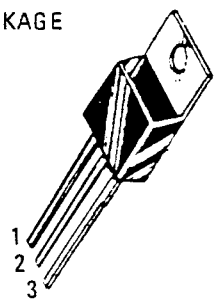
Note: Pin 6 connected to bottom of package.
TOP VIEW

LM317T
THREE-TERMINAL
ADJUSTABLE POSITIVE
VOLTAGE REGULATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

The 317 is an adjustable three-terminal positive voltage regulator capable of supplying 1.5 A over an output range of 1.2 V to 37 V. Internal current limiting, thermal shutdown, and safe area compensation make the regulator almost blow-out proof.

T SUFFIX
PLASTIC PACKAGE
CASE 221A
(TO-220)



PIN 1 ADJUST
PIN 2 V_{OUT}
PIN 3 V_{IN}

HEATSINK SURFACE CONNECTED
TO PIN 2

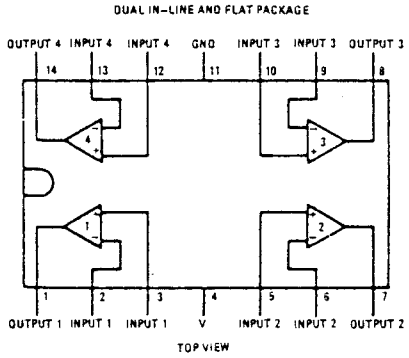
LM324
LOW POWER QUAD OPERATIONAL AMPLIFIERS

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Connection Diagram

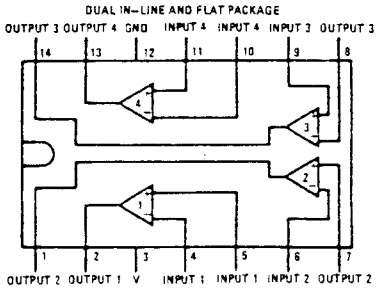


LM339
LOWER POWER LOW OFFSET VOLTAGE QUAD COMPARATORS

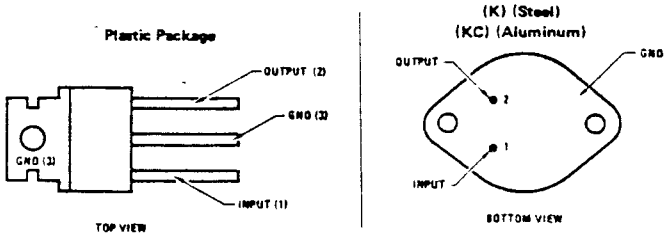
General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

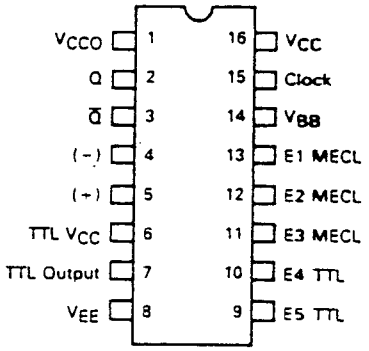


LM340 SERIES
VOLTAGE REGULATORS

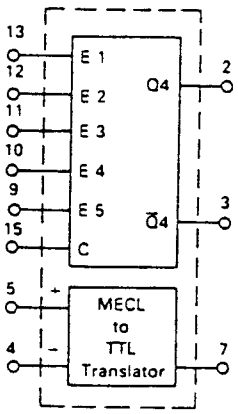


MC12013
TWO-MODULUS PRESCALER

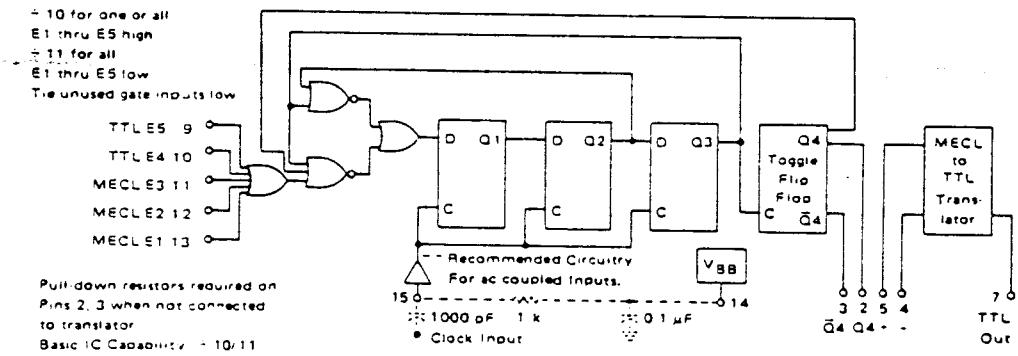
These devices are two-modulus prescalers which will divide by 5 and 6, 8 and 9, and 10 and 11, respectively. A MECL-to-TTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.



LOGIC DIAGRAM



V_{CCO} = pin 1
V_{CC} = pin 16
V_{EE} = pin 8



MC145156
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

The MC145156 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

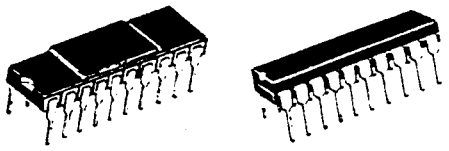
The MC145156 is programmed by a clocked, serial input, 19-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit programmable ÷A counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145156 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145156.

- General Purpose Applications —
  CATV — TV Tuning
  AM/FM Radios — Scanning Receivers
  Two-Way Radios — Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values — 8, 64, 128, 256, 640, 1000, 1024, 2048
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Dual Modulus/Serial Programming
- ÷N Range = 3 to 1023
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options —
  Single Ended (Three-State)
  Double Ended

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

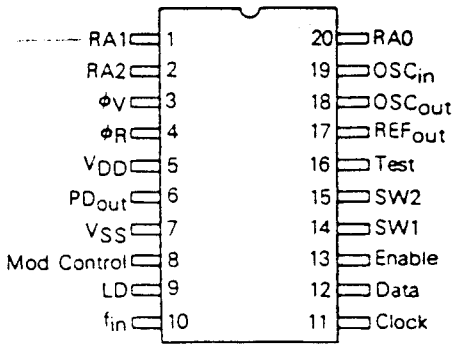
SERIAL INPUT PLL
FREQUENCY SYNTHESIZER

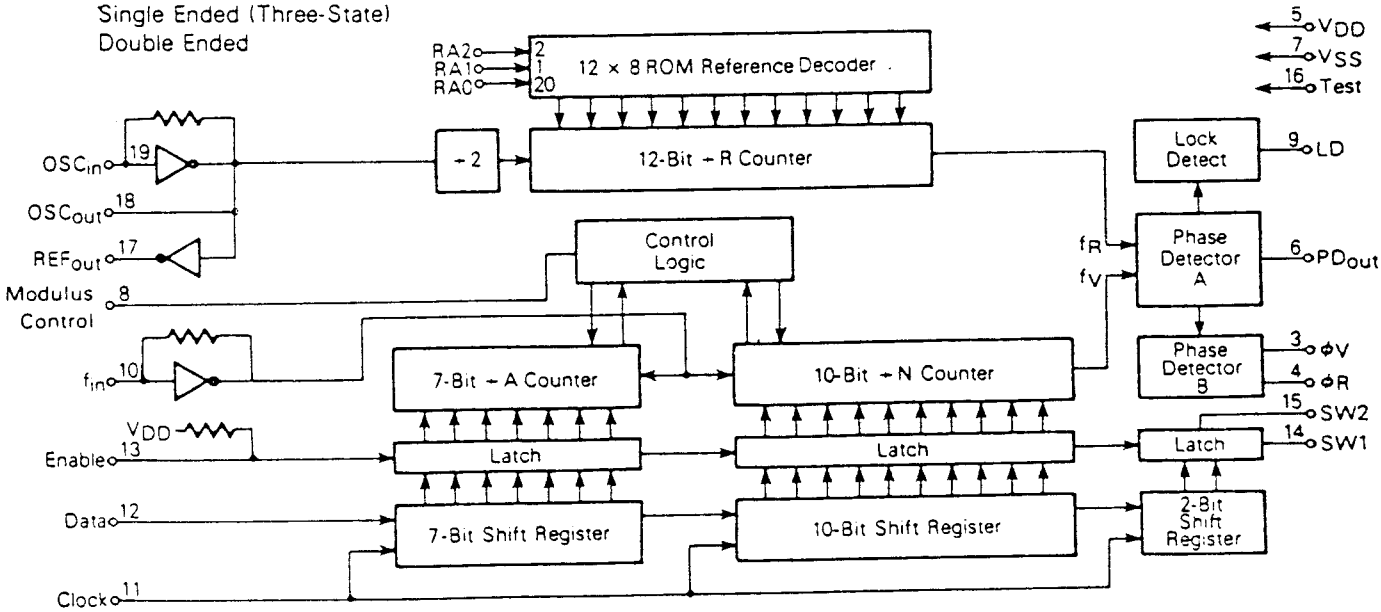


L SUFFIX
CERAMIC PACKAGE
CASE 729-01

P SUFFIX
PLASTIC PACKAGE
CASE 738-02

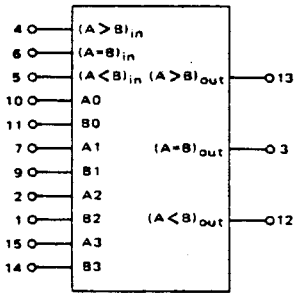
PIN ASSIGNMENT





MC14585B
CMOS MSI
(LOW POWER COMPLEMENTARY MOS)
4-BIT MAGNITUDE COMPARATOR

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

4-BIT MAGNITUDE COMPARATOR

The MC14585B 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A<B, A=B, and A>B), and three outputs (A<B, A=B, and A>B). This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A<B), and (A=B) to the corresponding inputs of the next significant comparator (input A>B is connected to a high). Inputs (A<B), (A=B), and (A>B) on the least significant (first) comparator are connected to a low, a high, and a high, respectively.

Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

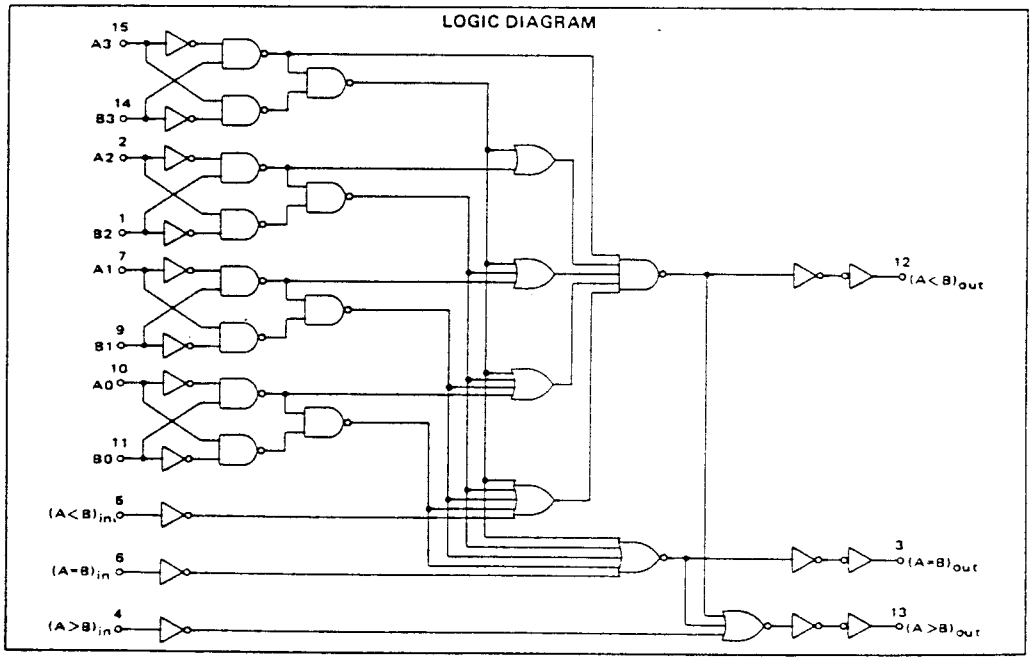
- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout > 50
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Expandable
- Applicable to Binary or 8421-BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	1	0	0	1
A3=B3	A2>B2	X	X	X	X	1	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	1	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	1	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

X = Don't Care

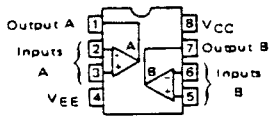
LOGIC DIAGRAM



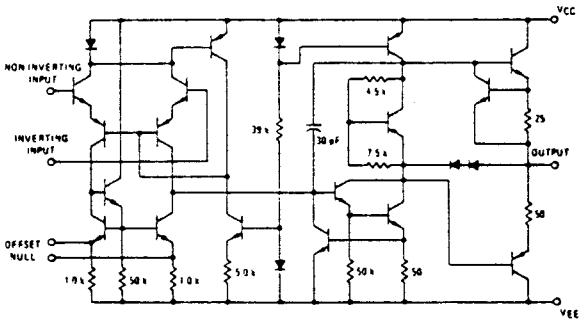
MC1458
DUAL OPERATIONAL AMPLIFIER
SILICON MONOLITHIC INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1458,MC1458C,MC1458N)

U SUFFIX
CERAMIC PACKAGE
CASE 693



EQUIVALENT CIRCUIT SCHEMATIC



MC1496
BALANCED MODULATOR – DEMODULATOR
SILICON MONOLITHIC INTEGRATED CIRCUIT

VOLTAGE GAIN AND OUTPUT FREQUENCIES

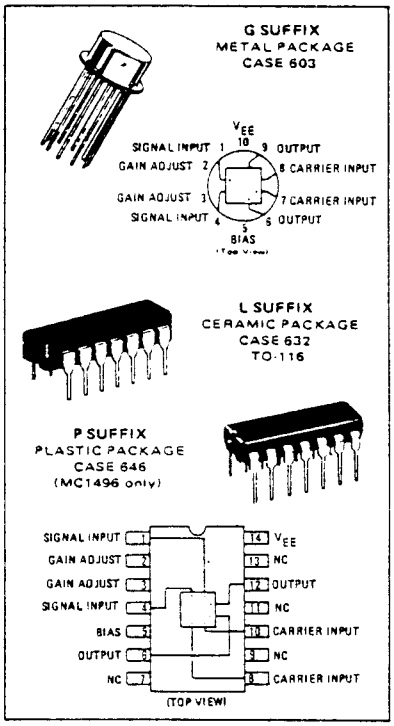
Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637\, R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

NOTES:
1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at +25°C:

$$r_e \approx \frac{26\ mV}{I_5\ (mA)}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26\ mV \text{ at room temperature}$$



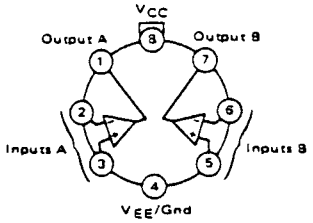
G SUFFIX
METAL PACKAGE
CASE 603

L SUFFIX
CERAMIC PACKAGE
CASE 632
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 646
(MC1496 only)

MC3358
DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS
SILICON MONOLITHIC INTEGRATED CIRCUIT

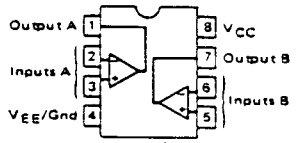
G SUFFIX
METAL PACKAGE
CASE 601



(TOP VIEW)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC3458, MC3358 only)

U SUFFIX
CERAMIC PACKAGE
CASE 693



(TOP VIEW)

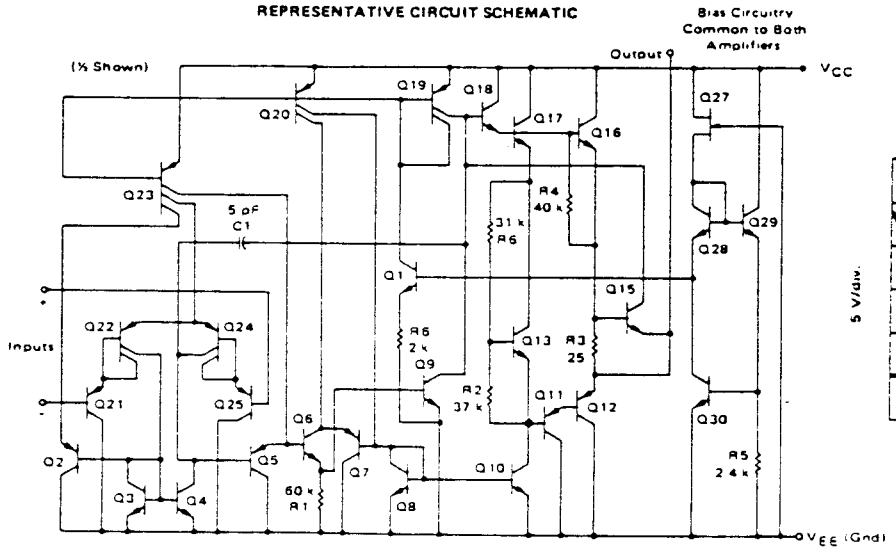
CIRCUIT DESCRIPTION

The MC3358 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

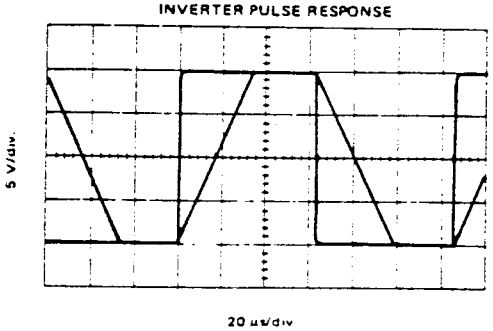
The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

REPRESENTATIVE CIRCUIT SCHEMATIC



INVERTER PULSE RESPONSE



MC7800C, AC SERIES
THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

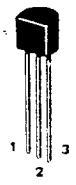
These devices offer a substantial performance advantage over the traditional zener diode-resistor combination. Output impedance is greatly reduced and quiescent current is substantially reduced.

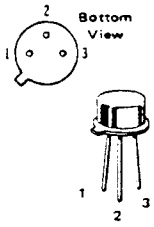
- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

P SUFFIX
CASE 29
TO-92

Pin 1. Output
2. Ground
3. Input



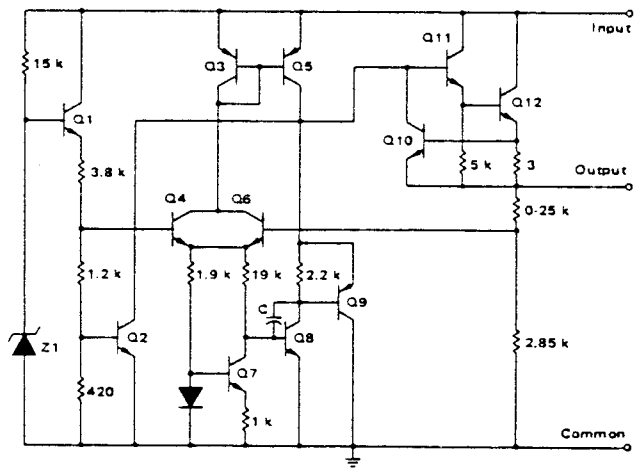


G SUFFIX
CASE 79
TO-39

Pin 1. Input
2. Output
3. Ground

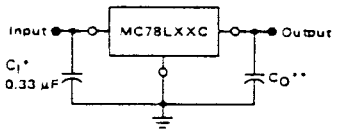
(Case connected to pin 3)

REPRESENTATIVE CIRCUIT SCHEMATIC



Device No. ±10%	Device No. ±5%	Nominal Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

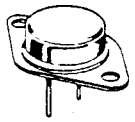
MC7900C SERIES
THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

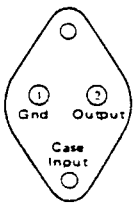
Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation – making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A and Case 1 (TO-220 and Hermetic TO-3)

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS



K SUFFIX
METAL PACKAGE
CASE 1
(TO-3 TYPE)

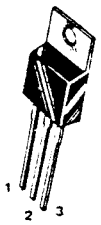


(bottom view)

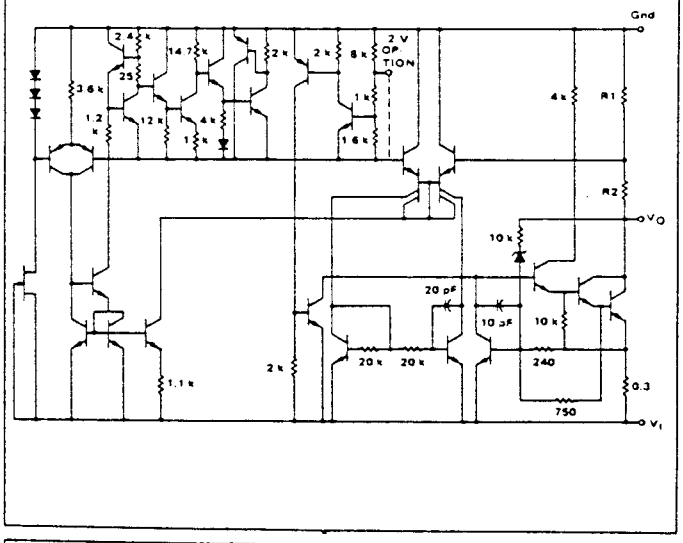
T SUFFIX
PLASTIC PACKAGE
CASE 221A

Pin 1. Ground
2. Input
3. Output

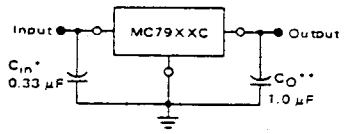
(Heatsink surface connected to Pin2)



SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

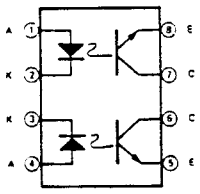
DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7902C - 2.0 Volts	MC7906C - 6.0 Volts	MC7915C - 15 Volts
MC7905C - 5.0 Volts	MC7908C - 8.0 Volts	MC7918C - 18 Volts
MC7905.2C - 5.2 Volts	MC7912C - 12 Volts	MC7924C - 24 Volts

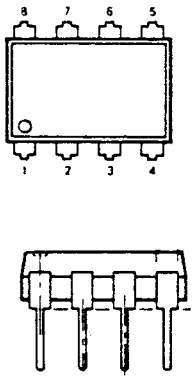
MCT6
DUAL PHOTOTRANSISTOR OPTOISOLATORS

DESCRIPTION

The MCT6 and MCT66 optoisolators have two channels for high density applications. For four channel applications, two-packages fit into a standard 16-pin DIP socket. Each channel is an NPN silicon planar phototransistor opticaily coupled to a gallium arsenide diode.



PACKAGE DIMENSIONS

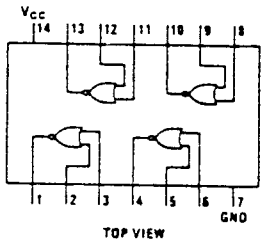


MM54C02/MM74C02
QUAD 2-INPUT NOR GATE

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

MM54C02/MM74C02

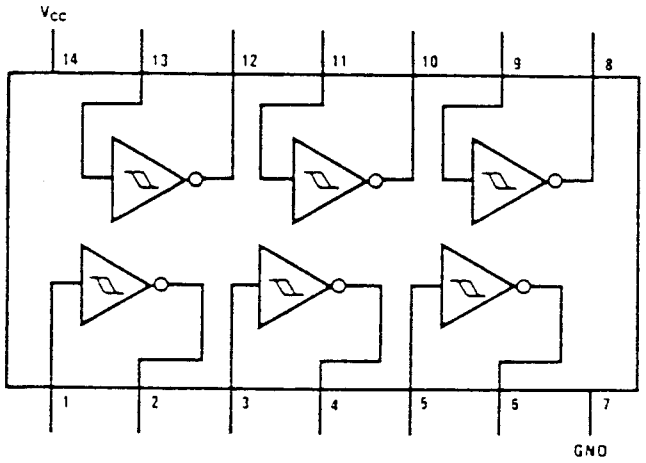


TOP VIEW

MM74C14
HEX SCHMITT TRIGGER

The MM54C14/MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ. 0.0005 V/°C at $V_{CC} = 10$ V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2 V_{CC}$ is guaranteed.

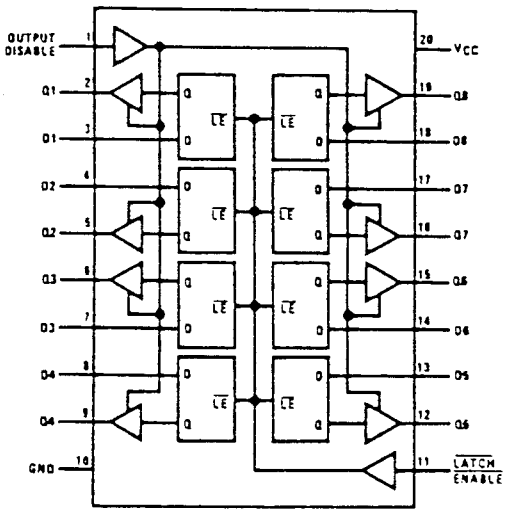
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.



TOP VIEW

MM74C373
OCTAL LATCH

Connection Diagram



TOP VIEW

General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads, such as one might find when driving a bus, and to have a fan-out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When $\overline{\text{LATCH ENABLE}}$ is high, the Q outputs will follow the D inputs. When $\overline{\text{LATCH ENABLE}}$ goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until $\overline{\text{LATCH ENABLE}}$ returns high again.

NE-SA594
VACUUM FLUORESCENT DISPLAY DRIVER

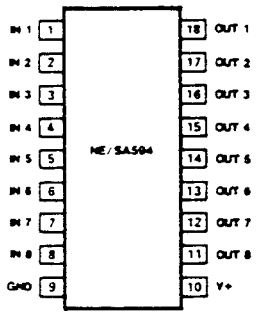
DESCRIPTION

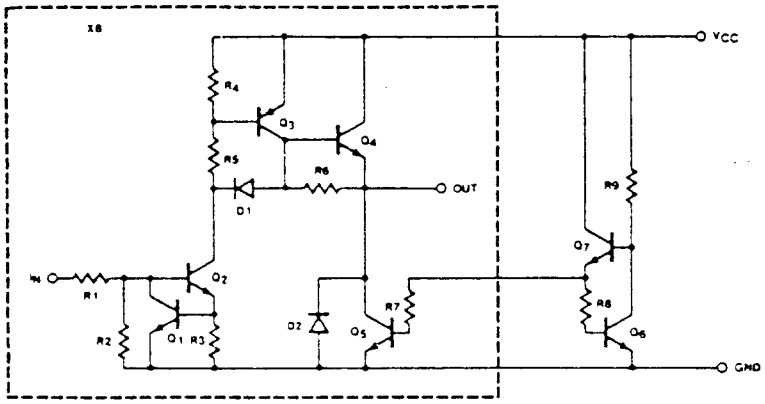
The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

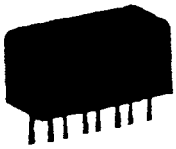
N, F PACKAGE





SAY-1
SUPER HIGH LEVEL (+23 DBM LO) DOUBLE-BALANCED MIXERS

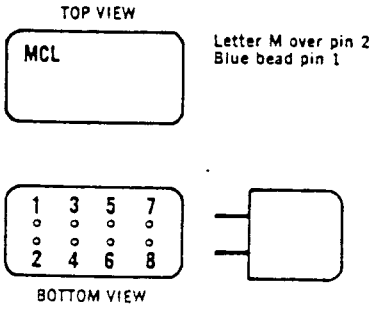
SAY SERIES

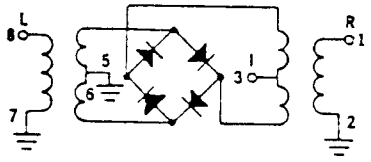


DESCRIPTION — High-level RF input capability coupled with ultra-low distortion, octaves of bandwidth, and reasonably good conversion loss make the SAY series obvious choices for applications in ECM receivers, spectrum analyzers, and field radios.

These mixers offer two-tone, third order intermodulation products that are typically 70 dB below the desired IF level (each tone is set at 0 dBm and the LO drive is at +23 dBm). The 1 dB conversion compression point occurs at an RF level of +20 dBm.

CONNECTIONS

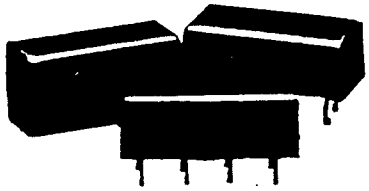




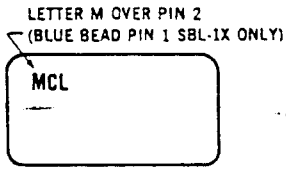
Model No.	-1 -2 -11
LO	8
RF	1
IF	3
Ground	2,5,6,7
Case Ground	2,5,6,7

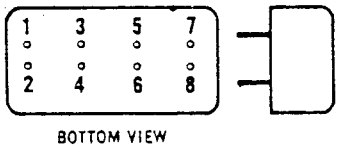
SBL-1
STANDARD LEVEL (+7 DBM LO)
DOUBLE-BALANCED MIXERS

SBL SERIES

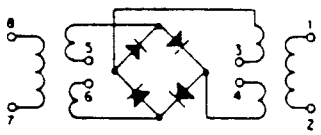


CONNECTIONS





BOTTOM VIEW



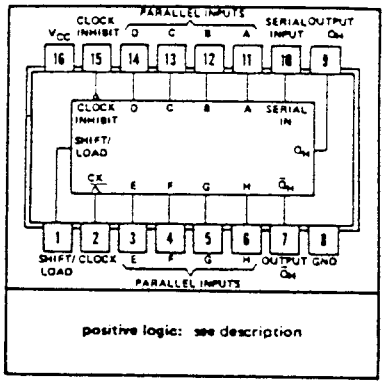
PIN LAYOUT

	Fig. 1	Fig. 2
Model No.	-1	-1X
LO	8	8
RF	1	3,4
IF	3,4	1
Ground	2,5,6,7	2,5,6,7
Case Ground	—	2,5,6,7

NOTE: PINS 3 AND 4 MUST BE CONNECTED TOGETHER

SN74165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

(TOP VIEW)



The '165 and 'LS165 are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

SN74L90
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTER

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

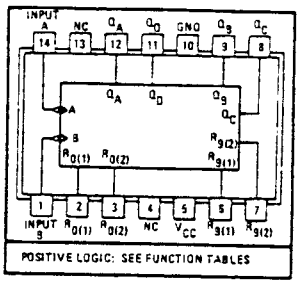
To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

'90A, 'L90, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

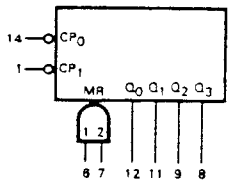


'90A, 'L90, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

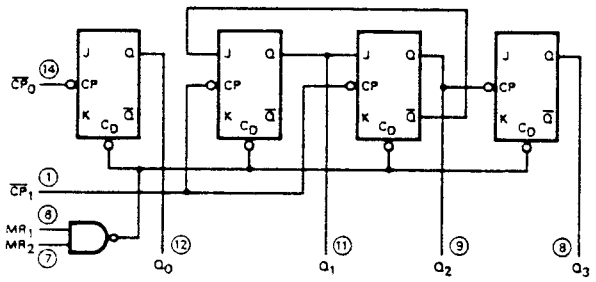
SN54LS/74LS92
DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER
LOW POWER SCHOTTKY



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 2, 3, 4, 13

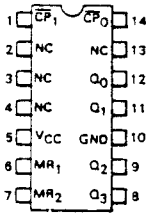
LOGIC DIAGRAM

LS92



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \bullet MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \bullet MS_2$) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

A. Modulo 12, Divide-By-Twelve Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

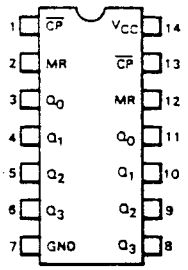
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

Note: Output Q_0 connected to input $\overline{CP}_1$

SN54LS/74LS393
DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER
LOW POWER SCHOTTKY

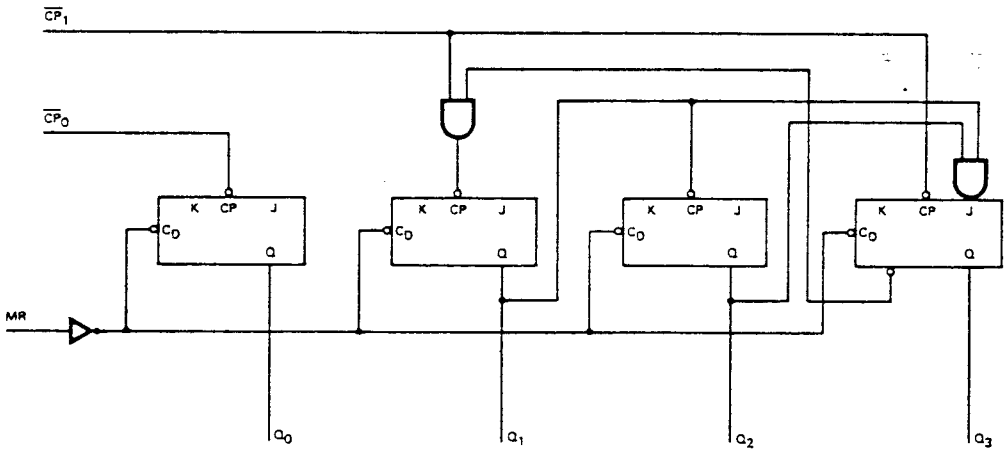
SN54LS/74LS393



J Suffix — Case 632-06 (Ceramic)
N Suffix — Case 646-05 (Plastic)

FUNCTIONAL DESCRIPTION—Each half of the SN54LS/74LS393 Operates in the Modulo 16 binary sequence, as indicated in the ÷16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

SN54LS/74LS393 LOGIC DIAGRAM (one half shown)



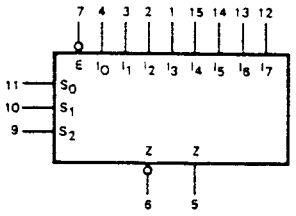
SN54LS/74LS393
TRUTH TABLE

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

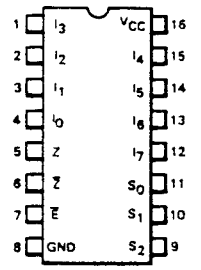
SN54LS151/SN74LS151
8-INPUT MULTIPLEXER
LOW POWER SCHOTTKY

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



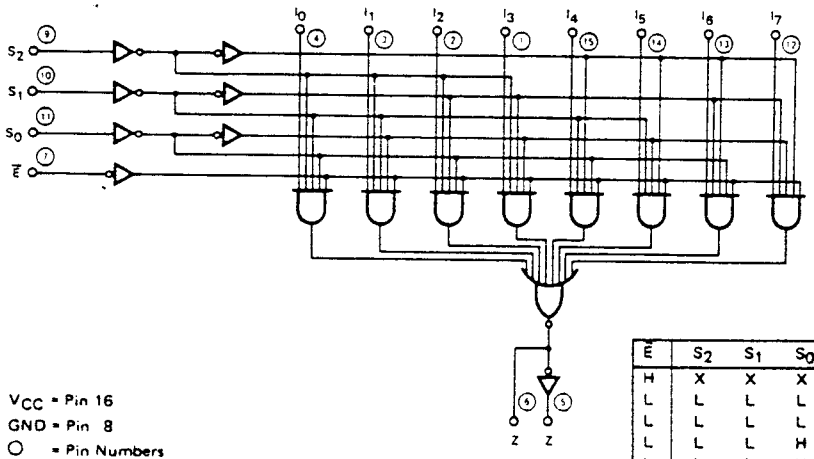
J Suffix — Case 620-06
(Ceramic)
N Suffix — Case 648-05
(Plastic)

FUNCTIONAL DESCRIPTION – The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The LS151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the LS151 can provide any logic function of four variables and its negation.

LOGIC DIAGRAM



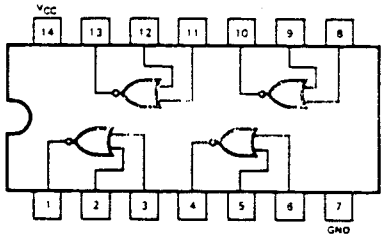
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

TRUTH TABLE

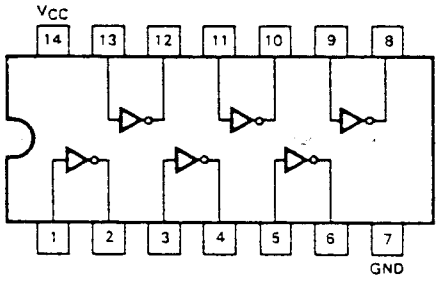
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SN54LS02/SN74LS02
QUAD 2-INPUT NOR GATE
LOW POWER SCHOTTKY

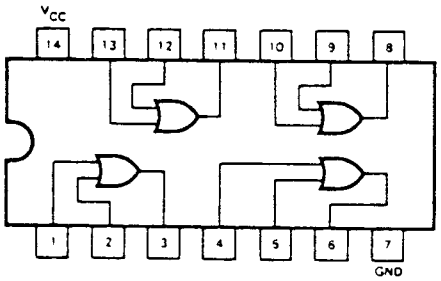


SN54LS04/SN74LS04
HEX INVERTER
LOW POWER SCHOTTKY



J Suffix — Case 632-06 (Ceramic)
N Suffix — Case 646-05 (Plastic)

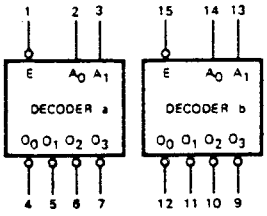
SN54LS32/SN74LS32
QUAD 2-INPUT OR GATE
LOW POWER SCHOTTKY



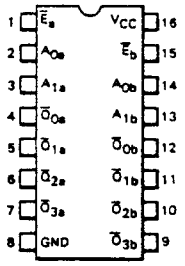
J Suffix — Case 632-06 (Ceramic)
N Suffix — Case 646-05 (Plastic)

SN54LS139/SN74LS139
DUAL 1-OF-4 DECODER/DEMULTIPLEXER
LOW POWER SCHOTTKY

LOGIC SYMBOL



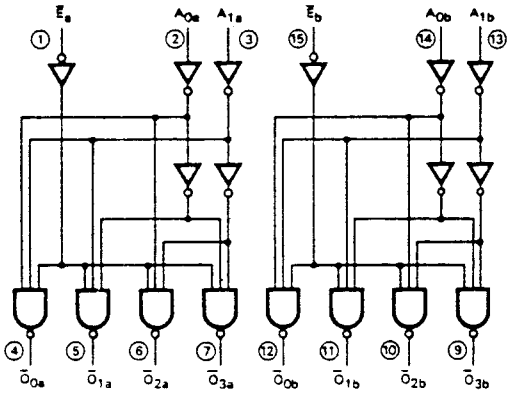
CONNECTION DIAGRAM
DIP (TOP VIEW)



J Suffix — Case 620-06
(Ceramic)
N Suffix — Case 648-05
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



VCC = Pin 16
GND = Pin 8
○ = Pin Numbers

VCC = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The LS139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

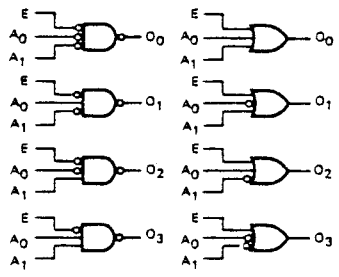
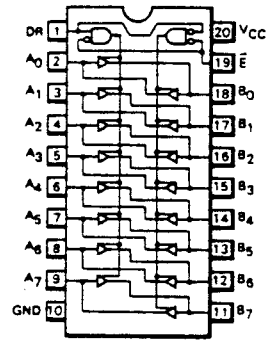


Fig. a

SN54LS245/SN74LS245
OCTAL BUS TRANSCEIVER
LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input ($\overline{E}$) can be used to isolate the buses.

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)



J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-01 (Plastic)

TRUTH TABLE

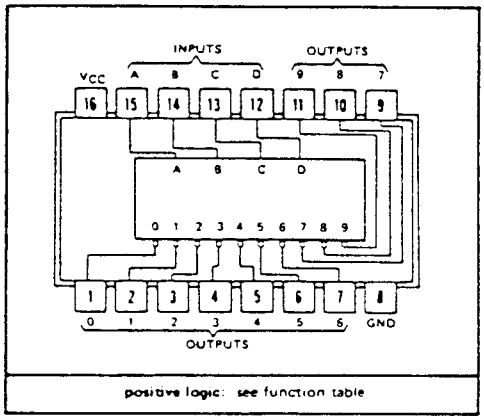
INPUTS		OUTPUT
$\overline{E}$	DR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SN74LS42
4-LINE-TO-10-LINE DECODERS (1-OF-10)

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A, 'L42, and 'LS42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 excess-3-gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. D-c noise margins are typically one volt.



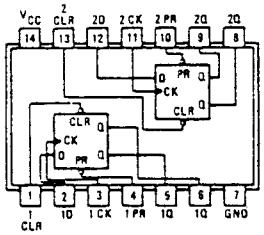
positive logic: see function table

ALL TYPES									
DECIMAL OUTPUT									
0	1	2	3	4	5	6	7	8	9
L	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H
H	H	H	H	L	H	H	H	H	H
H	H	H	H	H	L	H	H	H	H
H	H	H	H	H	H	L	H	H	H
H	H	H	H	H	H	H	L	H	H
H	H	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	L
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H

SN74LS74N
DUAL D-TYPE POSITIVE EDGE TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

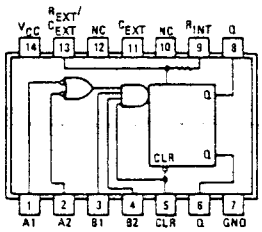


SN74LS122
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

NOTES:
1. AN EXTERNAL TIMING CAPACITOR MAY BE CONNECTED BETWEEN C_{EXT} AND R_{EXT}/C_{EXT} (POSITIVE).
2. FOR ACCURATE REPEATABLE PULSE WIDTHS, CONNECT AN EXTERNAL RESISTOR BETWEEN R_{EXT}/C_{EXT} AND V_{CC} WITH R_{INT} OPEN-CIRCUITED.

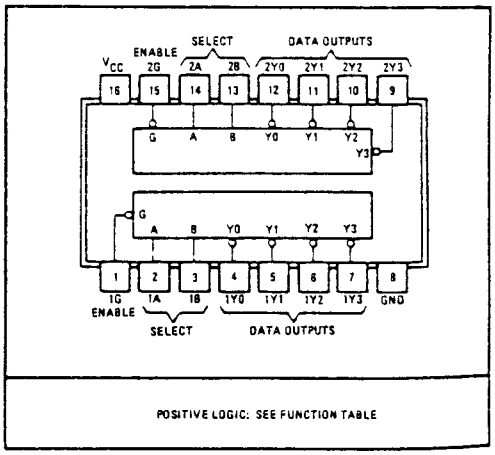


SN54122 (J, W) **SN74122 (J, N)**
SN54L122 (J, T) **SN74L122 (J, N)**
SN54LS122 (J, W) **SN74LS122 (J, N)**
'122 . . . R_{int} = 10 kΩ NOM
'L122 . . . R_{int} = 20 kΩ NOM
'LS122 . . . R_{int} = 10 kΩ NOM

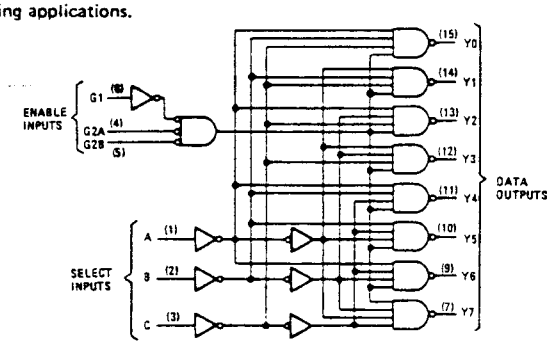
SN74LS138
DECODER/DEMULTIPLEXER

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.



'LS138, 'S138



'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2 = G2A + G2B
H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

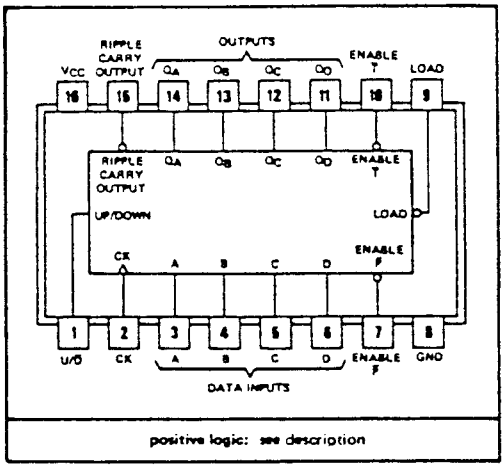
SN74LS168A
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

Programmable Look-Ahead Up/Down
Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS168A, 'LS169A	35 MHz	35 MHz	100 mW
'S168, 'S169	70 MHz	55 MHz	500 mW

(TOP VIEW)



positive logic: see description

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS168A and 'S168 are decade counters and the 'LS169A and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS168A and 'LS169A are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond minimum hold time and reduced input currents I_{IH} and I_{IL}.

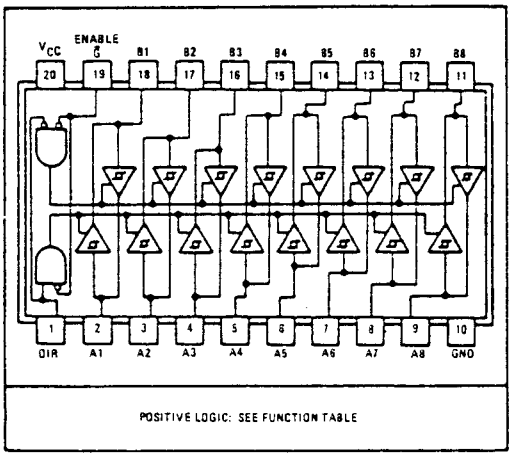
SN74LS245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The SN54LS245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS245 is characterized for operation from 0°C to 70°C.



FUNCTION TABLE

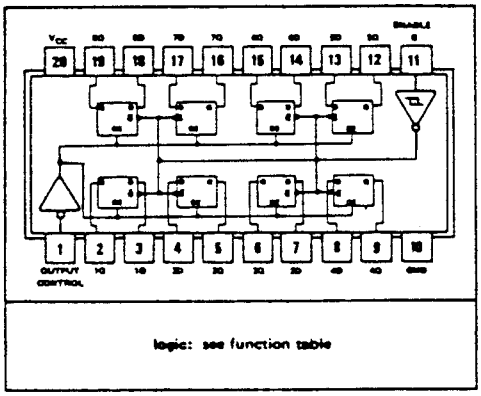
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

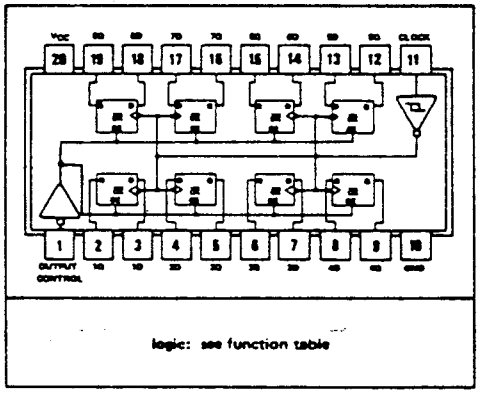
SN74LS373, SN74LS374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.



logic: see function table



logic: see function table

'LS373, 'S373
FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

'LS374, 'S374
FUNCTION TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

SP8629
150 MHz ÷ 100

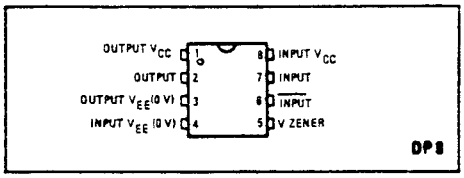
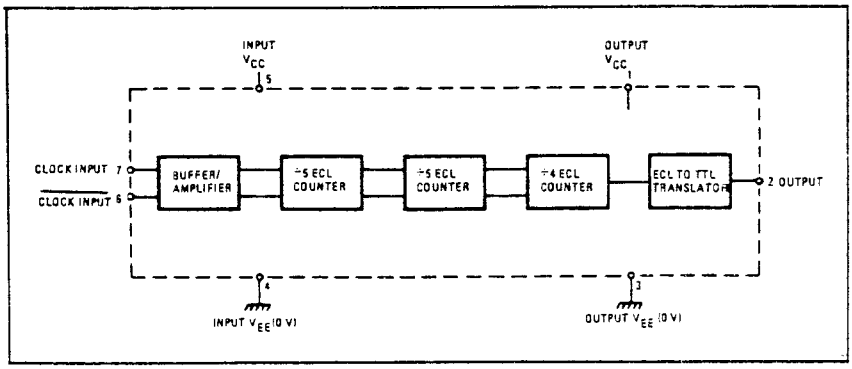
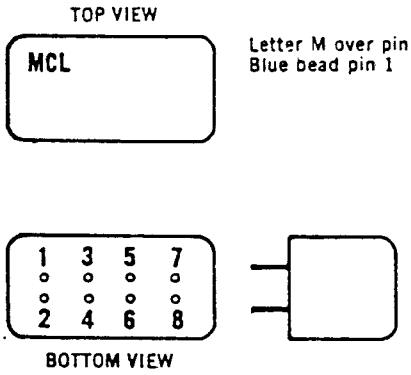


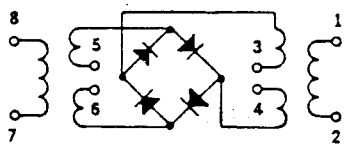
Fig.1 Pin connections - top view



SRA-1
STANDARD LEVEL (+7 DBM LO)
DOUBLE-BALANCED MIXERS

CONNECTIONS

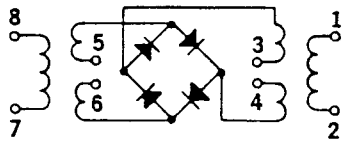


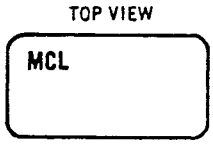


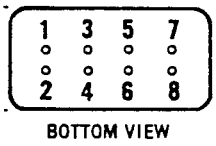
PIN LAYOUT

	Fig. 1
Model No.	-1 -1-1 -3 -1TX
LO	8
RF	1
IF	3,4
Ground	2,5,6,7
Case Ground	2

SRA-1H
0.5 MHz - 500 MHz
HIGH LEVEL (+17 dBm LO)
DOUBLE-BALANCED MIXERS







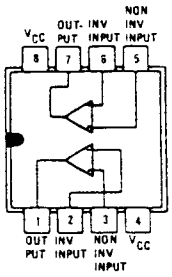
PIN LAYOUT

LO	8
RF	1
IF	3,4
Ground	2,5,6,7
Case Ground	2

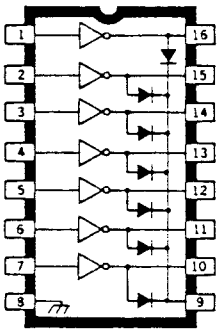
TL072
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

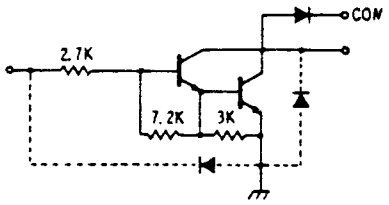
description

The JFET-input operational amplifiers of the TL071 series are designed as low-noise versions of the TL081 series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL071 series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET-inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

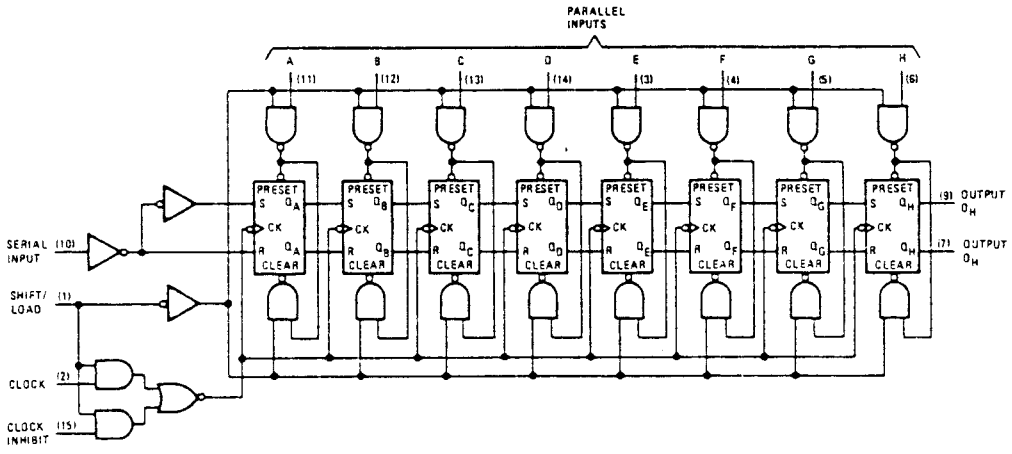


SERIES ULN-2000A
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS





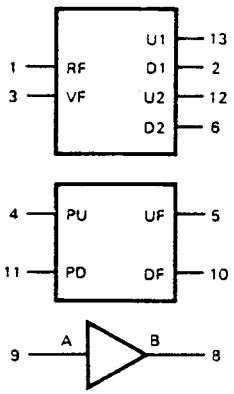
Series ULN-2003A
(each driver)



11C44
PHASE/FREQUENCY DETECTOR

GENERAL DESCRIPTION — The 11C44 contains a Phase/Frequency Detector, a Phase Detector, a Charge Pump, and an Amplifier. The Phase/Frequency Detector accepts TTL signals representing a Reference Frequency (RF) and a Variable Frequency (VF), compares the relative timing of their negative going transitions, and generates either an UP (U1) or a DOWN (D1) signal whose duration is equal to the RF-VF timing difference. When the RF and VF signals have the same frequency, the Phase Detector outputs U2 and D2 provide binary signals whose duty cycles are proportional to the phase angle between RF and VF. The Charge Pump can be driven from U1 and D1 or U2 and D2, and has three possible output states representing CHARGE, DISCHARGE, and HOLD instructions when applied to an integrator. The Amplifier is a Darlington transistor with grounded emitter and uncommitted collector and base. The 11C44 thus contains several of the functional elements used in phase-locked loop applications. It is pin compatible with the Motorola MC4044/4344, but has better discrimination capability for small phase differences.

LOGIC SYMBOL

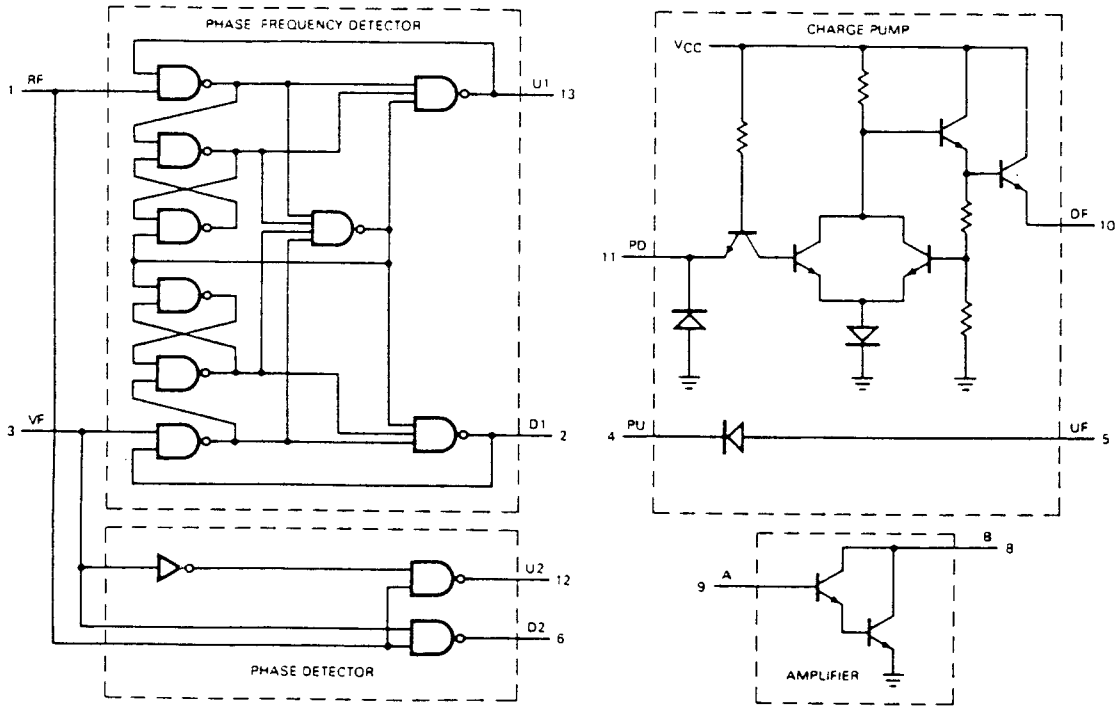


V_{CC} = Pin 14
GND = Pin 7

FUNCTIONS

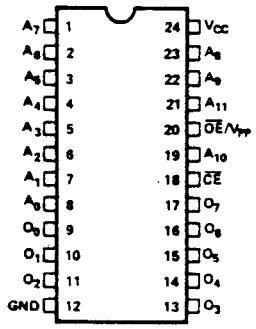
RF — Reference Frequency Input
VF — Variable Frequency Input
U1, D1 — Phase/Frequency Detector Outputs
U2, D2 — Phase Detector Outputs
PU, PD — Charge Pump Inputs
UF, DF — Charge Pump Outputs
A — Amplifier Input
B — Amplifier Output

LOGIC DIAGRAM AND SCHEMATIC



27C 32
32K (4K X 8) UV ERASABLE PROM

PIN CONFIGURATION



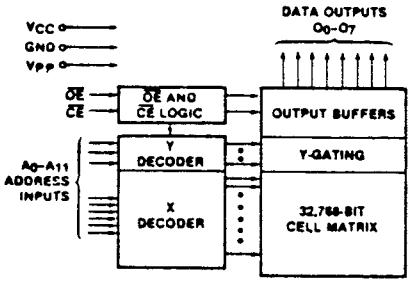
PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

MODE SELECTION

PINS / MODE	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	Vpp	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	Vpp	+5	High Z

BLOCK DIAGRAM



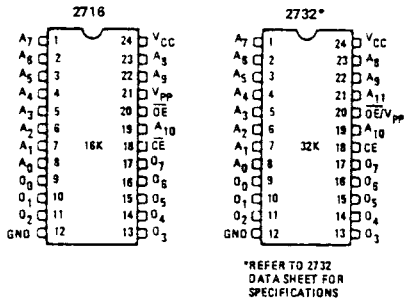
2716
16K (2K x 8) UV ERASABLE PROM

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



*REFER TO 2732 DATA SHEET FOR SPECIFICATIONS

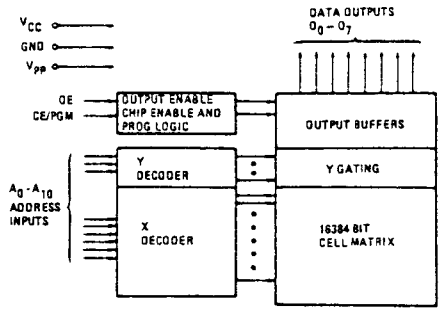
PIN NAMES

$A_0 - A_{10}$	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
$O_0 - O_7$	OUTPUTS

MODE SELECTION

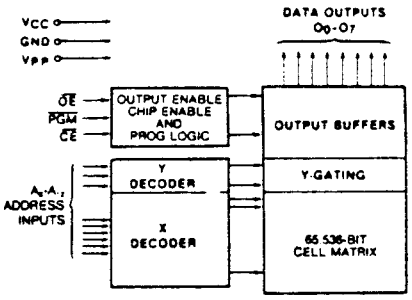
MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
READ	V_{IL}	V_{IL}	+5	+5	O_{OUT}
STANDBY	V_{IH}	DON'T CARE	+5	+5	HIGH Z
PROGRAM	PULSED V_{IL} TO V_{IH}	V_{IH}	+25	+5	O_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	+25	+5	O_{OUT}
PROGRAM INHIBIT	V_{IL}	V_{IH}	+25	+5	HIGH Z

BLOCK DIAGRAM



2764
(8K X 8) UV ERASABLE PROM

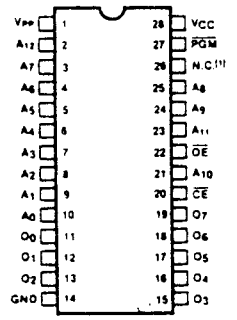
BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECT

2764
PIN CONFIGURATION



DEVICE OPERATION

The five modes of operation of the 2764 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

TABLE 1. MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	x	x	V_{CC}	V_{CC}	High Z
Program	V_{IL}	x	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	x	x	V_{PP}	V_{CC}	High Z

x can be either V_{IL} or V_{IH}

READ MODE

The 2764 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{\overline{OE}}$.

Standby Mode

The 2764 has a standby mode which reduces the active power current from 150mA to 50mA. The 2764 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connection. The two line control function allows for:

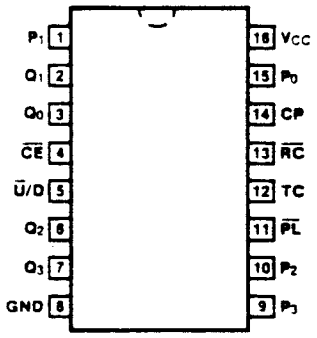
a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

54F/74F191
UP/DOWN BINARY COUNTER
(WITH PRESET AND RIPPLE CLOCK)

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
$P_0 - P_3$	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}/D$	Up/Down Count Control Input
$Q_0 - Q_3$	Flip-flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Count Output (Active HIGH)

Connection Diagram



Mode Select Table

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

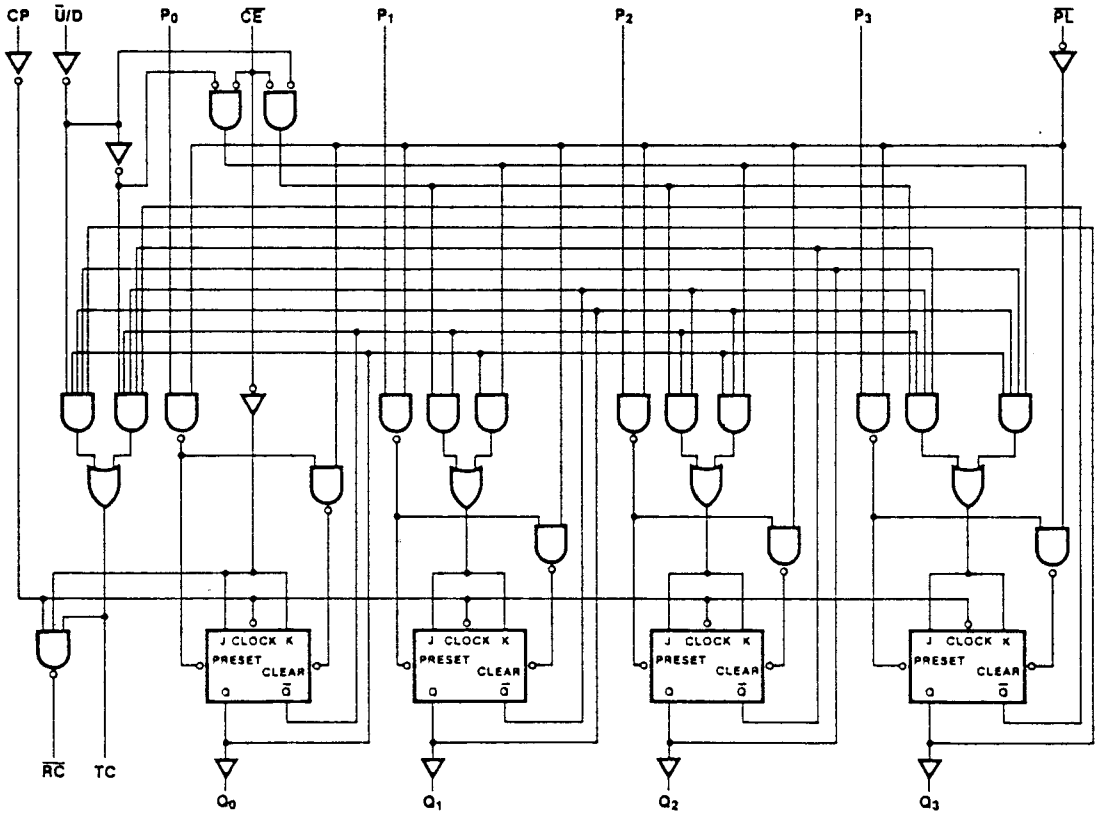
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

$\overline{RC}$ Truth Table

INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⎍	⎍
H	X	X	H
X	L	X	H

*TC is generated internally

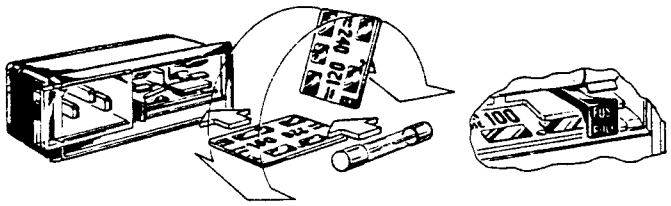
Logic Diagram

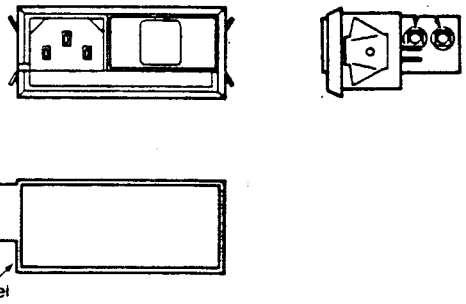


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

CORCOM
J SERIES
VOLTAGE SELECTING AND FUSED CONNECTOR
6J4

Voltage Selection

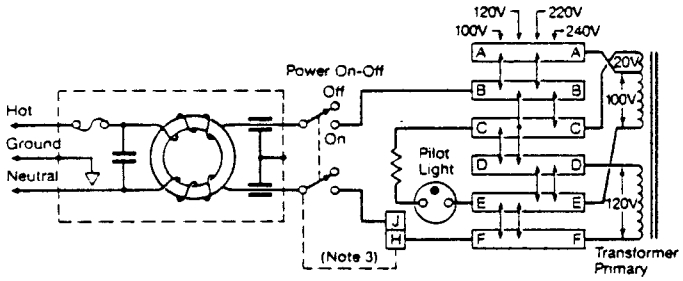




Open cover door and rotate fuse pull to left.

Select operating voltage by orienting PC Board to position desired voltage on top left side. Push board firmly into module slot.

Rotate fuse-pull back into normal position and re-insert fuse into holders, using caution to select correct fuse value.



Note 3: Jumper required if only SPST Power Switch is used.
Note 4: Jumpers required if no input filtering is used.

8035
SINGLE COMPONENT 8-BIT MICROCOMPUTER

*8048 Mask Programmable ROM
*8748 User Programmable/Erasable EPROM
*8035 External ROM or EPROM

- 8-Bit CPU, ROM, RAM, I/O in Single Package
- Interchangeable ROM and EPROM Versions
- Single 5V Supply
- 2.5 µsec and 5.0 µsec Cycle Versions All Instructions 1 or 2 Cycles.
- Over 90 Instructions: 70% Single Byte
- 1K x 8 ROM/EPROM
  64 x 8 RAM
  27 I/O Lines
- Interval Timer/Event Counter
- Easily Expandable Memory and I/O
- Compatible with 8000 Series Peripherals
- Single Level Interrupt

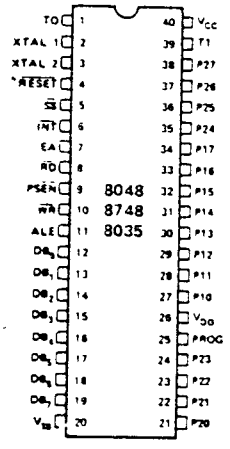
The Intel® 8048/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and 8000 series peripherals. The 8035 is the equivalent of an 8048 without program memory.

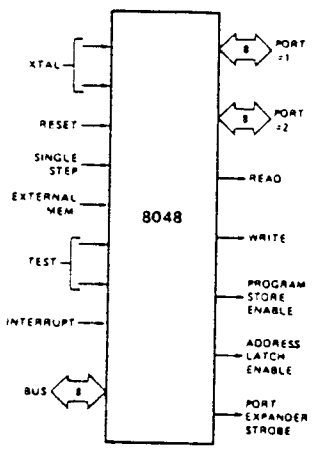
To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible versions of this single component microcomputer exist: the 8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems, the 8048 with factory-programmed mask ROM program memory for low-cost high volume production, and the 8035 without program memory for use with external program memories.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

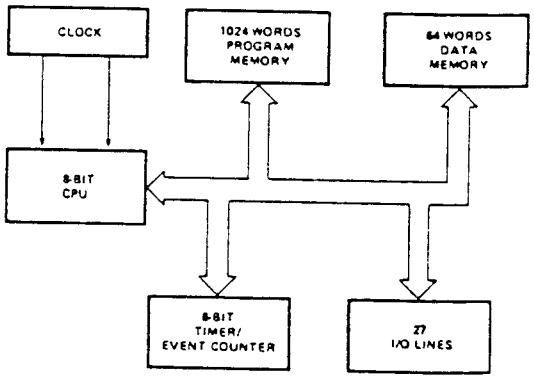
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



8035 (Cont.)

PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 ROM version.
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Program pulse (+25V) input pin during 8748 programming.
		Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243
DB_0-DB_7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

Designation	Pin #	Function
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.
		Used as a Read Strobe to External Data Memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low)
$\overline{WR}$	10	Output strobe during a BUS write. (Active low)(Non TTL V_{IH})
		Used as write strobe to External Data Memory.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Not TTL Compatible)
XTAL2	3	Other side of crystal input.

8085A/8085A-2
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSORS

FUNCTIONAL DESCRIPTION

The 8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz (8085A) or 5 MHz (8085A-2), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The cpu (8085A), a RAM/IO (8156), and a ROM or EPROM/IO chip (8355 or 8755A).

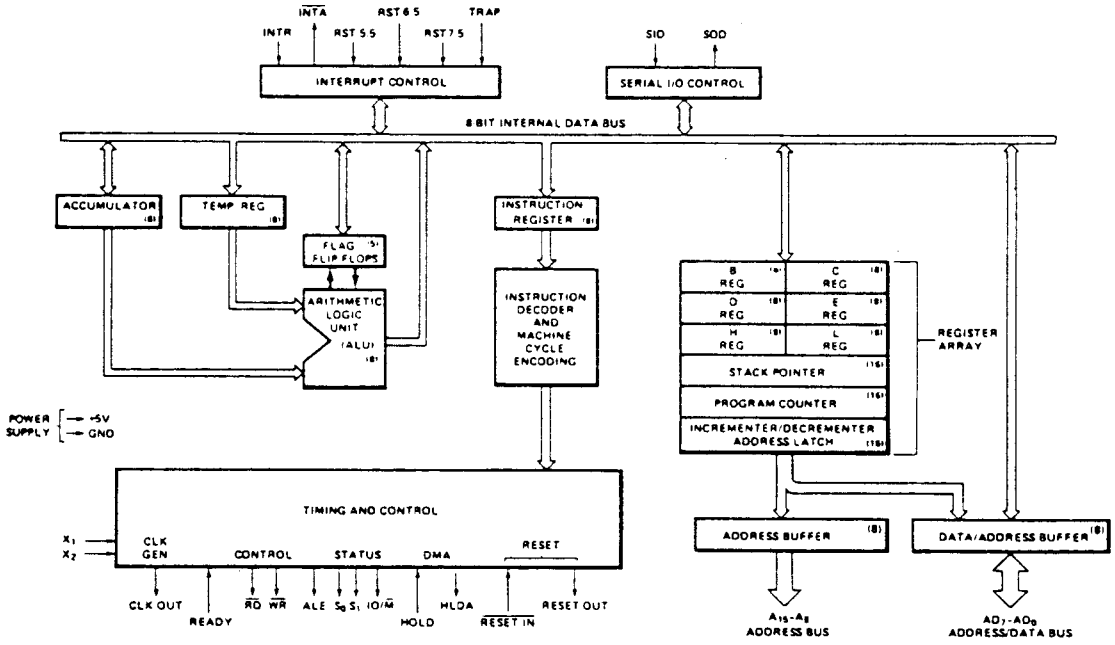
The 8085A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC,DE,HL	General-Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The 8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085A provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The 8085A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.



8085A CPU Functional Block Diagram

8085A/8085A-2 (Cont.)

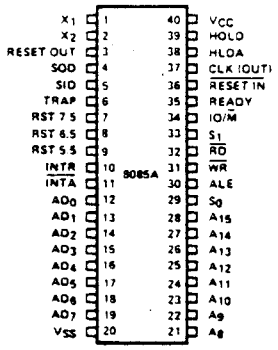


Figure 2. 8085A Pinout Diagram

8085A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

Symbol	Function
A_8–A_{15} (Output, 3-state)	Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_{0-7} (Input/Output, 3-state)	Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE (Output)	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, and IO/$\overline{M}$ (Output)	Machine cycle status:

IO/$\overline{M}$	S_1	S_0	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt Acknowledge
*	0	0	Halt
*	X	X	Hold
*	X	X	Reset

* = 3-state (high impedance)
X = unspecified

Symbol	Function
	S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$ (Output, 3-state)	READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$ (Output, 3-state)	WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR (Input)	INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

8085A/8085A-2 (Cont.)

8085A FUNCTIONAL PIN DESCRIPTION (Continued)

Symbol	Function
$\overline{\text{INTA}}$ (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of and has the same timing as $\overline{\text{RD}}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5 (Inputs)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 1.)
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

TABLE 1. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:

(1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

8155/8156/8155-2/8156-2
2048 BIT STATIC MOS RAM
WITH I/O PORTS AND TIMER

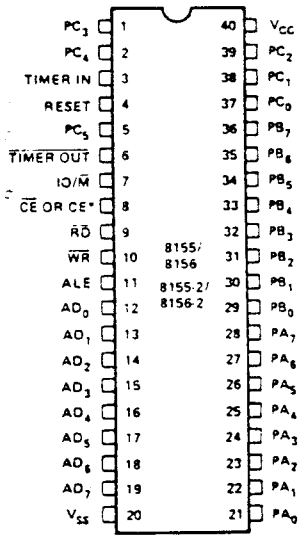
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/ Timer
- Compatible with 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 8156 are RAM and I/O chips to be used in the 8085A and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085A CPU. The 8155-2 and 8156-2 have maximum access times of 330 ns for use with the 8085A-2 and the full speed 5 MHz 8088 CPU.

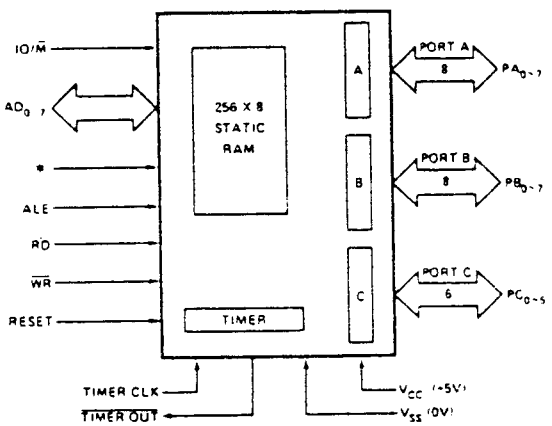
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



* 8155/8155-2 = $\overline{CE}$, 8156 8156-2 = CE

8155/8156/8155-2/8156-2 (Cont.)

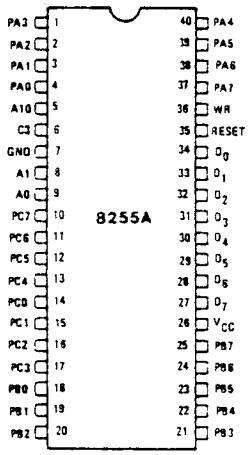
8155/8156 PIN FUNCTIONS

Symbol	Function
RESET (input)	Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085A clock cycle times.
AD_{0-7} (input)	3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155/56 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
CE or $\overline{CE}$ (input)	Chip Enable: On the 8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$ (input)	Read control: Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$ (input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/$\overline{M}$.
ALE (input)	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$ (input)	Selects memory if low and I/O and command/status registers if high.
PA_{0-7}(8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7}(8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5}(6) (input/output)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — $\overline{ABF}$ (Port A Buffer Full) PC_2 — $\overline{A\ STB}$ (Port A Strobe) PC_3 — B INTR (Port B Interrupt) PC_4 — $\overline{B\ BF}$ (Port B Buffer Full) PC_5 — B STB (Port B Strobe)
TIMER IN (input)	Input to the counter-timer.
$\overline{TIMER\ OUT}$ (output)	Timer output. This output can be either a square wave or a pulse depending on the timer mode.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

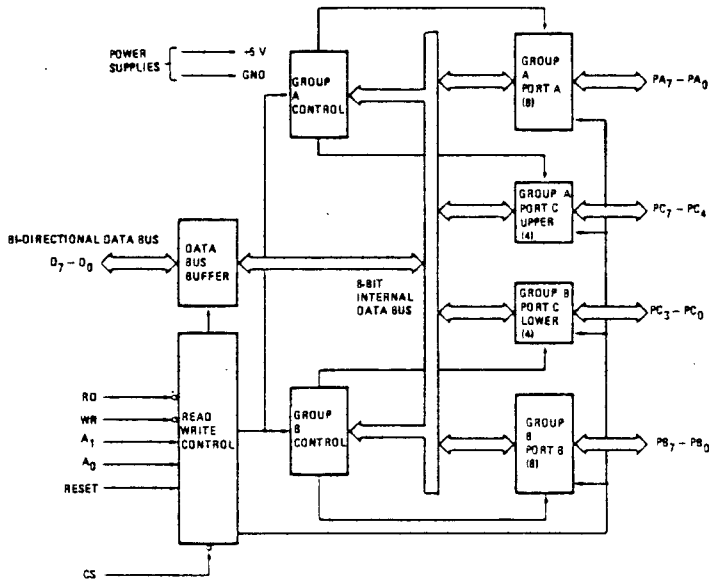
PIN CONFIGURATION

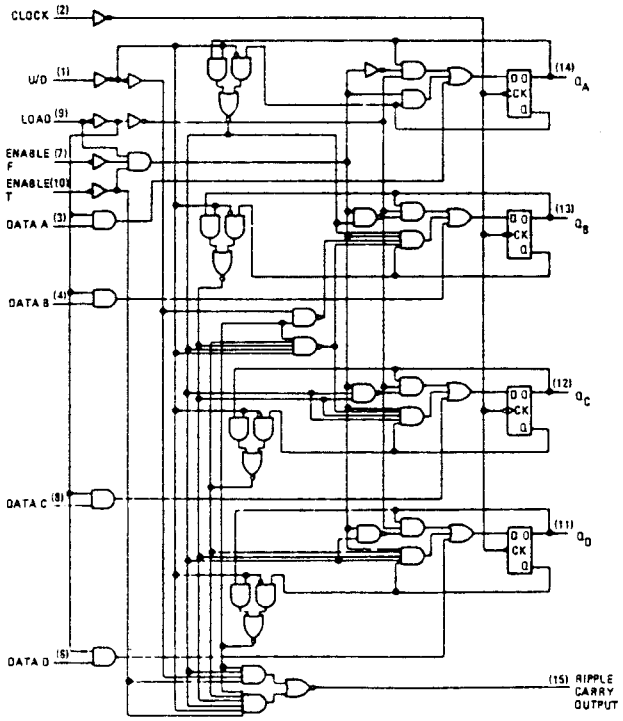


PIN NAMES

$D_7 - D_0$	DATA BUS (BIDIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7 – PA0	PORT A (BIT)
PC7 – PB0	PORT B (BIT)
PC7 – PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	5 VOLTS

8255A BLOCK DIAGRAM





TECHNICAL PUBLICATION EVALUATION FORM

To the User of This Instruction Manual:

HARRIS Corporation, RF Communications Group continually evaluates its technical publications for completeness, technical accuracy, and organization. You can assist in this process by completing and returning this form. Please specify section, page number, figure or table number where applicable.

MANUAL TITLE: _____

MANUAL NUMBER: _____ REVISION: ____ COVER DATE: _____

GENERAL	EXCELLENT	GOOD	FAIR	POOR
TEXT	[ ]	[ ]	[ ]	[ ]
SETUP/ALIGNMENT INST.	[ ]	[ ]	[ ]	[ ]
TROUBLESHOOTING INST.	[ ]	[ ]	[ ]	[ ]
TABLES	[ ]	[ ]	[ ]	[ ]
ILLUSTRATIONS	[ ]	[ ]	[ ]	[ ]
PARTS LISTS	[ ]	[ ]	[ ]	[ ]
SCHEMATIC DIAGRAMS	[ ]	[ ]	[ ]	[ ]

GENERAL COMMENTS: Please include your suggestions for improvements to the manual. Specify section, page, paragraph, figure number, or table number as applicable. Attach examples or extra pages if more space is needed.

_____
_____
_____
_____

TEAR HERE

INTRODUCTION SECTION:
COMMENT _____
_____
_____

INSTALLATION SECTION:
COMMENT _____
_____
_____

OPERATION SECTION:
COMMENT _____
_____
_____

THEORY OF OPERATION SECTION (Technical Descriptions):
COMMENT _____
_____
_____

MAINTENANCE SECTION:
COMMENT _____
_____
_____

SUB-ASSEMBLY SECTIONS:
COMMENT _____
_____
_____

NAME: _____ DATE: _____

COMPANY: _____

ADDRESS: _____

CITY: _____ STATE: _____

ZIP: _____ COUNTRY: _____

PHONE NUMBER (INCLUDE AREA CODE): _____

NOTE

U.S. POSTAL REGULATIONS NO LONGER PERMIT THE USE OF STAPLES. PLEASE SEAL THIS FORM WITH TAPE.

MAKE FIRST FOLD HERE

TEAR HERE

MAKE LAST FOLD HERE

_____

_____

_____

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL
FIRST CLASS PERMIT NO. 4033 ROCHESTER, N.Y.

POSTAGE WILL BE PAID BY ADDRESSEE

HARRIS CORPORATION
RF Communications Group
1680 University Avenue
Rochester, New York 14610 U.S.A.

ATTN: Publications Department

TAPE HERE

RF-P-671D