A18A1
SYSTEM INTERFACE PROCESSOR BOARD ASSEMBLY

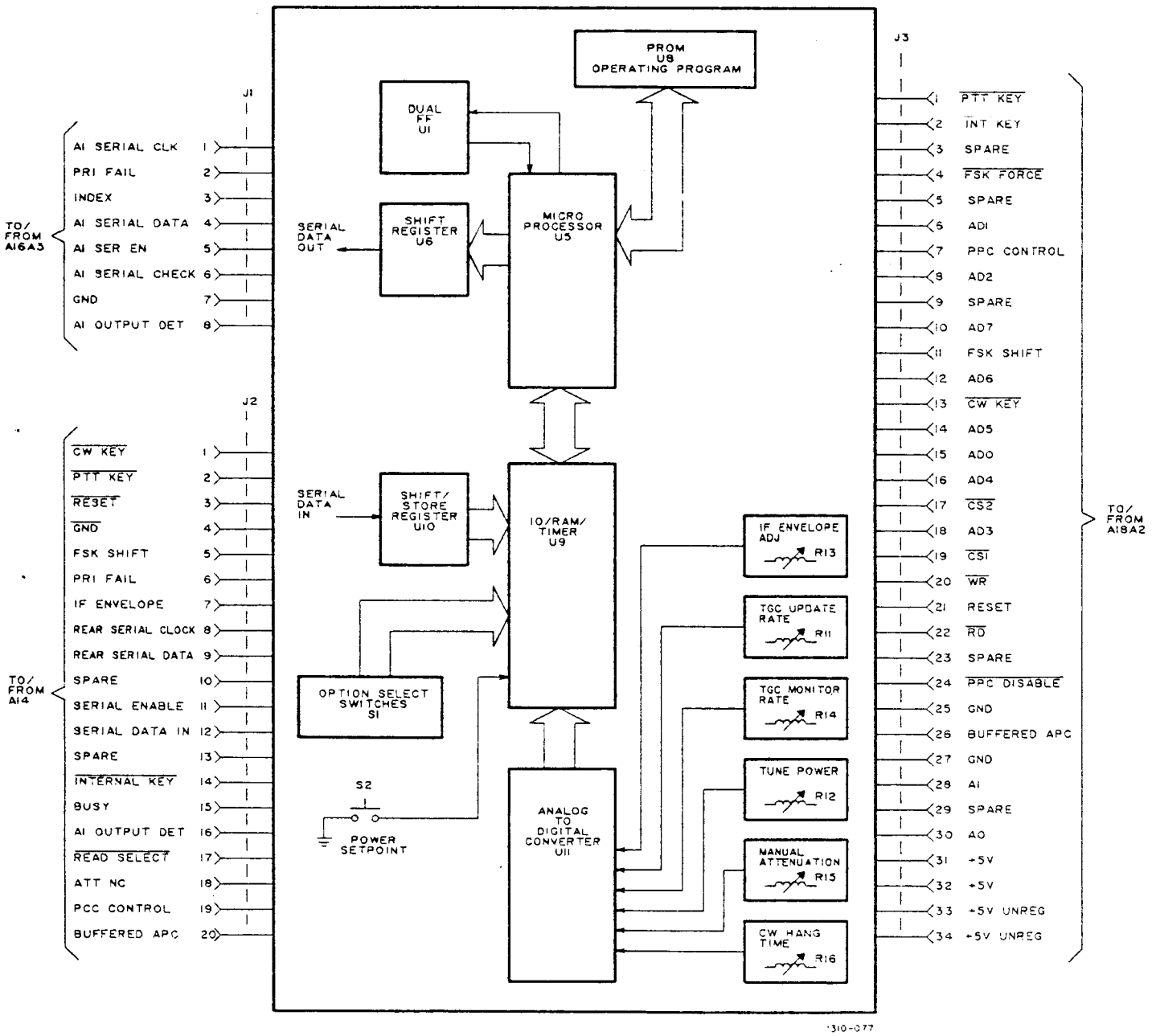


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF TABLES (Cont.)

SYSTEM INTERFACE ASSY A18A1

1. GENERAL DESCRIPTION

System Interface Assembly A18A1 is a self-contained processor unit with its own 8085A processor, RAM, and EPROM. The A18A1 and A18A2 assemblies are shown in figure1. Its primary functions are to accept PA control commands from the A14 assembly, translate these commands to the A18A2 I/O assembly, and provide readbacks from the A18A2 I/O assembly. The A18A1 assembly contains its own CPU, an 8K byte EPROM, 256 bytes of RAM memory, serial-to-parallel conversion circuits, parallel-to-serial conversion circuits, analog-to-digital conversion abilities, and a multiport I/O. Note that with the exception of serial communications with the A14 assembly, this processor board runs independently using software stored in its own EPROM. It performs its own self testing (BITE) when requested to by the exciter's BITE procedure.

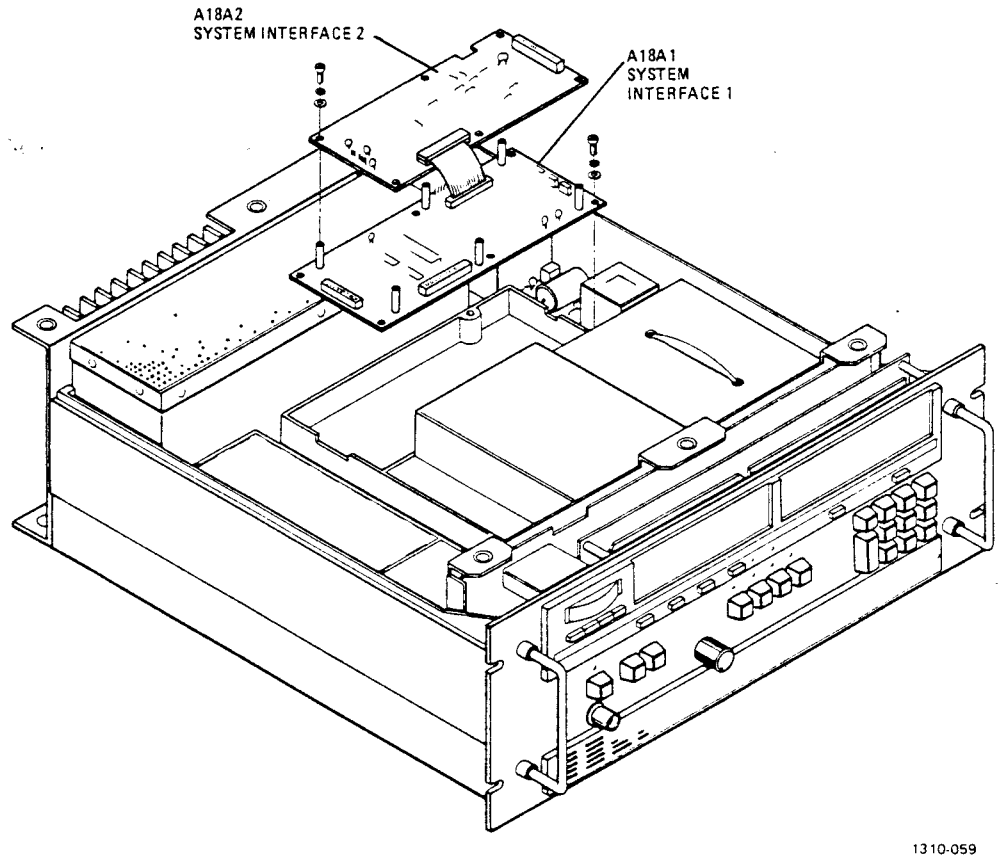


Figure 1. A18 Assembly Location

2. INTERFACE CONNECTIONS

System Interface Assembly A18A1 interface connections are shown in table 1.

Table 1. RF-1310 System Interface Assembly A18A1 Interface Lines

Connector	Function	To	From
A18A1J1-1	A1 SERIAL CLOCK	A16A3J3-1	----------
A18A1J1-2	PRIMARY FAIL	----------	A16A3J3-2
A18A1J1-3	INDEX	----------	----------
A18A1J1-4	A1 SERIAL DATA	A16A3J3-4	----------
A18A1J1-5	A1 SERIAL ENABLE	A16A3J3-5	----------
A18A1J1-6	A1 SERIAL CHECK	----------	A16A3J3-6
A18A1J1-7	GROUND	A16A3J3-7	A16A3J3-8
A18A1J1-8	A1 OUTPUT DETECT	----------	A16A3J3-8
A18A1J2-1	CW KEY	----------	A14J4-1
A18A1J2-2	PTT KEY	----------	A14J4-2
A18A1J2-3	RESET	----------	A14J4-3
A18A1J2-4	GROUND	----------	A14J4-4
A18A1J2-5	FSK SHIFT	A14J4-5	----------
A18A1J2-6	PRIMARY FAIL	A14J4-6	----------
A18A1J2-7	IF ENVELOPE	----------	A14J4-7
A18A1J2-8	REAR SERIAL CLOCK	----------	A14J4-8
A18A1J2-9	REAR SERIAL DATA	----------	A14J4-9
A18A1J2-10	SPARE	----------	----------
A18A1J2-11	SERIAL ENABLE	----------	A14J4-11
A18A1J2-12	SERIAL DATA IN	A14J4-12	----------
A18A1J2-13	SPARE	----------	----------
A18A1J2-14	INTERNAL KEY	----------	A14J4-14
A18A1J2-15	BUSY	A14J4-15	----------
A18A1J2-16	A1 OUTPUT DETECT	A14J4-16	----------
A18A1J2-17	READ SELECT	----------	A14J4-17
A18A1J2-18	ATTNC	A14J4-18	----------
A18A1J2-19	PPC CONTROL	A14J4-19	----------
A18A1J2-20	BUFFERED APC	A14J4-20	----------
A18A1J3-1	PTT KEY	A18A2P1-1	----------
A18A1J3-2	INTERNAL KEY	A18A2P2-2	----------
A18A1J3-3	SPARE	----------	----------
A18A1J3-4	FSK FORCE	A18A2P2-4	----------
A18A1J3-5	SPARE	----------	----------
A18A1J3-6	AD1	A18A2P1-6	BIDIRECTIONAL

Table 1. RF-1310 System Interface Assembly A18A1 Interface Lines (Cont.)

Connector	Function	To	From
A18A1J3-7	PPC CONTROL	----------	A18A2P1-7
A18A1J3-8	AD2	A18A2P1-8	BIDIRECTIONAL
A18A1J3-9	SPARE	----------	----------
A18A1J3-10	AD7	A18A2P1-10	BIDIRECTIONAL
A18A1J3-11	FSK SHIFT	----------	A18A2P1-11
A18A1J3-12	AD6	A18A2P1-12	BIDIRECTIONAL
A18A1J3-13	CW KEY	A18A2P1-13	----------
A18A1J3-14	AD5	A18A2P1-14	BIDIRECTIONAL
A18A1J3-15	AD0	A18A2P1-15	BIDIRECTIONAL
A18A1J3-16	AD4	A18A2P1-16	BIDIRECTIONAL
A18A1J3-17	CS2	A18A2P1-17	----------
A18A1J3-18	AD3	A18A2P1-18	BIDIRECTIONAL
A18A1J3-19	CS1	A18A2P1-19	----------
A18A1J3-20	WR	A18A2P1-20	----------
A18A1J3-21	RESET	A18A2P1-21	----------
A18A1J3-22	RD	A18A2P1-22	----------
A18A1J3-23	BUFFERED APC #2	----------	A18A2P1-26
A18A1J3-24	PPC DISABLE	A18A2P1-24	----------
A18A1J3-25	GROUND	A18A2P1-25	----------
A18A1J3-26	BUFFERED APC #1	----------	A18A2P1-26
A18A1J3-27	GROUND	A18A2P1-27	----------
A18A1J3-28	A1	A18A2P1-28	----------
A18A1J3-29	IF ENVELOPE	----------	----------
A18A1J3-30	A0	A18A2P1-30	----------
A18A1J3-31	+5 V	A18A2P1-31	----------
A18A1J3-32	+5 V	A18A2P1-32	----------
A18A1J3-33	+5 V UNREGULATED	----------	A18A2P1-33
A18A1J3-34	+5 V UNREGULATED	----------	A18A2P1-34

3. FUNCTIONAL DESCRIPTION

Figure 2 is a block diagram of the A18A1 assembly.

3.1 CPU and Clock Generation

The 8085AH-2 microprocessor executes the application program stored in EPROM U8. The CPU operates off the 6.0 MHz crystal Y1, internally divides this frequency to 3.0 MHz and outputs it on pin 37. The 3.0 MHz is fed to U9 where it is internally divided down to 1 kHz, the frequency of the real time clock, which returns to the processor as the RST 7.5 input. The 3.0 MHz is also fed to U2 and is divided by four to achieve 750 kHz, the

operating frequency of the A/D converter U11. The three high order address bits of U5 (A13, A14, and A15 assemblies) are inputs to decoder U4. U4 produces active low chip selects for the peripheral circuits on the A18 assembly. The remaining high address bits (A8 through A12) are used exclusively to address the EPROM U8. The multiplexed low address/data bus of U5 is input to address latch U7, serial out register U6, EPROM U8, I/O memory chip U9, and the A18A2 assembly via J3. The low address side of U7 provides the addressing for U8, A/D converter U11, and A18A2. The microprocessor is reset simultaneously with the U24 processor on Control Board Assembly A14 any time a RESET is initiated on the A14 assembly. Dual flip-flop U1 and NOR gate U3D provide communications control between the system interface board and the control board. Resistor pack R5 provides the pull-up termination for the low address/data bus. The active high interrupt lines of the CPU are assigned as follows:

- RST 5.5 and RST 6.5 are used for communications control between the assemblies
- RST 7.5 is used for the real time clock

3.2 Memory

The firmware program to run the system interface assembly is independent of that used on the A14 assembly and is stored in its own EPROM U8. A chip select from U4 enables the EPROM. Jumpers E1, E2, and E3 are reserved for further EPROM expansion.

The information stored in U8 is part of the RF-1310 system interface software and cannot be altered by the customer.

CAUTION

Do not remove the opaque protective shield on the EPROMs. EPROMs are ultraviolet erasable over extended periods of exposure to fluorescent light or sunlight. Extended exposure can erase the memory information.

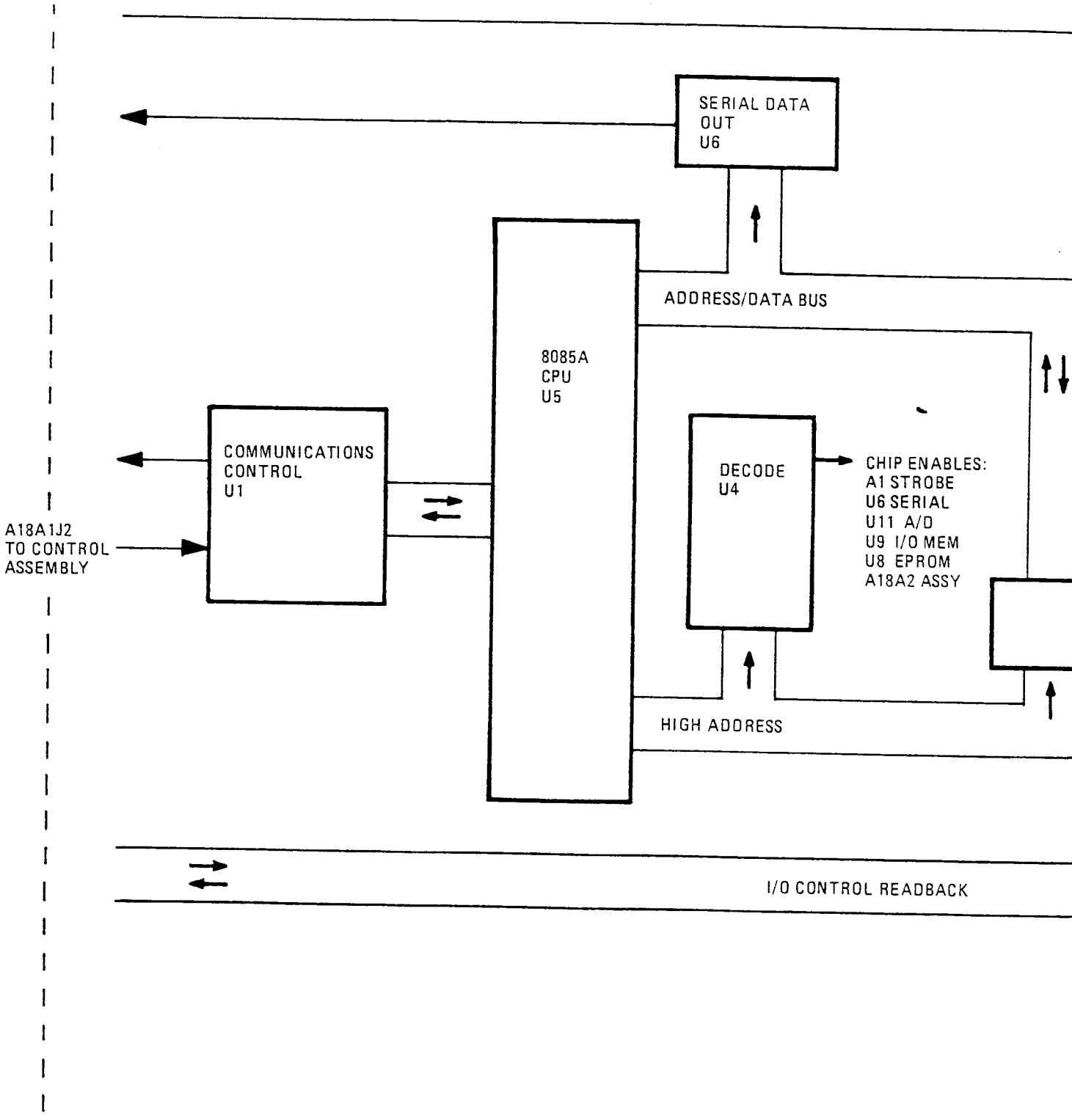
There are 256 bytes of RAM in I/O timer device U9. U9 is selectable as either a memory device, or an I/O device depending on the status of its control line IO/M pin 7. Data is accessed when it is a memory device by using the $\overline{RD}$ and WR lines in conjunction with the low address/data bus. Unlike the RAM on the control assembly, this device does not have battery backed storage capabilities.

3.3 Serial Communications

System Interface Assembly A18A1 communicates with Control Board Assembly A14 by serial data transmissions. Data is transferred serially, eight bits at a time. Varying numbers of eight bit groups (bytes) are needed to properly relay messages back and forth. Data is transmitted in one direction at a time (simplex). While data is being relayed, the receiving assembly is inhibited from further transmission activity until all bytes are received. These messages are formatted in a structured manner and may consist of command or readback information, message start and finish flags, total number of bytes in message count, and/or message data integrity codes (checksums).

3.3.1 Serial Reception Circuit

The serial reception circuit receives data from the control board as rear serial data and is input to the shift/store register U10. It is clocked into U10 by the rear serial clock, and since the READ SELECT line from the control board is being held high by the A14 Assembly CPU, this clock only affects U10. A serial enable is then sent to the control board and two things happen. The serial data inputted to U10 is strobed into its output


SERIAL DATA
OUT
U6
ADDRESS/DATA BUS
8085A
CPU
U5
COMMUNICATIONS
CONTROL
U1
A18A1J2
TO CONTROL
ASSEMBLY
DECODE
U4
CHIP ENABLES:
A1 STROBE
U6 SERIAL
U11 A/D
U9 I/O MEM
U8 EPROM
A18A2 ASSY
HIGH ADDRESS
I/O CONTROL READBACK

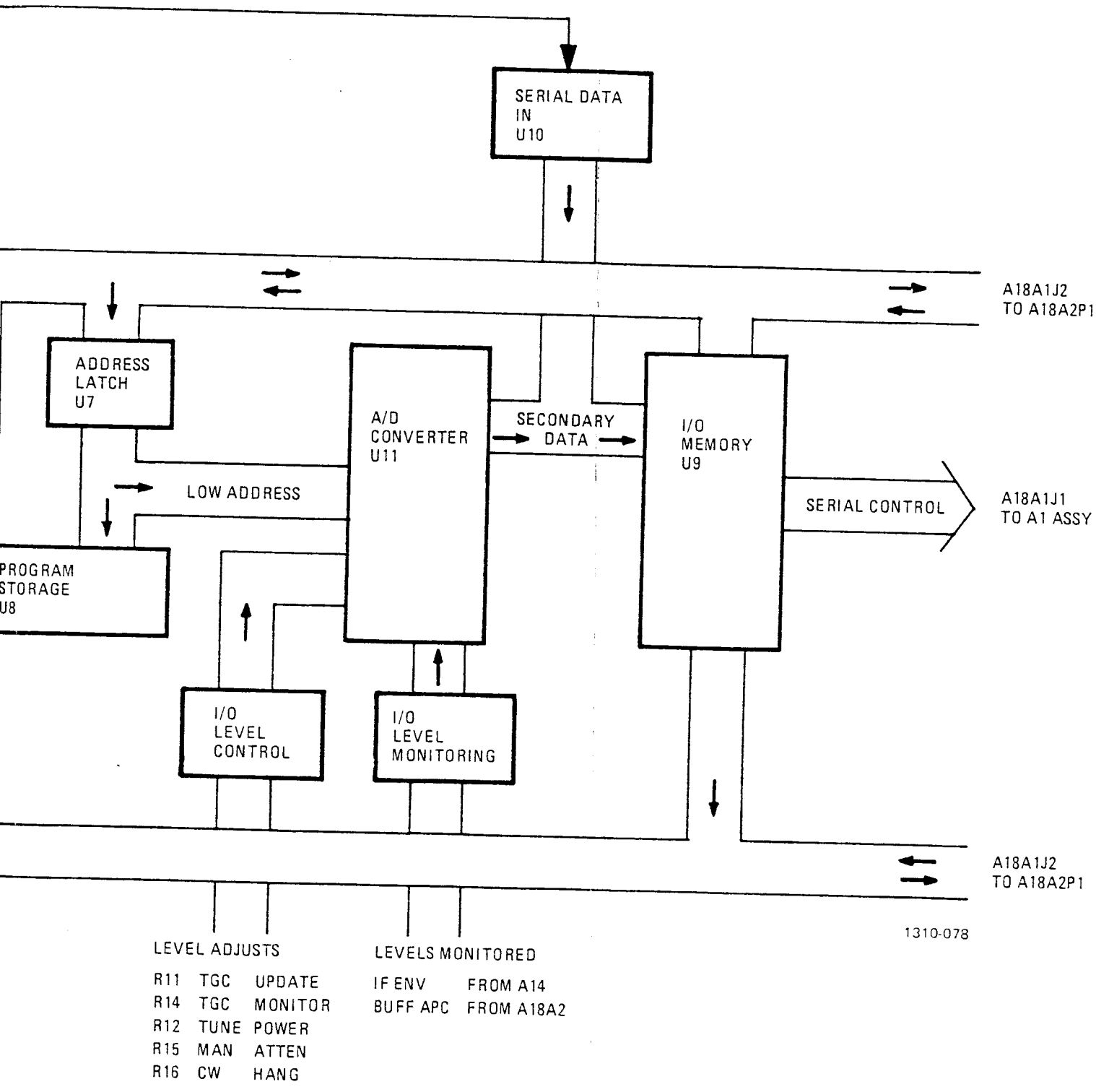


Figure 2. System Interface Assembly A18A1 Block Diagram

registers, and the clock input to flip-flop U1-11 pulses high, forcing U1-9 output high. This is the RST 6.5 input to the CPU, signalling the processor that a byte is being received. This signal also goes back to the control board as the line labeled BUSY. This signals the control board processor that the system interface is processing the received byte. When the system interface is done accepting this byte, the CPU pulses its SOD line. This pulse clears U1, which clears the BUSY line to signal the control board that all reception is complete and the process can be repeated. This will continue until all the bytes of the received message have been interpreted. The data in U10 is read in to U9. The data bus connecting U10 to U9 is shared with A/D U11. Pin 39 of U9 provides the output enable control for U10 and U11 to control this data bus.

3.3.2 Serial Transmission Circuit

Data is transmitted from the A18 assembly to the A14 assembly in the following manner. The byte to be transmitted is put on the data bus (AD0 through AD7). Shift register U6 is enabled by a pulse sent from U4, via U3. I/O device U9 sets the attention line (ATTNC) to Control Board Assembly A14, indicating a message is ready to be sent. The control board in turn lowers the READ SELECT line to the system interface assembly. This READ SELECT line is gated through U3 to enable the rear serial clock input to register U6. The data is shifted out of U6 to the control board. When the control board receives this byte, it raises the READ SELECT line to remove the clock from U6 and force the Q8 output of U1-5 high. This tells the CPU that the control board has received the byte. The ATTNC line is forced low and a pulse is output on SOD to clear the RST 5.5 line. This enables the transmission process to be repeated.

3.4 Parallel I/O

Programmable I/O timer U9 provides a variety of input/output control and monitoring on System Interface Assembly A18A1. This device has three I/O ports. Two are used as inputs and one as an output. Table 2 lists the three port assignments.

Table 2. 8155A Port Dedication

Port	Function
PA Input	Secondary data bus receives serial data or A/D conversion data.
PB Input	PA setup switch and pushbutton S2 (See paragraph 4, TGC Select Switch), internal key, and A1 serial check.
PC Output	A1 serial control lines, FSK force (used during BITE), ATTNC, PPC disable, and secondary data bus control.

3.5 Analog Inputs

A/D converter U11 handles the analog-to-digital conversions on the system interface assembly. Five of the analog inputs are from potentiometers R11 through R16 and set various PA system operational parameters. (See paragraph 6.1, Alignment.) One input is reserved for system interface BITE, while one additional line monitors the average power control (APC) level coming from the A18A2 assembly. One line monitors the IF sample voltage. A/D U11 operates off its own reference voltage, ensuring a high degree of accuracy in its measurements.

4. TRANSMITTER GAIN CONTROL (TGC) SELECT SWITCH

DIP switch S1 along with pushbutton S2 are used on the system interface processor board to select various TGC operating parameters for the RF-1310 Exciter and transmitting system. Table 3 lists the S1 switch assignments.

Table 3. Options Switches

Switch Function	Description	
S1-1	TGC Learn Enable	Determines if full power attenuation value used is the one stored in the A14 RAM or if a new one is learned and stored at the end of a PA tune cycle. Closed = Learn Disable - attenuation value is the one stored in A14 RAM Open = Learn - a new value of attenuation needed for full power out will be learned and stored in A14 RAM
S1-2	Attenuation Control	Determines if attenuator control values are a function of what is read from potentiometer R15 or if normal TGC operation is in effect. Closed = Attenuation Manual - control value is read directly from R15 and TGC is disabled. This value may be stored in the A14 RAM as the learned value for a particular frequency by checking that S1-1 is closed and depressing S2. Open = Attenuation Auto - normal attenuation control under TGC.
S1-3	Coupler Control	Tells exciter to include coupler in tune cycle. Closed = no coupler/all couplers Open = RF-601 coupler only
S1-4	Signal Generator	Allows exciter to be operated as a signal generator. In this mode, attenuation is set to front panel value. Exciter is ready when placed in operate and exciter must be keyed for output. PA is disabled from keying. Closed = exciter is in normal operating mode Open = exciter is in generator mode

5. SYSTEM INTERFACE BITE

The self-testing procedure performed on System Interface Assembly A18A1 is done in a similar manner to that of Control Board Assembly A14. The tests are done sequentially in order of importance. If a test fails, the test will stop and the appropriate error code will be displayed on the front panel. The order in which these tests are performed is as follows:

- Communication Test
- EPROM Test
- RAM Test
- I/O Test
- A1 Output Amp Communication Test
- A/D Converter Test

A failure in any of these tests will generate the appropriate error code listed in table 4. This error code is sent to Control Board Assembly A14. The error code will be displayed on the front panel of the exciter along with the System Interface Assembly A18A1 number. For example, if the RAM test failed, the front panel display would indicate "ASSY 18 FAULT 03". If there were no errors in any of the system interface assembly tests, nothing would be displayed on the front panel, and the control assembly BITE procedure would continue.

Table 4. System Interface BITE Codes

Code	Fault
01	Serial Communications
02	ROM Failure
03	RAM Failure
04	I/O Failure
05	Output Amp Communication
06	A-to-D EOC Failure
07	A-to-D Conversion Failure

5.1 Communications

This test ensures proper serial communication between System Interface Assembly A18A1 and the Control Board Assembly A14. The A14 assembly sends a checksum byte code as part of the BITE start message. This code is verified by System Interface Assembly A18A1 and sent back to the control board where it is verified. Any discrepancies will cause the fault code to be displayed.

5.2 ROM Test

The ROM test is performed next. EPROM U8 contains all the firmware used to control the system interface and is tested to ensure that the information it contains is correct. This information is factory programmed; if an error is determined in this test, some preliminary operational checks should be made. If no problems are found, the device should be replaced by ordering a new one from the factory.

5.3 RAM Test

After the ROM test, the read/write capabilities of the 256 bytes of RAM memory available in the 8155 chip U9 are checked. If any faults are found, the proper fault code will be displayed.

5.4 I/O Test

The ability of the microprocessor to read and write to the A18A2 assembly is tested next. A bit pattern is written to a latch on the A18A2 assembly. The data in the latch is then read and compared to the original bit pattern. A fault code is displayed if the two patterns are not the same.

5.5 A1 Serial Test

Following the I/O test, the ability of the system interface assembly to serially communicate with output amplifier A1 is tested. This serial communications is necessary to control the output attenuators. The test is done by toggling the lowest bit in the serial attenuator command stream from high to low and checking to see that the A1 serial check bit did change. Any problem will display the proper fault code.

5.6 A to D Test

A/D converter U11 is tested after all other A18 assembly tests have been passed. The microprocessor reads the digital representation of the fixed voltage present at U11-1. A failure to generate the proper analog-to-digital conversion will be indicated by the appropriate fault code.

6. MAINTENANCE

6.1 Alignment

There are six potentiometers on the A18A1 assembly that require adjustments. They are primarily used in TGC operations. Table 5 lists the potentiometers and brief description of their functions. Alignment depends on the particular application and is covered in the appropriate system manual.

Table 5. A18A1 Assembly Potentiometers

Potentiometer	Description	
R11	TGC Update Rate	Sets the rate at which the TGC circuitry is updated to make power corrections. Normally set = midrange 2.5 Vdc @ U11-28.
R12	Tune Power	Adjusts the amount of exciter drive to the PA during a tune cycle.
R13	IF Envelope	Sets the exciter RF signal level to the normalized value for TGC operation. Normally set = 4.5 Vdc @ TP1 while keyed and in CW.
R14	TGC Monitor	Varies the rate at which long term TGC samplings are made. Clockwise = one set samples/10 seconds Counterclockwise = four set samples/1 second
R15	Manual Attenuation	Varies the range of manual output attenuation from 0 to 8 dB. Clockwise = maximum 8 dB Counterclockwise = minimum 0 dB
R16	CW Hang Time	Sets amount of time system key is held after exciter input key is released. Clockwise = 1.25 second delay Counterclockwise = no delay

6.2 Troubleshooting

Most of the circuitry on the system interface assembly is controlled directly or indirectly by the microprocessor. Standard digital troubleshooting methods will isolate most faults to the component level. Circuit areas involved in minor faults can be determined by BITE fault codes. General or major failures are best handled by proceeding, in order, through the checks outlined below.

6.2.1 Communications

The first and most important item to check is the ability of the system interface to communicate with the control board and vice versa. The easiest way to verify communications is to depress the AMP OFF and STBY buttons on the exciter front panel. If the LED above each button lights when the respective button is pressed, the two boards are communicating properly. If this does not happen, then the system interface board must be checked by using the procedures listed below.

6.2.2 CPU

If the microprocessor U5 is running, it can be used to debug several circuits on the A18A1 assembly. However, it must first be determined that the 8085AH-2 is running.

The following inputs must be present in order for the device to run.

- U5-1, 2 Crystal inputs - 6.0 MHz
- U5-36 Reset input - HIGH

The A18A2 assembly + 5 volt supply should measure between + 4.75 and + 5.1 volts. Following is a list of CPU outputs that should be present.

- U5-37 Clock out - 3 MHz square wave
- U5-3 Reset out - low
- U5-31 Write - active low pulses
- U5-32 Read - active low pulses
- U5-30 Address latch enable - active high pulses

When the CPU is running and executing the application software, its outputs will only be active a portion of each millisecond. The rest of the time it will stop waiting for the real time clock interrupt on pin 7.

6.2.3 Device Selection

Address decoder U4 aids the access of peripheral devices by outputting low active chip enable signals corresponding to the high order bits of the CPU. During normal operation, the enables can be seen on pins 10, 13, and 15 of U4.

6.2.4 Memory

Problems in the memory circuitry can be difficult to isolate. If BITE indicates a PROM failure, the fact that BITE even runs indicates that the address and data bus are operating properly and the PROM is being accessed. However, invalid data in device U8 is probably causing this error and it should be replaced.

If a RAM failure is indicated, some checks are in order. Check for high going pulses on the IO/$\overline{M}$ line U9-7 and on the ALE line U9-11. Also check to see that the chip is being enabled by low going pulses on U9-8. Make sure that the RESET line U9-4 is low.

6.2.5 Timing

The timing circuits on the A18A2 assembly are minimal and easy to check. Look for the following TTL square wave signals at the noted locations.

- U9-3, U2-3 3.0 MHz
- U5-7 1.0 kHz - output of U9
- U11-10 750 kHz - output of U2

6.2.6 Serial Transmission Circuitry

As stated in paragraph 6.2.1, the easiest way to verify interboard communication is to move the front panel switches back and forth between AMP OFF and STBY.

When messages are being sent, high going pulses of TTL levels should be seen at the following locations:

- U6-3 Serial Data In
- U6-10 and U10-3 Rear Serial Clock
- U10-2 Rear Serial Data
- U5-8 and U5-9 Communications Interrupts
- U6-9 Data Out Load Pulse

In addition, a low going pulse should be seen on U5-4.

6.2.7 Parallel I/O

Three ports of I/O are used on this assembly through I/O timer U9. By going through the checks for U9 outlined in 6.2.4, the general operation of U9 can be verified. If it is found that a particular port is being handled improperly, then U9 may be at fault.

6.2.8 Analog Conversions

A/D converter U11 is used primarily to read the potentiometer settings of R11 through R16. Starting any conversion consists of writing two narrow active high pulses to U11-6. After 10 microseconds (or less), the end of conversion line (EOC) will go low. It will stay low for 100 microseconds, and after it goes high again there will be one active high pulse on U11-9. At this point, the digital version of the input signal read will be transferred to the secondary data bus and into U9. Signals of interest in the analog conversion circuit are:

- U2-3 Clock in - 3 MHz TTL square wave
- U2-9 A/D clock - 750 kHz TTL square wave
- U11-6, 2 Start Conversion - two narrow high going pulses every time a conversion is initiated
- U11-7 End of Conversion - 85 microseconds low at the completion of a conversion

- U11-9 Output enable - narrow high going pulse after a conversion has been made
- IN0 through IN7 All analog inputs should be between 0 and + 5 Vdc.

7. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components of the A18A1 assembly are listed in table 6. Figure 3 shows the component locations of the A18A1 assembly. Figure 4 is the schematic diagram of the assembly.

Table 6. System Interface Assembly A18A1 Parts List

Ref. Desig.	Part Number	Description
A18A1	10121-6310	SYSTEM INTERFACE PROCESSOR ASSEMBLY
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	C26-0016-150	CAP 15UF 20% 16V TANT
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	C26-0010-680	CAP 68UF 20% 10V TANT
C9	M39014/02-1310	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	C26-0035-159	CAP 1.5UF 20% 35V TANT
C12	C26-0035-159	CAP 1.5UF 20% 35V TANT
C13	C26-0025-339	CAP 3.3UF 20% 25V TANT
CR1	1N6263	DIODE .40W 60V HOT CARR
CR2	1N6263	DIODE .40W 60V HOT CARR
CR3	1N6263	DIODE .40W 60V HOT CARR
CR4	1N6263	DIODE .40W 60V HOT CARR
CR5	1N5231B	DIODE 5.1V 5% .5W ZENER
J1	J46-0032-008	CONN,8 PIN
J2	J46-0013-020	HEADER, PROTECTED, 20 PIN
J3	J46-0013-034	CONN, 34 PIN
Q1	2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R2	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R3	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R4	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R5	R50-0010-103	RES,10SIP, 10K,2.0%, 9RES
R6	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R7	R65-0003-471	RES,470 5% 1/4W CAR FILM
R8	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R9	R50-0010-103	RES,10SIP, 10K,2.0%, 9RES
R10	R65-0003-911	RES,910 5% 1/4W CAR FILM

Table 6. System Interface Assembly A18A1 Parts List (Cont.)

Ref. Desig.	Part Number	Description
R11	R30-0008-203	RES,VAR,PCB 20K 1/2W 10%
R12	R30-0008-203	RES,VAR,PCB 20K 1/2W 10%
R13	R30-0008-203	RES,VAR,PCB 20K 1/2W 10%
R14	R30-0008-203	RES,VAR,PCB 20K 1/2W 10%
R15	R30-0008-203	RES,VAR,PCB 20K 1/2W 10%
R16	R30-0008-203	RES,VAR,PCB 20K 1/2W 10%
S1	S50-0001-004	SW SPST 4SEC .1A SLD DIP
S2	S06-0002-100	SW PB SPST NO MOM BLK PCT
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
U1	I05-0000-074	IC 74LS74 PLASTIC TTL
U2	I05-0000-074	IC 74LS74 PLASTIC TTL
U3	I05-0000-002	IC 74LS02 PLASTIC TTL
U4	I05-0000-138	IC 74LS138 PLASTIC TTL
U5	I27-0006-001	IC 8085A MICRO 8-BIT PLA
U6	I01-0000-153	IC 4021B PLASTIC CMOS
U7	I05-0000-373	IC 74LS373 PLASTIC TTL
U8	SEE NOTE	PROGRAMMED PROM
U9	I26-0003-001	IC 8155-2 STAT RAM 256X8
U10	I01-0000-156	IC 4094B PLASTIC CMOS
U11	I40-0011-001	IC ADC0809 PLASTIC CMOS

NOTE

The part number for U8 is 10121-8XXX-X, where XXX-X is the four character software kit code found on the PROM label. For example, if the code is 501C, the part number for the programmed PROM is 10121-8501-C.

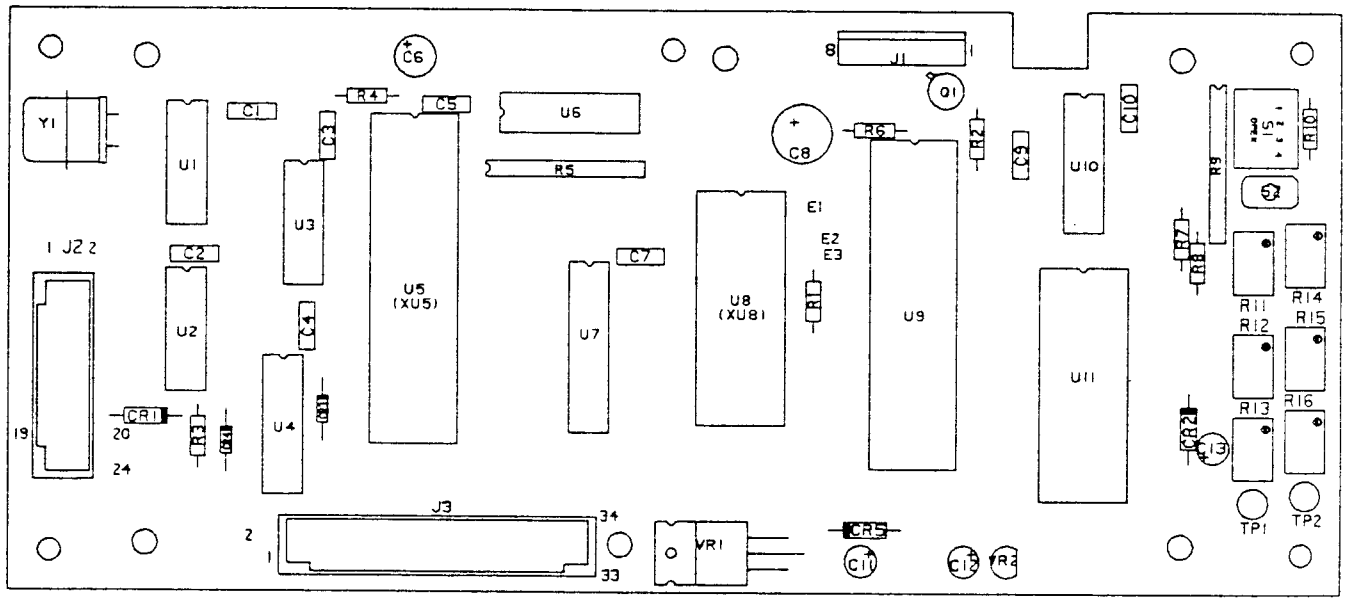


Figure 3. System Interface Processor Board Assembly A18A1
Component Location Diagram (10121-6310)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. FOR ALTERNATE PROM TYPES
   JUMPER E1 TO E2 FOR 2732
   USE NO JUMPER FOR 2764
   JUMPER E2 TO E3 FOR 27128
6. SWITCH S1 OPTIONS:
   - S1-1 TGC PRESET (CLOSED)
     TGC LEARN (OPEN)
   - S1-2 MANUAL ATTENUATION (CLOSED)
     NORMAL (OPEN)
   - S1-3 COUPLER ATTACHED (OPEN)
     NO COUPLER (CLOSED)
   - S1-4 SIGNAL GENERATOR MODE (OPEN)

ARE SHOWN.
IX WITH
GNATION.

1/4W, ±5%.

OF ARADS.

REFERENCE ONLY.
T NO. IN PARTS LIST.

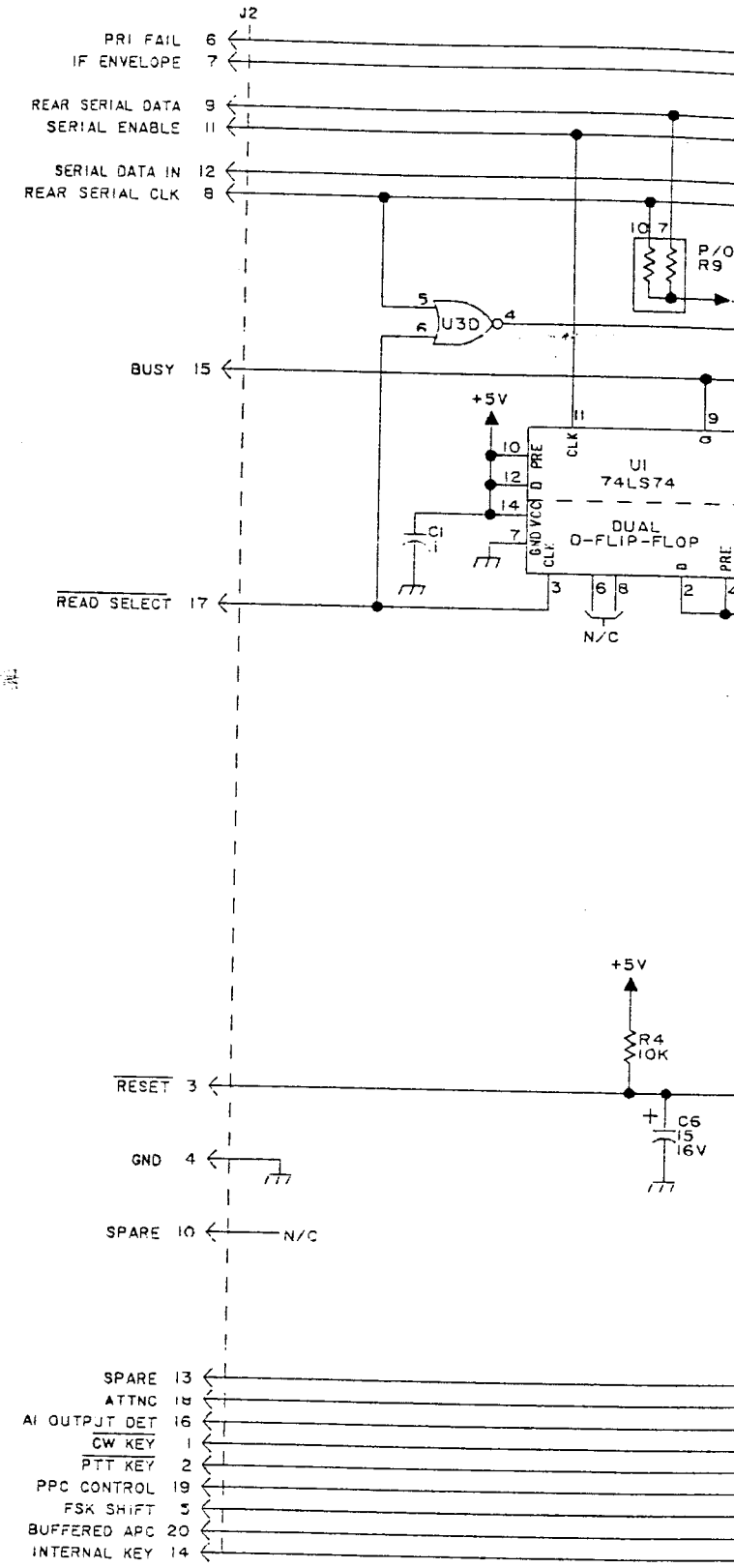
6. SWITCH SI OPTIONS:

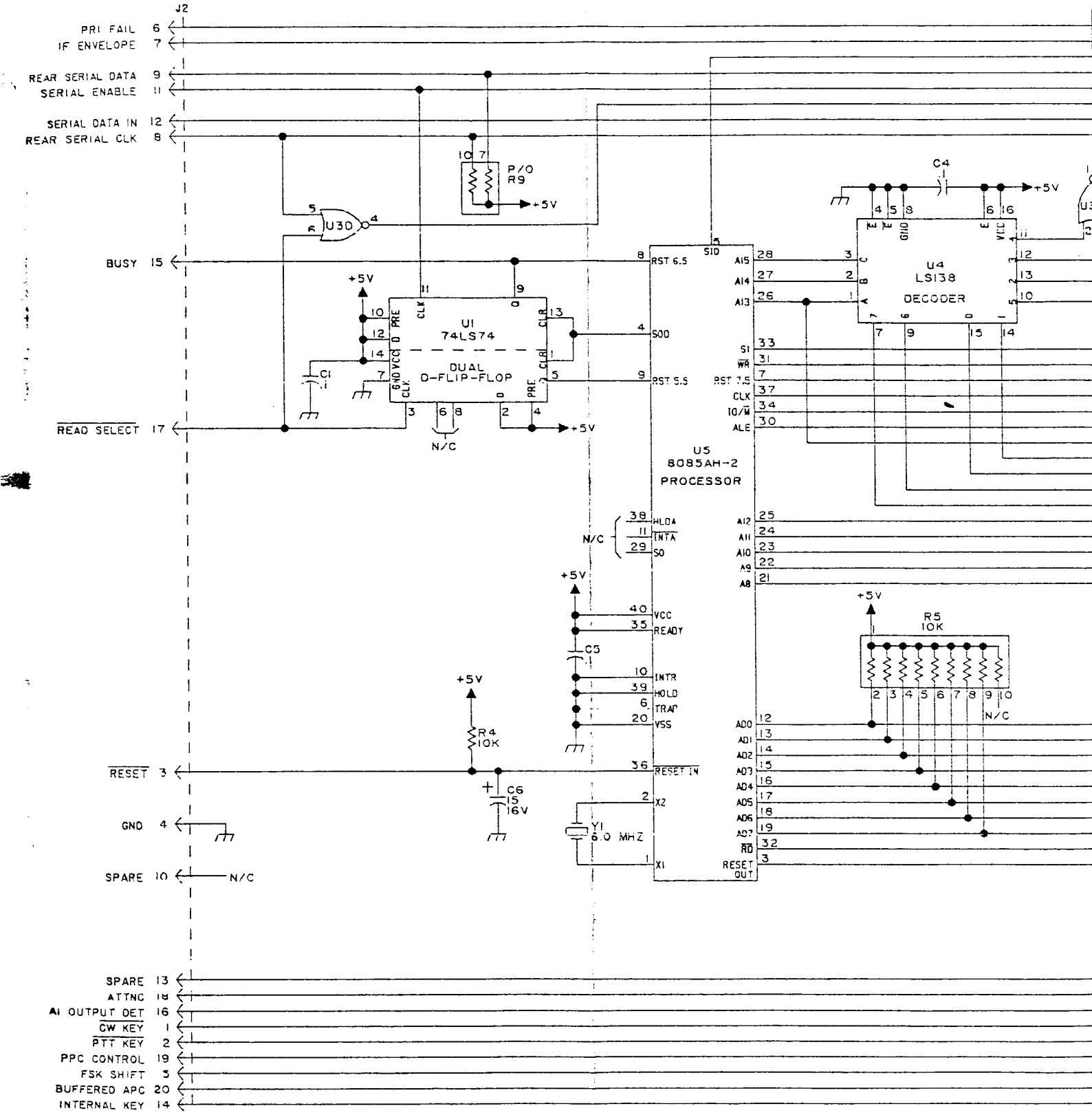
SI-1 TGC PRESET (CLOSED)
TGC LEARN (OPEN)

SI-2 MANUAL ATTENUATION (CLOSED)
NORMAL (OPEN)

SI-3 COUPLER ATTACHED (OPEN)
NO COUPLER (CLOSED)

SI-4 SIGNAL GENERATOR MODE (OPEN)




J2
PRI FAIL 6
IF ENVELOPE 7
REAR SERIAL DATA 9
SERIAL ENABLE 11
SERIAL DATA IN 12
REAR SERIAL CLK 8
P/O R9
+5V
U30
BUSY 15
U1 74LS74 DUAL D-FLIP-FLOP
C1 .1
READ SELECT 17
N/C
U5 8085AH-2 PROCESSOR
RST 6.5
SID
SOD
RST 5.5
HLDA
INTA
SO
VCC
READY
INTR
HOLD
TRAP
VSS
RESET IN
X2
X1
Y1 6.0 MHZ
C5
C6 15 16V
R4 10K
RESET 3
GND 4
SPARE 10
U4 LS138 DECODER
C4
A15
A14
A13
S1
WR
RST 7.5
CLK
IO/M
ALE
A12
A11
A10
A9
A8
R5 10K
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
RD
RESET OUT
SPARE 13
ATTNC 18
A1 OUTPUT DET 16
CW KEY 1
PTT KEY 2
PPC CONTROL 19
FSK SHIFT 5
BUFFERED APC 20
INTERNAL KEY 14

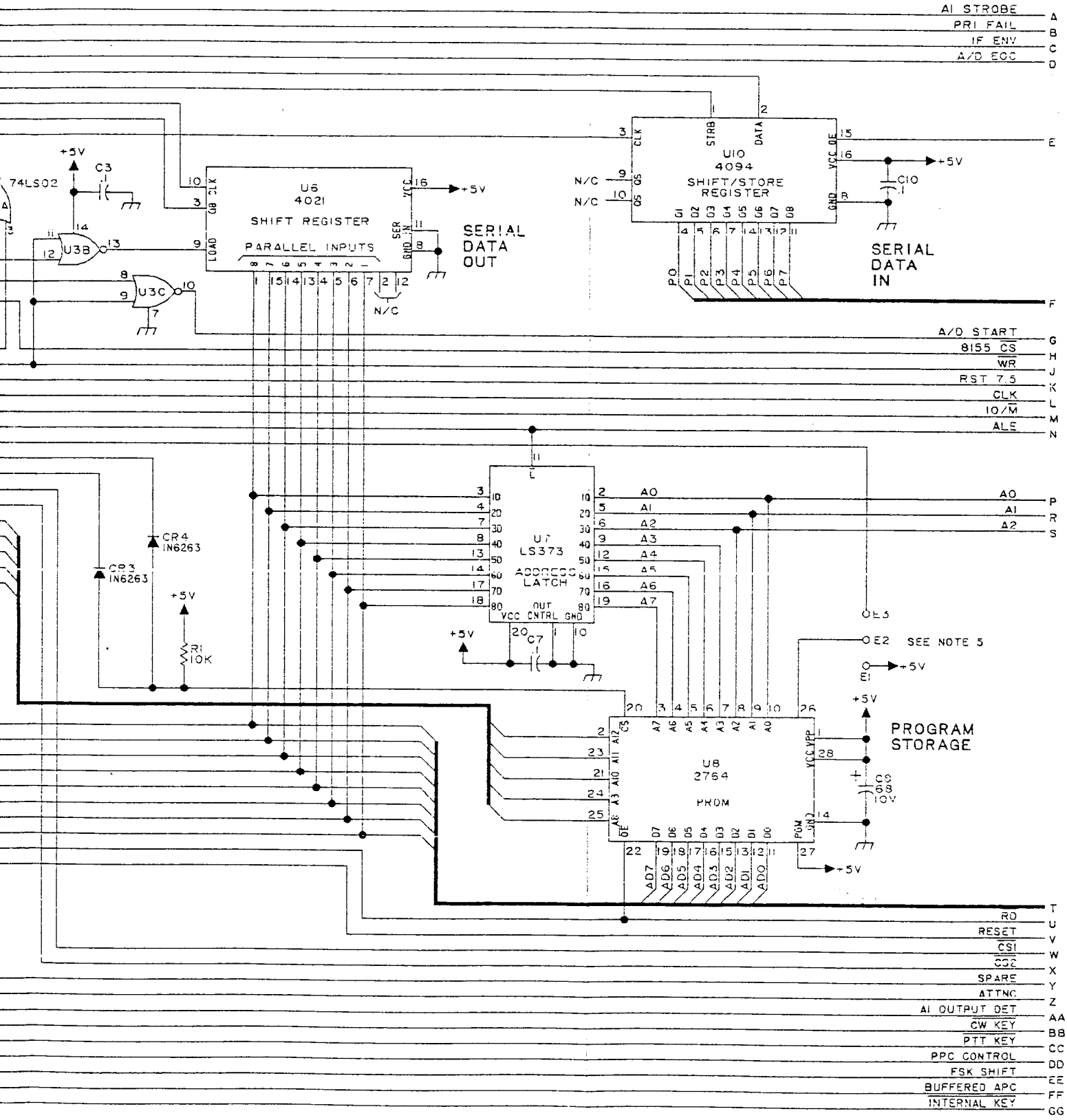
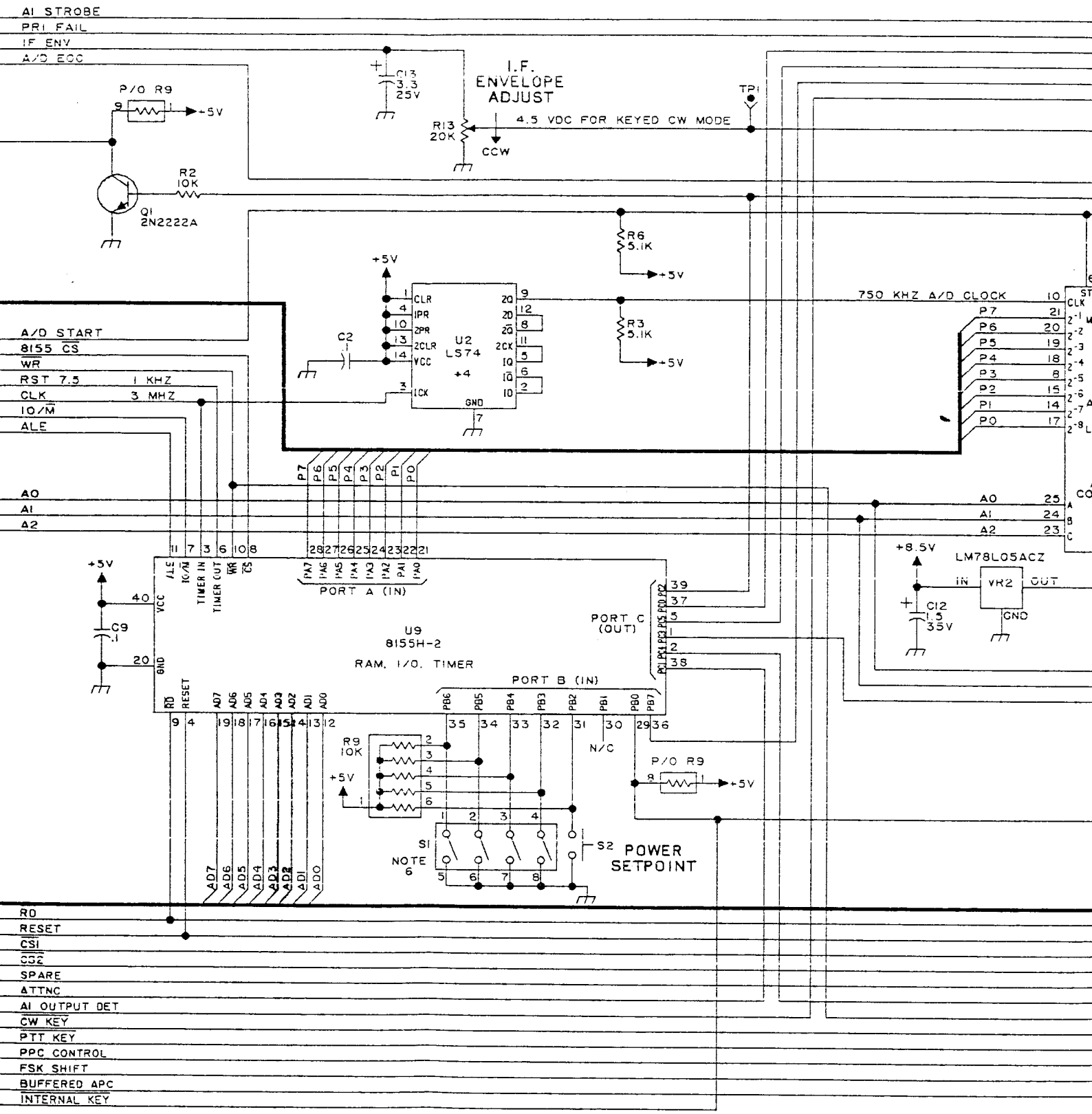


Figure 4. System Interface Assembly, A18A1 Schematic Diagram (10121-6311 Rev. F) (Sheet 1 of 2)


AI STROBE
PRI FAIL
IF ENV
A/D EOC
P/O R9
+5V
C13
3.3
25V
I.F.
ENVELOPE
ADJUST
TP1
R13
20K
4.5 VDC FOR KEYED CW MODE
CCW
R2
10K
Q1
2N2222A
R6
5.1K
+5V
R3
5.1K
750 KHZ A/D CLOCK
A/D START
8155 CS
WR
RST 7.5
1 KHZ
CLK
3 MHZ
IO/M
ALE
C2
U2
LS74
+4
CLR
1PR
2PR
2CLR
VCC
1CK
GND
A0
A1
A2
P7
P6
P5
P4
P3
P2
P1
P0
PORT A (IN)
PORT C
(OUT)
U9
8155H-2
RAM, I/O, TIMER
PORT B (IN)
TIMER IN
TIMER OUT
RD
RESET
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
PB6
PB5
PB4
PB3
PB2
PB1
PB0
N/C
C9
.1
R9
10K
P/O R9
+5V
S1
S2
POWER
SETPOINT
NOTE
6
+8.5V
LM78L05ACZ
IN
VR2
OUT
GND
C12
1.5
35V
RD
RESET
CS1
CS2
SPARE
ATTNC
AI OUTPUT DET
CW KEY
PTT KEY
PPC CONTROL
FSK SHIFT
BUFFERED APC
INTERNAL KEY

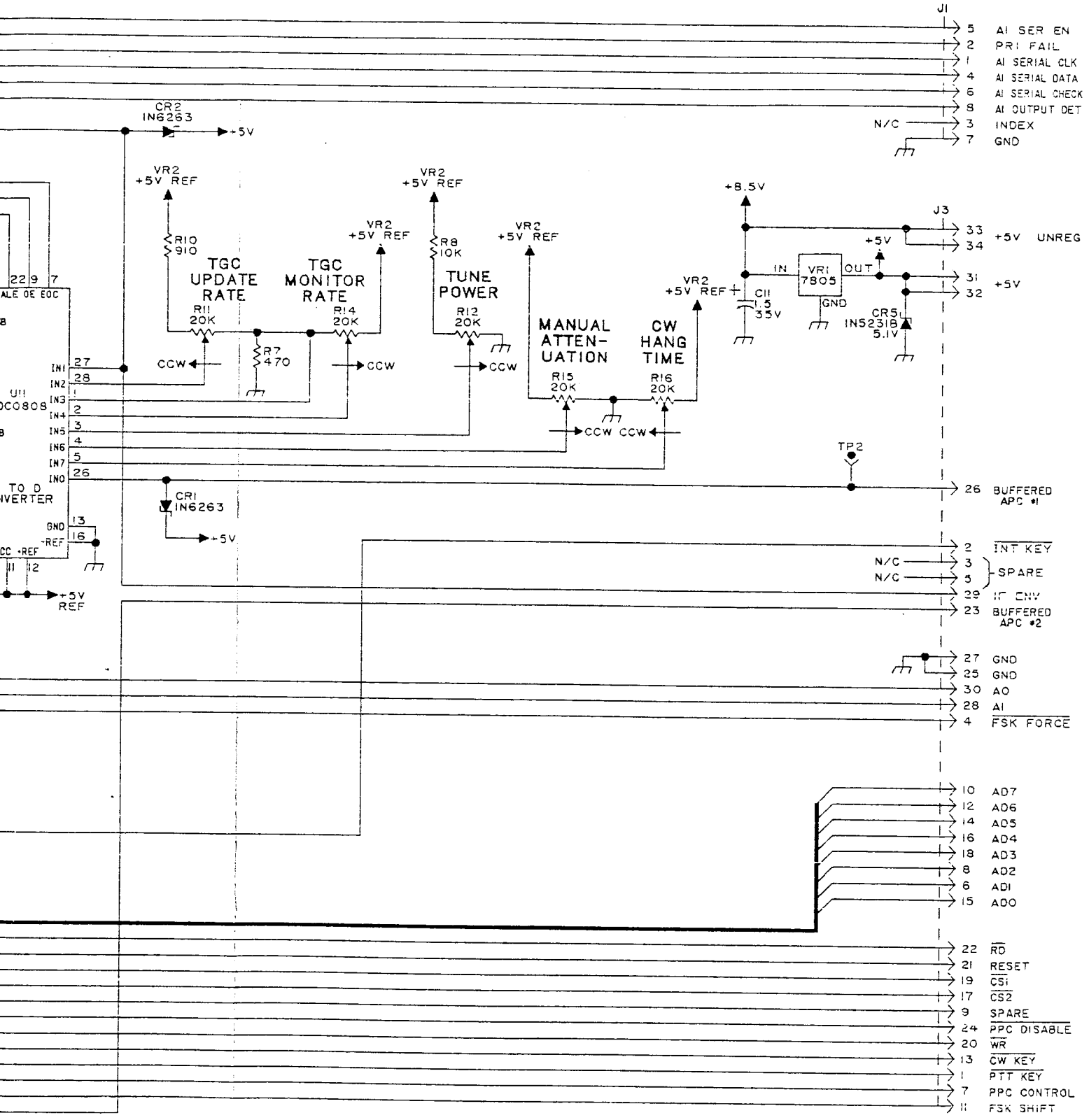


Figure 4. System Interface Assembly, A18A1 Schematic Diagram (10121-6311 Rev. F) (Sheet 2 of 2)