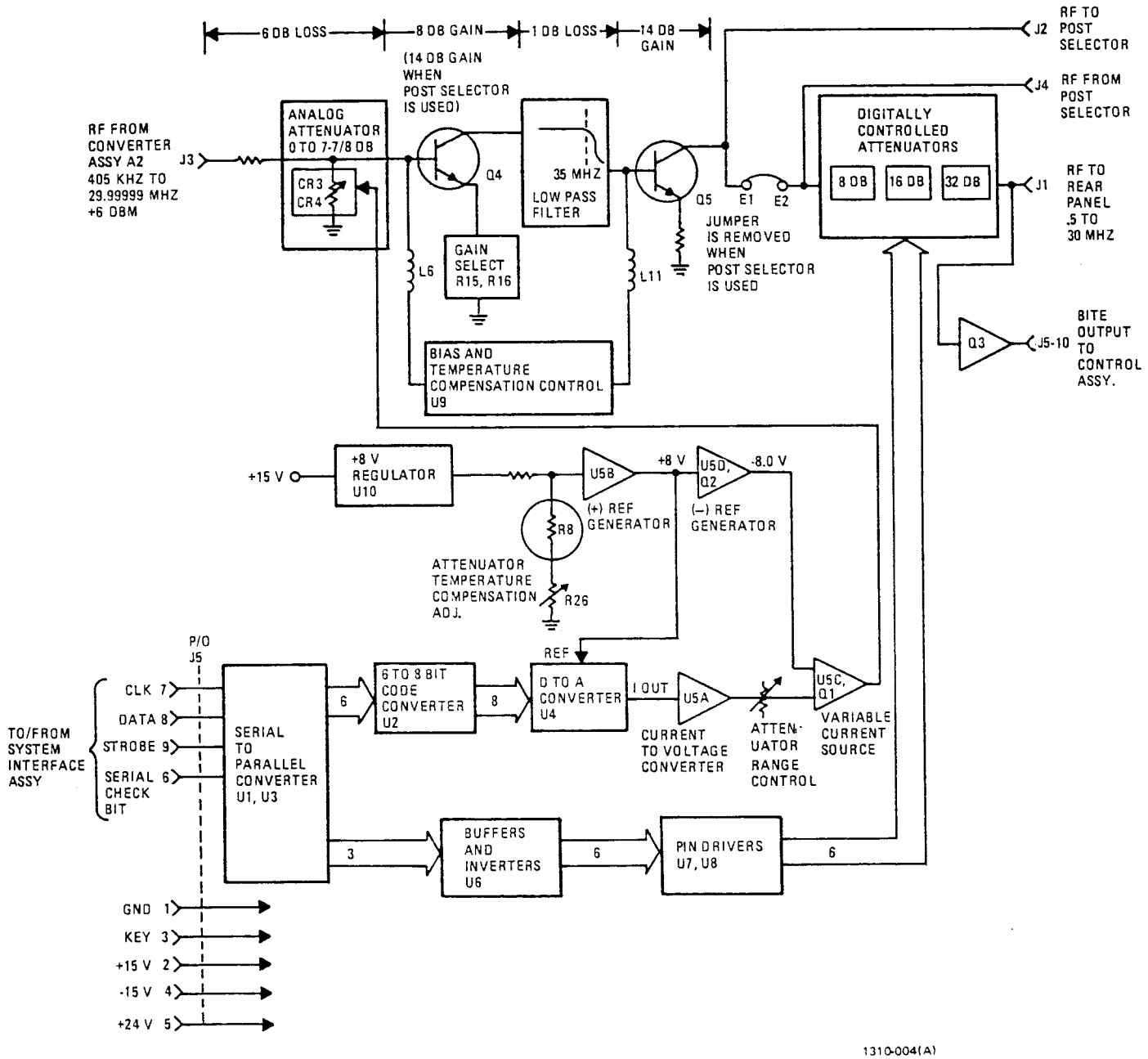
A1
OUTPUT AMPLIFIER ASSEMBLY



1310-004(A)

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OUTPUT AMPLIFIER ASSEMBLY A1

1. GENERAL DESCRIPTION

The Output Amplifier is a single PWB assembly; its position is shown in figure 1. This assembly amplifies the +6 dBm RF signal generated by Converter Assembly A2 and controls the exciter output power level. A two-stage amplifier can boost the 405 kHz to 29.99999 MHz RF signal up to 400 mW in high-gain mode. A lowpass filter is located between the two stages to attenuate noise and spurious emissions above 35 MHz.

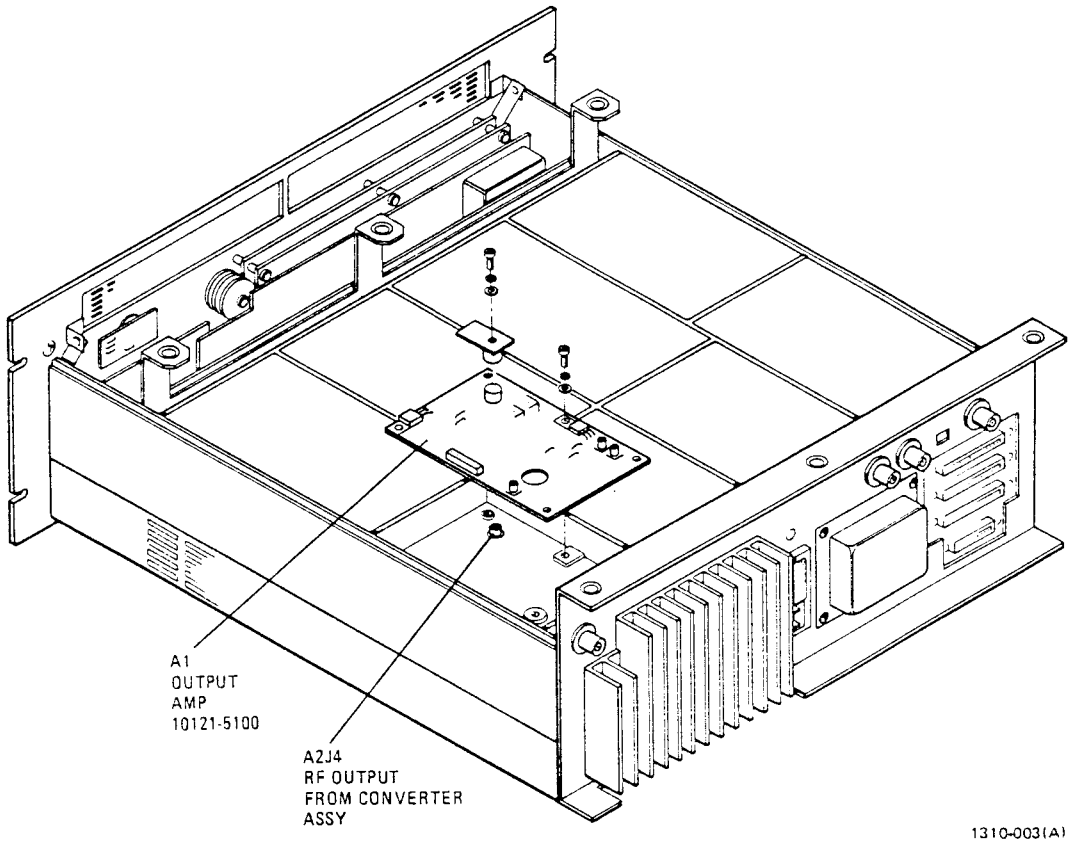


Figure 1. Output Amplifier Assembly A1 Location

Two attenuator circuits provide precise output power level control over a 63-7/8 dB range. An analog controlled attenuator can reduce the level of the incoming RF signal by 0 to 7-7/8 dB in 1/8 steps before it is introduced to the first amplifier stage. The second attenuator is digitally controlled and can reduce the level of the outgoing signal by up to 56 dB. Both attenuators are controlled by a serial data stream sent from the System Interface Assembly. The attenuator control signals are decoded and administered by digital and analog ICs.

The power control on the exciter front panel can adjust the power output over a 50 dB range in 1 dB steps. The A1 assembly can also provide automatic PA output power control in systems that have PA to exciter feedback lines.

The overall gain of the Output Amplifier Assembly can be preset to compensate for differences in system configuration. When a postselector is used, a jumper connecting E1 to E2 is removed and the gain of Q4 is set at 14 dB. For systems not using a postselector, the gain of Q4 is set at 8 dB and E1 is connected to E2.

Q3 is a driver that supplies a sample of the output signal to the exciter meter circuits and BITE circuit.

The A1 assembly mounts directly on the exciter chassis. The assembly is secured to the chassis by four mounting screws. A fifth screw secures Q5 and its mounting hardware to a heatsink built into the exciter chassis.

WARNING

Do not operate the A1 assembly unless Q5 is properly installed with a heatsink pad and insulating shoulder washer. It must be secured to the chassis or other appropriate heatsink.

A1J3 is located on the underside of the PWB. The connector cannot be accessed unless the A1 or A2 assembly is removed.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. Output Amplifier Assembly A1 Interface Connections

Connector	Function	Characteristics
J1	RF Output	0.5 to 30 MHz, + 20 dBm, 50 ohms
J2	Post Selector Input	0.5 to 30 MHz, + 27 dBm, 50 ohms when postselector is used
J3	RF Input	0.5 to 30 MHz, + 6 dBm, 50 ohms (nominally)
J4	Post Selector Output	0.5 to 30 MHz, + 21 dBm, 50 ohms when postselector is used
J5-1	Ground	
J5-2	Power	+ 15 Vdc, 270 mA (High Gain)/220 mA (Low Gain)
J5-3	Index Key	
J5-4	Power	-15 Vdc, 60 mA (High or Low Gain)
J5-5	Power	+ 24 V: 250 mA (High Gain); 190 mA (Low Gain)
J5-6	Serial Check Bit	P/O BITE Test, 5 Vdc = 'OK'
J5-7	Clock	TTL
J5-8	Data	Serial TTL, 0 Vdc = attenuation requested
J5-9	Strobe	+ pulse, (0 to 5 V transition) = strobe data
J5-10	BITE Output	Approximately 1 Vdc for 100 mW output

3. CIRCUIT DESCRIPTIONS

3.1 RF Signal Path

Paragraph 3.1.1 will detail circuit operation assuming that the postselector option is not installed (ie, low-gain mode is selected). Paragraph 3.1.2 will point out the differences when a postselector option is installed (high-gain mode). Note 6 of the schematic lists the circuit configurations which are applicable to the different gain modes. These configurations are preset at the factory.

3.1.1 Low Gain Mode

The A2 assembly provides + 6 dBm (into 50 ohms) at J3 from 405 kHz to 29.99999 MHz. The Analog Controlled Attenuator (ACA) network comprised of R11, R10, R12, L2, CR3, and CR4 has approximately 6 dB of initial insertion loss. PIN diodes CR3 and CR4 function as variable resistance elements, providing from 0 to 7-7/8 dB additional attenuation to the RF signal. The additional attenuation is dependent on the amount of control current supplied by Q1. (See paragraph 3.2.)

At a 0 dB ACA attenuator setting, a level of approximately 0 dBm is supplied to Q4. The low-gain configuration of Q4 provides 8 dB of gain, and the amplified signal is then applied to the low pass filter (LPF).

The LPF typically provides 50 dB of rejection to frequencies above 40 MHz in order to further reduce any high frequency spurious emissions. The LPF typically has 1 dB of insertion loss.

The LPF output is applied to Q5, which provides about 14 dB of signal amplification. The signal is then supplied to the discrete 8, 16, and 32 dB digitally controlled attenuator (DCA) networks.

The optimum bias points and collector currents for Q4 and Q5 are maintained by U9 and associated components. (Figure 2 shows an equivalent circuit.) Q4 and Q5 collector currents are 90 mA and 180 mA, respectively.

With the ACA set to 0 dB, approximately + 21 dBm is applied to the input of the DCA networks. Insertion loss of all three cascaded DCA networks is 1 dB, when none are selected. The nominal exciter power output is + 20 dBm (100 mW). Each DCA is configured as either a T- or pi- resistive pad which is switched in or out of the RF signal path by PIN diode switches. Figure 3 shows an equivalent RF circuit, in which the 16 dB DCA is the only one which has been selected. The drive current to the various PIN diode switches is supplied from drivers U7 and U8. (See paragraph 3.2.)

BITE amplifier and detector stage Q3 monitors the RF output signal level, and produces a dc output voltage proportional to this level. C51 and C52 sample the signal, Q3 amplifies it, and CR13, CR14, C37, and R43 convert it to a dc level. This BITE level is monitored by the Control Board Assembly whenever the operator chooses to perform a BITE test. At that time, a CW signal is fed through preceding signal chain assemblies and a + 6 dBm signal at the exciter's tuned frequency is presented at J3. All attenuators are set to 0 dB, and therefore the full 100 mW of output level will appear at J1. The BITE detector output will be approximately 1 Vdc for this output level under normal conditions. The Control Board Assembly will recognize this level as being valid, and will proceed in its testing. If the BITE level is significantly different, indicating a possible A1 fault, the appropriate fault code will appear on the exciter front panel.

The BITE output is also routed to the front panel meter, for use as the meter's drive signal indicating exciter output power.

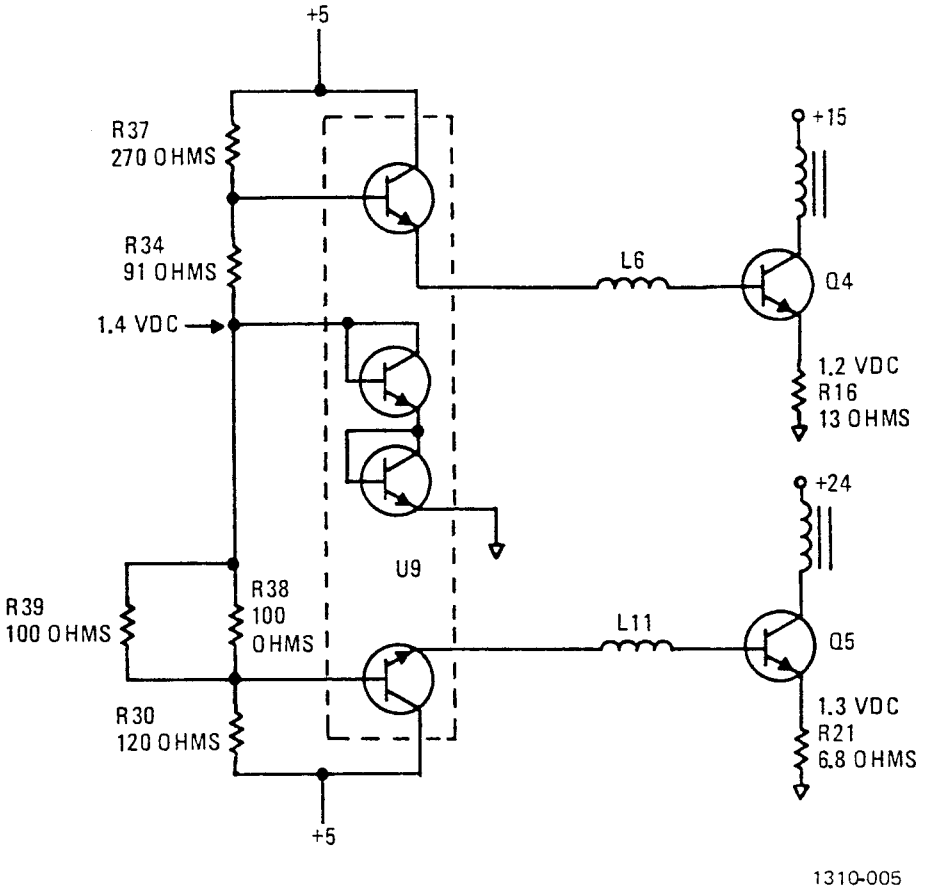


Figure 2. Q4, Q5 Equivalent Bias Circuit Low Gain Mode

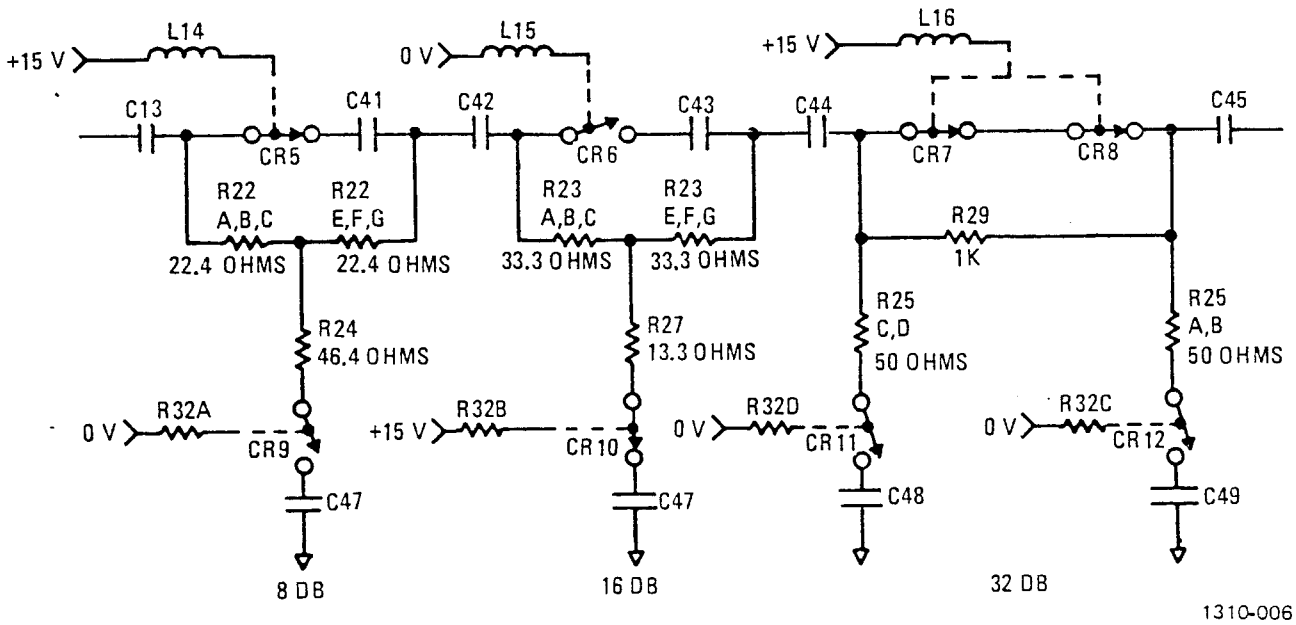


Figure 3. Digital Controlled Attenuator Equivalent Circuit

3.1.2 High Gain Mode

Exciter operation with an internal postselector option requires that the Output Amplifier Assembly gain be increased by about 6 dB to compensate for a nominal insertion loss of that option.

All circuits function as described in paragraph 3.1.1 with the following exceptions:

a. The Q4 amplifier gain is 14 dB instead of 8 dB.

b. Both Q4 and Q5 collector currents are increased to 150 mA and 250 mA respectively to accommodate the higher signal levels involved.

c. The signal path is broken at E1-E2, and the postselector is inserted in line at J2-J4.

3.2 ATTENUATION CONTROL CIRCUITRY

Data concerning the attenuation values desired are supplied from System Interface Assembly A18. Updating of the attenuator values occurs only when a change is to be made; it is not a continuous function. The System Interface Assembly receives its commands via the system PA feedback lines and/or the operator's use of the front panel power control button.

Data received at J3 pin 8 is a nine-bit data stream (MSB first) which is clocked into a serial-to-parallel converter circuit comprised of U1 and U3. All bits are clocked into and through U1 on positive clock transistions, but the outputs will not change until a strobe pulse is present. After the first eight clock pulses, the MSB is applied to U3-D1 input via U1-QS output. The ninth clock pulse places the MSB at U3-Q1 output and U3-D2 input. After the ninth clock pulse, the strobe line goes high, and the 1/8 dB bit through the 16 dB bit appears at U1-Q1 through Q8. The 32 dB bit appears at U3-Q2. The strobe line then goes low, disabling any further changes. Note that a '0' at the data input is interpreted as a request to select attenuation and a '1' as a request to remove attenuation.

U1-Q7, Q8, and U3-Q2 contain the 8, 16, and 32 dB bits, respectively. These bits are applied through signal buffer/inverter U6 to PIN diode drivers U7 and U8. The table on sheet 2 of the schematic lists the three DCA states as a function of U6 inputs. U7 and U8 provide the appropriate dc voltage levels to reverse bias the diodes and turn them off, and the necessary forward bias current to provide a low resistance to the RF signal when they are on.

U1-Q1 through Q6 outputs are applied to PROM decoder U2. U2 converts the six-bit word into an eight-bit word for digital to analog (D/A) converter U4. The binary data represents ACA values of 1/8, 1/4, 1/2, 1, 2, or 4 dB or sums of 2 or more values. U4, in turn, generates a proportional current for PIN diodes CR3 and CR4 to produce the attenuation requested. Operational amplifier U5A then converts this current into a voltage level. U5A output voltage can be determined according to the following formula:

$$V_{out}\,(U5A) = (-V_{ref}) \times \frac{\text{decimal value of binary word at U4-B1 through B8}}{256}$$

For example, if Vref = 8.0 Vdc and U2 output at U4 B1-B8 is:

B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8
1	0	1	1	0	1	1	1
MSB							LSB

Then: $10110111_2 = (128 + 32 + 16 + 4 + 2 + 1)_{10} = 183_{10}$

and V_{out} = -(8.0 Vdc) x $\frac{183}{256}$ = -5.718 Vdc

V_{ref} (+) is derived from voltage regulator U10, and is processed by (+) reference amplifier stage U5B to be nominally + 8.0 Vdc at U5B output. This voltage is used as the reference voltage for D/A converter U4. It is also applied to op amp U5D to generate a second reference voltage V_{ref}(-), which is equal in value to V_{ref}(+) but opposite in polarity.

U5A output ranges from V_{ref}(-) to 0 Vdc and is applied to one side of analog attenuation range adjust R7. The other side of R7 is connected to V_{ref}(-). A voltage will therefore be developed across R7 which is a function of the desired attenuation step requested. R7 scales this voltage and applies it to a precision current source comprised of U5C and Q1, which in turn supplies control current to PIN diodes CR3 and CR4. The resistance of CR3 and CR4 decreases, ie, attenuation increases, as the current through them is increased. R7 is factory adjusted to set the current range required by CR3 and CR4 corresponding to an analog attenuation range of 0 to 7-7/8 dB.

Analog Attenuation Control temperature compensation is provided by thermistor R8 and Analog Attenuation Compensation Control Adjust R26. This compensation network tracks and cancels the temperature induced effects due to PIN diodes CR3 and CR4. As the diodes ambient temperature increases, their attenuation value decreases. R8, however, will increase V_{ref}, which causes a larger voltage across R7 to develop. This results in a larger voltage drop across R5 so Q1 conducts more current through CR3 and CR4. When this happens, the diode's attenuation value increases back to the desired level. R26 is factory set to change the sensitivity of the temperature compensation, thereby tailoring the degree of compensation to any given diodes.

4. MAINTENANCE

The following adjustments should not be performed as routine maintenance procedures, but only when a PWB failure and subsequent repair indicates a definite need to realign the assembly outside the factory. (Note that all PWBs are purchased factory aligned.) The following assumptions are made:

a. The assembly is securely fastened to a chassis or similar test fixture; in particular Q5 is properly connected to a heatsink.

b. The assembly is configured for either low or high gain mode, per instructions on schematic diagram, figure 9. (Note that if high-gain mode is selected, a 50 ohm, 6 dB pad should be inserted in-line between J2 and J4 to simulate the insertion loss introduced by a postselector).

c. Figure 4 shows the circuit used to supply RF input power.

d. A serial data generator (SDG) test fixture or an analog attenuator switching network is available. If a serial data generator is not available, an analog attenuator switching network (AASN) may be fabricated (figure 5) and used in its place.

4.1 Analog Attenuator Adjustments

a. Set signal source output level to + 6 dBm (into 50 ohms) at 30 MHz.

b. Set R7 (Analog Attenuation Range Adjust) and R26 (Analog Attenuator Temperature Compensation Adjust) fully clockwise (cw).

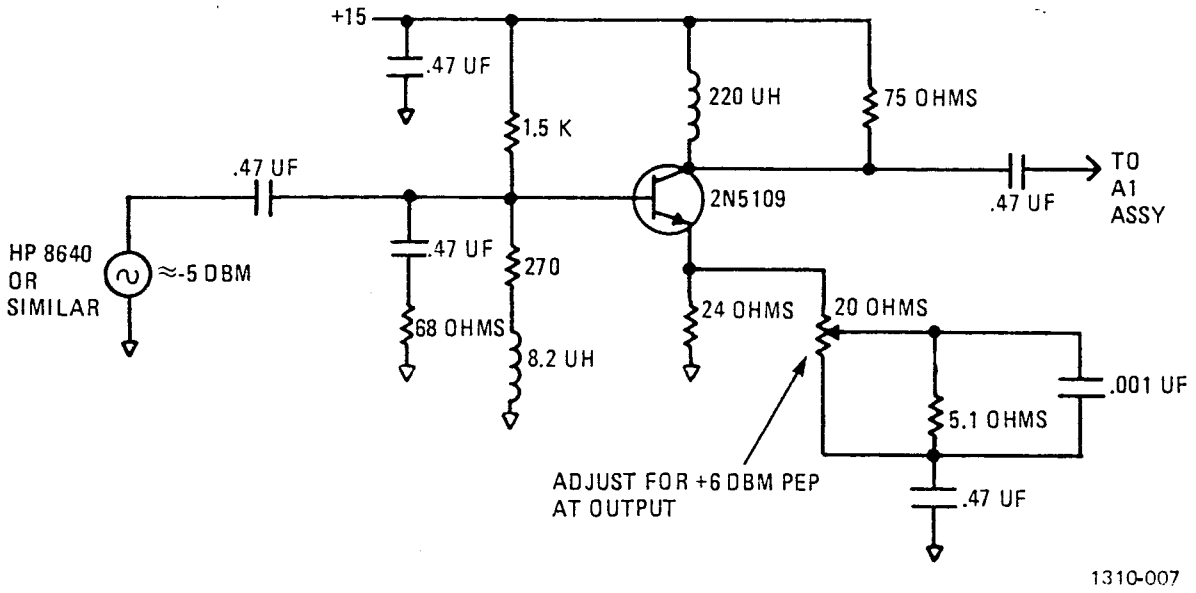


Figure 4. RF Signal Source

CAUTION

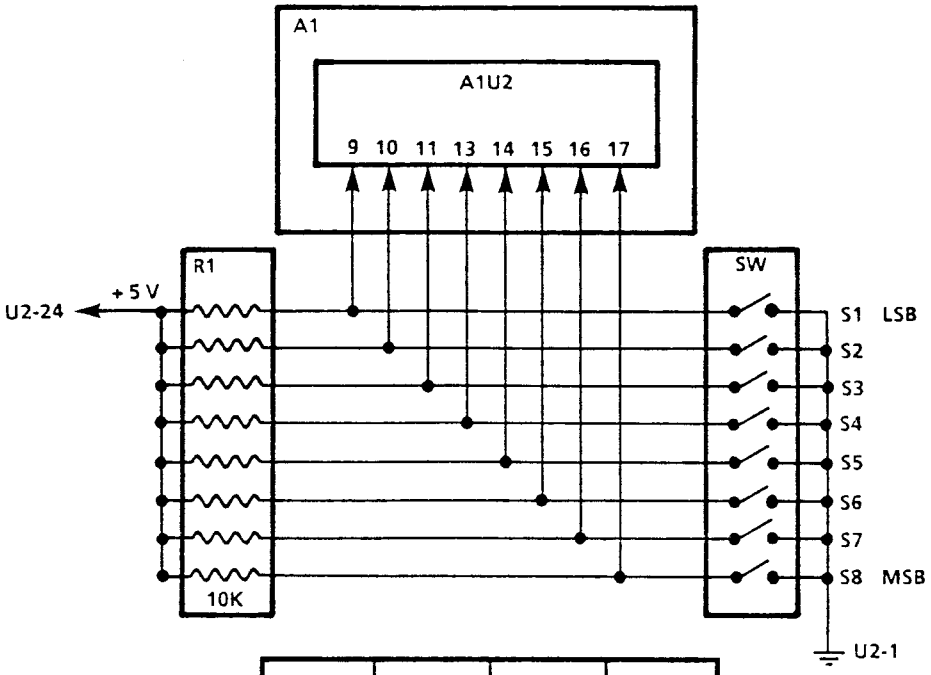
A1U2 is a static sensitive device. Precautionary measures must be taken to protect the device from static damage prior to performing the next step.

c. If a serial data generator is available, connect equipment as shown in figure 6. If an analog attenuator switching network (AASN) is to be used, and assuming that it has been fabricated per figure 5, carefully remove A1U2 from its socket. Refer to figure 7. Connect the AASN to the appropriate pins of the U2 socket as shown and connect the remaining test equipment. Allow the A1 assembly to operate for three minutes before proceeding.

d. Set serial data generator (SDG) or AASN to 0 dBm attenuation. Output level should be approximately +21 to +25 dBm.

e. Set SDG or AASN to 7-7/8 dB attenuation. Adjust R7 counterclockwise (ccw) for 11.5 dBm ± 0.05 dB. (Use RF voltmeter 10 dBm range for all readings around 11.5 dBm.)

f. Set SDG or AASN to 0 dB attenuation. Readjust signal source input level to obtain +20 dBm ± 0.05 dB at output.



SW	0 dB	4 dB	7 7/8 dB
LSB S1	C	O	O
S2	O	O	C
S3	C	C	C
S4	C	C	O
S5	O	C	C
S6	O	C	O
S7	O	O	O
MSB S8	O	O	C

C = SWITCH POSITION CLOSED
O = SWITCH POSITION OPEN

PARTS REQUIRED FOR MANUFACTURE OF ANALOG ATTENUATOR SWITCHING NETWORK

QTY.	DESIG.	DESCRIPTION	HARRIS Part No.
1	SW	Switch, 8 Section, SPST DIP (or equivalent)	S50-0001-008
1	R1	Resistor, 10K 10SIP (or equivalent)	R50-0010-103

1310-120

Figure 5. Analog Attenuator Switching Network Fabrication Information

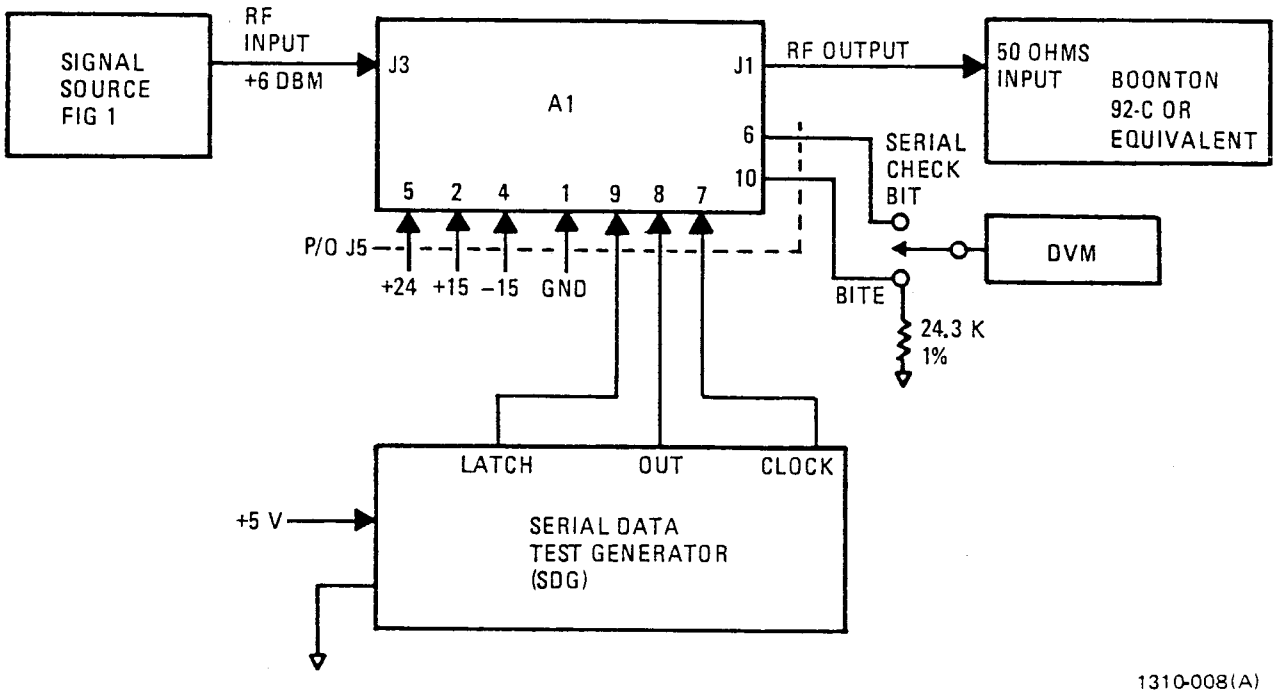


Figure 6. Output Amplifier Assembly Test Setup with a Serial Data test Generator (SDG)

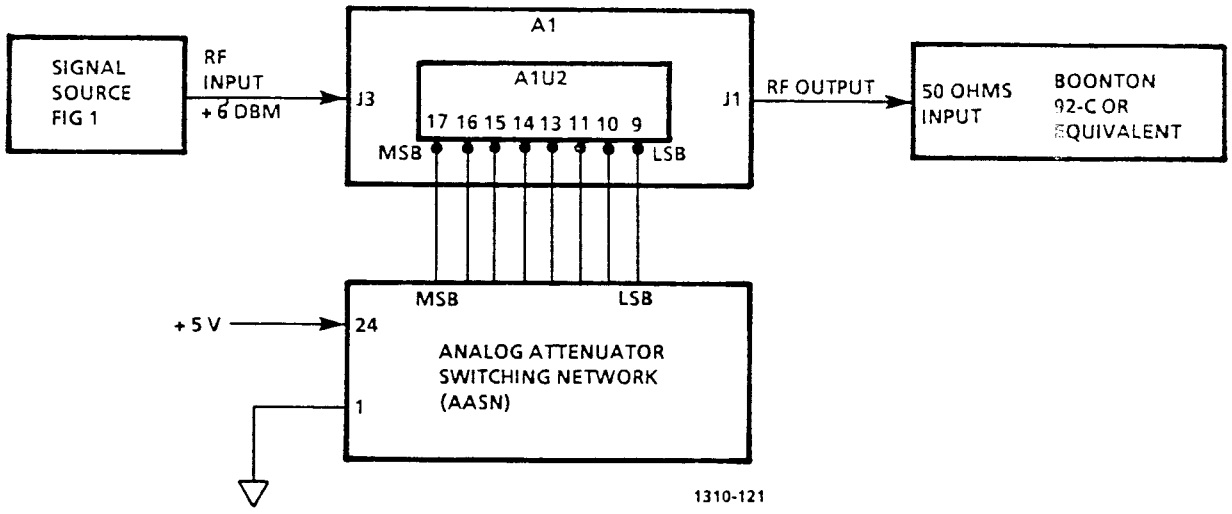


Figure 7. Alternate Output Amplifier Assembly test setup with an Analog Attenuator Switching Network (AASN)

g. Repeat steps e and f until:

1. The RF output is + 20 dBm ± 0.05 dB at 0 dB SDG or AASN setting.

and

2. The RF output is + 11.5 dBm ± 0.05 dB at 7-7/8 dB SDG or AASN setting.

h. Set SDG or AASN to 7-7/8 dB attenuation. Apply a forced-air heat source to the general area around which CR3, CR4, and thermistor R8 are located. Using a thermocoupled DVM (Fluke 2176A or equivalent), monitor the area and warm to approximately 60° C (near their surface) for at least 1 minute. (Note that steps i-l require that these components be maintained at the 60° C ambient temperature).

i. Adjust R26 to return the RF output level to 11.5 dBm.

j. Set the SDG or AASN to 0 dB attenuation. Readjust signal source input level to maintain + 20 dBm ± .05 dB RF output.

k. Set the SDG or AASN to 7-7/8 dB attenuation. Adjust R26 to return the RF output level to 11.5 dBm.

l. Repeat steps j and k until:

1. The RF output is + 20 dBm ± .05 dB at 0 dB SDG or AASN setting.

2. The RF output is 11.5 dBm ± .1 dB at 7-7/8 dB SDG or AASN setting.

m. Verify frequency response as follows:

1. Set signal source to + 6 dBm (into 50 ohm) at 30 MHz.

2. Set SDG or AASN to 0 dB, note level. Verify RF output is + 20 dBm (+ 2, -1 dBm).

3. Set SDG or AASN to 4 dB. Verify RF output is in the range of 4 to 5.25 dB below level noted in 2.

4. Set SDG or AASN to 7-7/8 dB. Verify RF output is in the range of 8.1 to 10 dB below level noted in 2.

5. Repeat steps 1-4 at 10 and .5 MHz.

n. Test is completed.

4.2 Digital Attenuator Verification

a. If a serial data generator is to be used, connect equipment as shown in figure 6. If the AASN was used for the analog attenuator alignment, disconnect the AASN from the U2 socket and carefully reinsert A1U2. If an SDG is not available, the RF power level adjustment can be set on the front panel by pressing the RF POWER control and entering the desired attenuation via the keypad.

b. Set SDG to -8, and adjust R24 to obtain a + 12 dBm RF output level.

c. Set SDG to -16, and adjust R27 to obtain a + 4 dBm RF output level.

d. Set SDG to -32, and adjust R29 to obtain a -12 dBm RF output level.

e. Set signal source level to obtain a + 20 dBm RF output at 10 MHz.

f. Set SDG to -8, -16, then -32 dB. Verify that the output level falls to 12, 4, and -12 dBm (respectively), ± 5%.

g. Repeat steps e. and f. at 0.5 MHz.

h. Test is completed.

4.3 Bite Verification

NOTE

The AASN should not be connected for this test.

a. Connect equipment as shown in figure 5. Set SDG to 0 dB. If a serial data test generator (SDG) is not available, the 0 dBm setting can be set via the front panel RF power level adjustment. Set signal source to obtain + 20 dBm RF at 10 MHz.

b. Adjust R43 until the BITE output measures 1.2 Vdc.

c. Serial data test BITE should be 0. Set SDG to 1/8 dB. Serial data test BITE should now be + 5 Vdc.

NOTE

Serial data test BITE cannot be performed without an SDG. However, the serial data test BITE line is checked automatically when running the exciter BITE routine.

d. Test is completed.

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components of the A1 assembly are listed in table 2. Table 3 lists the parts substitutions for the 10121-5100-02, Output Amplifier Assembly A1 with optional postselector. Component Locations are shown in figure 8. The Output Amplifier circuit is shown in figure 9.

Table 2. Output Amplifier Assembly A1 Parts List

Ref. Desig.	Part Number	Description
A1	10121-5100-01	RF OUTPUT AMPLIFIER ASSEMBLY
C1	CM05ED270J03	CAP 27PF 5% 500V MICA
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	CM05FD161J03	CAP 160PF 5% 500V MICA
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	CK05BX271K	CAP 270PF 10% 200V CER
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	CK05BX220K	CAP 22PF 10% 200V CER
C9	M39014/02-1310	CAP .1UF 10% 100V CER-R

Table 2. Output Amplifier Assembly A1 Parts List (Cont.)

Ref. Desig.	Part Number	Description
C10	M39014/02-1320	CAP .47UF 10% 50V CER-R
C11	M39014/02-1320	CAP .47UF 10% 50V CER-R
C12	CK06BX103K	CAP .01UF 10% 200V CER
C13, C14	M39014/02-1320	CAP .47UF 10% 50V CER-R
C14	M39014/02-1320	CAP .47UF 10% 50V CER-R
C15	C26-0035-100	CAP 10UF 20% 35V TANT
C16	CM05ED750J03	CAP 75PF 5% 500V MICA
C17	C26-0025-100	CAP 10UF 20% 25V TANT
C18	M39014/02-1320	CAP .47UF 10% 50V CER-R
C19	M39014/02-1320	CAP .47UF 10% 50V CER-R
C20	M39014/02-1320	CAP .47UF 10% 50V CER-R
C21	CM05ED470J03	CAP 47PF 5% 500V MICA
C22	CM05ED620J03	CAP 62PF 5% 500V MICA
C23	CM05FD101J03	CAP 100PF 5% 500V MICA
C24	CM05ED820J03	CAP 82PF 5% 500V MICA
C25	CM05FD121J03	CAP 120PF 5% 500V MICA
C26	CM05CD150J03	CAP 15PF 5% 500V MICA
C27	CM05ED820J03	CAP 82PF 5% 500V MICA
C28	M39014/02-1310	CAP .1UF 10% 100V CER-R
C29	M39014/02-1310	CAP .1UF 10% 100V CER-R
C30	M39014/02-1320	CAP .47UF 10% 50V CER-R
C31	M39014/02-1320	CAP .47UF 10% 50V CER-R
C32	M39014/02-1320	CAP .47UF 10% 50V CER-R
C33	M39014/02-1320	CAP .47UF 10% 50V CER-R
C34	C26-0025-100	CAP 10UF 20% 25V TANT
C35	M39014/02-1310	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310	CAP .1UF 10% 100V CER-R
C37	CK06BX103K	CAP .01UF 10% 200V CER
C38	M39014/02-1320	CAP .47UF 10% 50V CER-R
C39	M39014/02-1320	CAP .47UF 10% 50V CER-R
C40	M39014/02-1320	CAP .47UF 10% 50V CER-R
C41	M39014/02-1320	CAP .47UF 10% 50V CER-R
C42	M39014/02-1320	CAP .47UF 10% 50V CER-R
C43	M39014/02-1320	CAP .47UF 10% 50V CER-R
C44	M39014/02-1320	CAP .47UF 10% 50V CER-R
C45	M39014/02-1320	CAP .47UF 10% 50V CER-R
C46	M39014/02-1320	CAP .47UF 10% 50V CER-R
C47	M39014/02-1320	CAP .47UF 10% 50V CER-R
C48	M39014/02-1320	CAP .47UF 10% 50V CER-R
C49	M39014/02-1320	CAP .47UF 10% 50V CER-R
C50	CK06BX103K	CAP .01UF 10% 200V CER
C51	CK05BX100K	CAP 10PF 10% 200V CER
C52	CK05BX220K	CAP 22PF 10% 200V CER
C53	CK06BX103K	CAP.01UF 10% 200V CER
C54	CK06BX103K	CAP .01UF 10% 200V CER
CR1	1N6263	DIODE .40W 60V HOT CARR
CR2	1N4454	DIODE 200MA 75V SW

Table 2. Output Amplifier Assembly A1 Parts List (Cont.)

Ref. Desig.	Part Number	Description
CR3	D12-0007-001	DIODE 1W 75V PIN SW
CR4	D12-0007-001	DIODE 1W 75V PIN SW
CR5	D12-0008-001	DIODE 2.5W 1200V PIN SW
CR6	D12-0008-001	DIODE 2.5W 1200V PIN SW
CR7	D12-0008-001	DIODE 2.5W 1200V PIN SW
CR8	D12-0008-001	DIODE 2.5W 1200V PIN SW
CR9	D12-0008-001	DIODE 2.5W 1200V PIN SW
CR10	D12-0008-001	DIODE 2.5W 1200V PIN SW
CR11	D12-0008-001	DIODE 2.5W 1200V PIN SW
CR12	D12-0008-001	DIODE 2.5W 1200V PIN SW
CR13	1N6263	DIODE .40W 60V HOT CARR
CR14	1N6263	DIODE .40W 60V HOT CARR
E3	L50-0001-003	FERRITE BEAD
J1	J-0031	CONN SMB VERT PCB
J2	J-0031	CONN SMB VERT PCB
J3	J90-0014-001	CONN SMB VERT PCB MT M
J4	J-0031	CONN SMB VERT PCB
J5	J46-0032-010	HEADER, 10 PIN DISCRETE
L1	MS75085-16	COIL 560UH 10% FXD RF
L2	MS75083-11	COIL .68UH 10% FXD RF
L3	L08-0001-001	CHOKE W B 50 MHZ
L4	MS75083-1	COIL .10UH 10% FXD RF
L5	10121-5104	INDUCTOR
L6	MS75085-16	COIL 560UH 10% FXD RF
L7	10121-7001	INDUCTOR .181UH
L8	10121-7002	INDUCTOR .174UH
L9	10121-7003	INDUCTOR .279UH
L10	L08-0001-001	CHOKE W B 50 MHZ
L11	MS75085-16	COIL 560UH 10% FXD RF
L12	MS75083-5	COIL .22UH 10% FXD RF
L13	10121-5105	INDUCTOR
L14	MS75085-16	COIL 560UH 10% FXD RF
L15	MS75085-16	COIL 560UH 10% FXD RF
L16	MS75085-16	COIL 560UH 10% FXD RF
L17	MS75085-16	COIL 560UH 10% FXD RF
L18	MS75085-16	COIL 560UH 10% FXD RF
L19	MS75085-16	COIL 560UH 10% FXD RF
L20	MS75084-6	COIL 3.3UH 10% FXD RF
L21	L08-0001-001	CHOKE W B 50 MHZ
Q1	2N2222A	XSTR SS/GP NPN TO-18
Q2	2N2907A	XSTR SS/GP PNP TO-18
Q3	Q35-0003-000	XSTR U310 JFET HIGH GM
Q4	Q25-0014-000	XSTR RFPWR
Q5	Q25-0016-000	XSTR RFPWR
R1	RN55D2001F	RES,2000 1% 1/8W MET FLM

Table 2. Output Amplifier Assembly A1 Parts List (Cont.)

Ref. Desig.	Part Number	Description
R2	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R3	R65-0003-221	RES,220 5% 1/4W CAR FILM
R4	R65-0003-222	RES,2.2K 5% 1/4W CAR FILM
R5	RN55D1000F	RES,100.0 1% 1/8W MET FLM
R6	R65-0003-222	RES,2.2K 5% 1/4W CAR FILM
R7	R30-0008-502	RES,VAR,PCB 5K 1/2W 10%
R8	D40-0004-004	THERM,2K, 5%
R9	R53-0002-103	RES NETWORK 14 PIN 10K
R10	R65-0003-309	RES,3.0 5% 1/4W CAR FILM
R11	RN55D30R1F	RES,30.1 1% 1/8W MET FLM
R12	R65-0003-309	RES,3.0 5% 1/4W CAR FILM
R13	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R16	R65-0003-130	RES,13 5% 1/4W CAR FILM
R17	R65-0003-750	RES,75 5% 1/4W CAR FILM
R18	R65-0003-430	RES,43 5% 1/4W CAR FILM
R19	R65-0003-101	RES,100 5% 1/4W CAR FILM
R20	R65-0003-331	RES,330 5% 1/4W CAR FILM
R21	RCR32G6R8JM	RES,6.8 5% 1W CAR COMP
R22	R50-0008-680	RES,8 SIP, 68,2.0%, 7RES
R23	R50-0008-101	RES,8 SIP, 100,2.0%, 7RES
R24	R30-0008-001	RES,POT,MULTI-TURN,100 OHMS,10%,1/2W
R25	R51-0008-101	RES, FXD, SIP, 100
R26	R30-0008-104	RES,VAR,PCB 100K 1/2W 10%
R27	R30-0008-500	RES,POT,MULTI-TURN,50 OHMS,20%,1/2W
R28	R65-0003-100	RES,10 5% 1/4W CAR FILM
R29	R30-0008-202	RES,POT,MULTI-TURN,2.0K OHMS,10%,1/2W
R30	R65-0003-121	RES,120 5% 1/4W CAR FILM
R31	R51-0006-330	RES, FXD, SIP, 33
R32	R51-0008-151	RES, FXD, SIP, 33
R33	R50-0006-104	RES,6 SIP,100K,2.0%, 5RES
R34	R65-0003-910	RES,91 5% 1/4W CAR FILM
R35	R50-0006-202	RES,6 SIP, 2K,2.0%, 5RES
R36	R50-0006-202	RES,6 SIP, 2K,2.0%, 5RES
R37	R65-0003-271	RES,270 5% 1/4W CAR FILM
R38	R65-0003-101	RES,100 5% 1/4W CAR FILM
R40	R65-0003-105	RES,1.0M 5% 1/4W CAR FILM
R41	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R42	R65-0003-221	RES,220 5% 1/4W CAR FILM
R43	R30-0008-503	RES,VAR,PCB 50K 1/2W 10%
U1	I01-0000-156	IC 4094B PLASTIC CMOS
U2	SEE NOTE	SOFTWARE KIT
U3	I01-0000-050	IC 4013B PLASTIC CMOS
U4	I03-0012-000	IC AD7523 PLASTIC CMOS
U5	I30-0003-000	IC 324 OP AMP PLASTIC
U6	I01-0000-018	IC 4049UB PLASTIC CMOS

Table 2. Output Amplifier Assembly A1 Parts List (Cont.)

Ref. Desig.	Part Number	Description
U7	135-0009-000	IC 75365 PLASTIC TTL
U8	135-0009-000	IC 75365 PLASTIC TTL
U9	190-0001-000	IC CA3083 XSTR ARRAY
U10	112-0006-008	IC VR 78L08A +8V .10A 4%
U11	111-0001-001	IC VR 7805 +5V 1.5A 4%
XU2	J77-0008-005	SKT IC MACH 24 PIN

NOTE

The part number for U2 is 10121-8XXX-X where XXX-X is the four-character software kit code found on the PROM label. For example, if the code is 501C, the part number for the programmed PROM is 10121-8501C.

Table 3. Output Amplifier Assembly A1 (10121-5100-02) Parts Substitutions

Ref. Desig.	Part Number	Description
R14	R65-0003-430	RES, 43 OHMS, 5%, 1/4 W, CAR FILM
R15	R65-0003-110	RES, 11 OHMS, 5%, 1/4 W, CAR FILM
R38		NOT USED
R39	R65-0003-241	RES, 240 OHMS, 5%, 1/4 W, CAR FILM

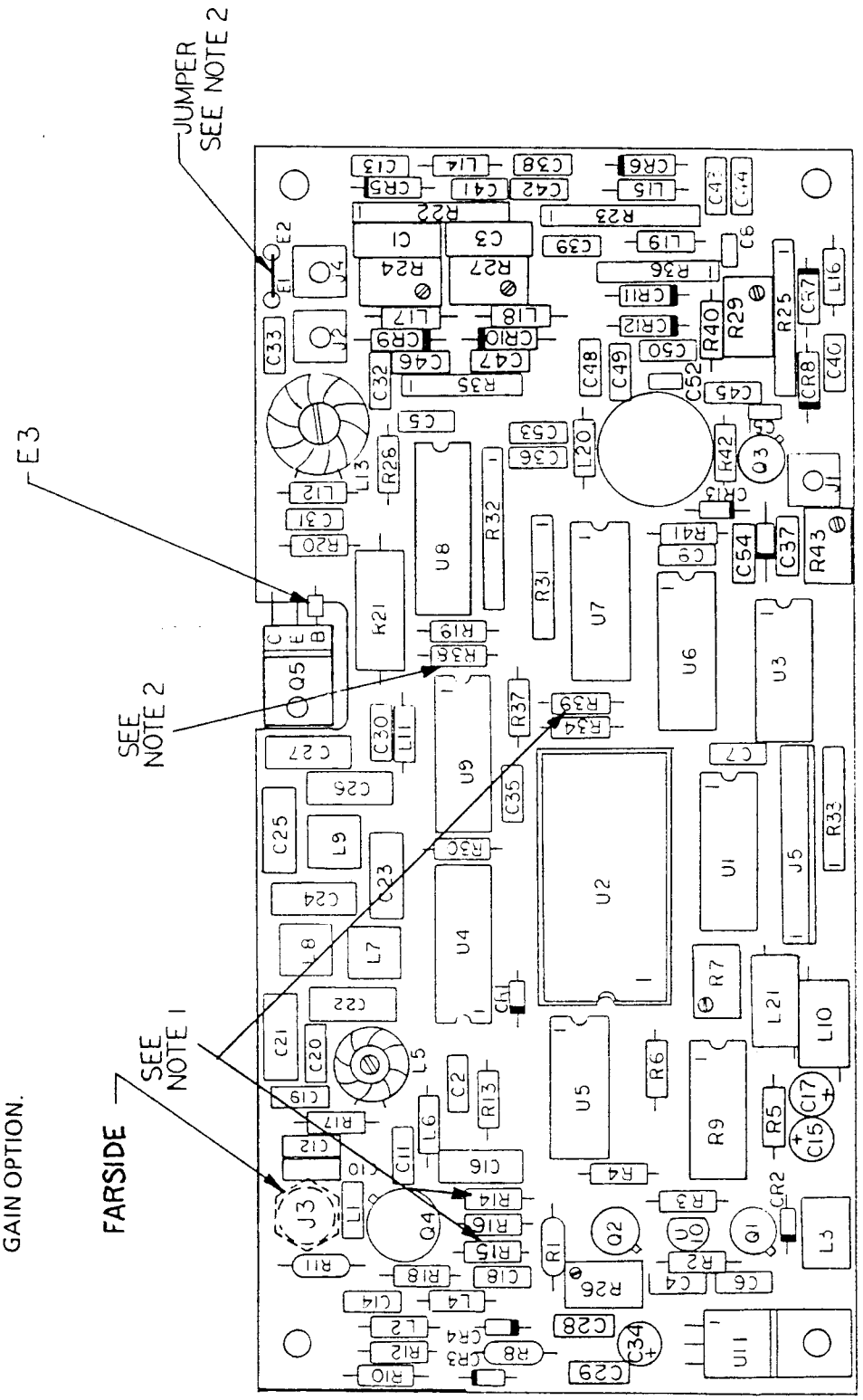


Figure 8. Output Amplifier Assembly A1 Component Location Diagram (10121-5100 Rev. F)

NOTES:

1. R14, R15 AND R39 ARE REMOVED FOR 10121-5100-02 LOW GAIN OPTION.

2. R38 AND E1 TO E2 JUMPER ARE REMOVED FOR 10121-5100-01 HIGH GAIN OPTION.

E: UNLESS OTHERWISE SPECIFIED:

RTIAL REFERENCE DESIGNATIONS ARE SHOWN.
R A COMPLETE DESIGNATION, PREFIX WITH
IT NO. AND/OR ASSEMBLY NO. DESIGNATION.

L RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.

L CAPACITOR VALUES ARE IN MICROFARADS.

L INDUCTOR VALUES ARE IN MICROHENRIES.

NDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY.
MPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

6.

	FOR ASSEMBLY 10121-5100-02 (WITH POST SELECTOR OPERATION)	FOR ASSEMBLY 10121-5100-01 (WITHOUT POST SELECTOR OPERATION)
R14	IN CIRCUIT	REMOVE
R15	IN CIRCUIT	REMOVE
R38	REMOVE	IN CIRCUIT
R39	IN CIRCUIT	REMOVE
E1-E2 JUMPER	REMOVE	IN CIRCUIT
J2	CONNECT TO POST SELECTOR INPUT	NOT USED
J4	CONNECT TO POST SELECTOR OUTPUT	NOT USED
Q4 GAIN	≈14 dB	≈8 dB

7. ALL VOLTAGES AND SIGNAL LEVELS SHOWN ARE NOMINAL VALUES.

RF INPU
.5-30MH
+6dB

INDEX KE

GN

+15

-15

+24

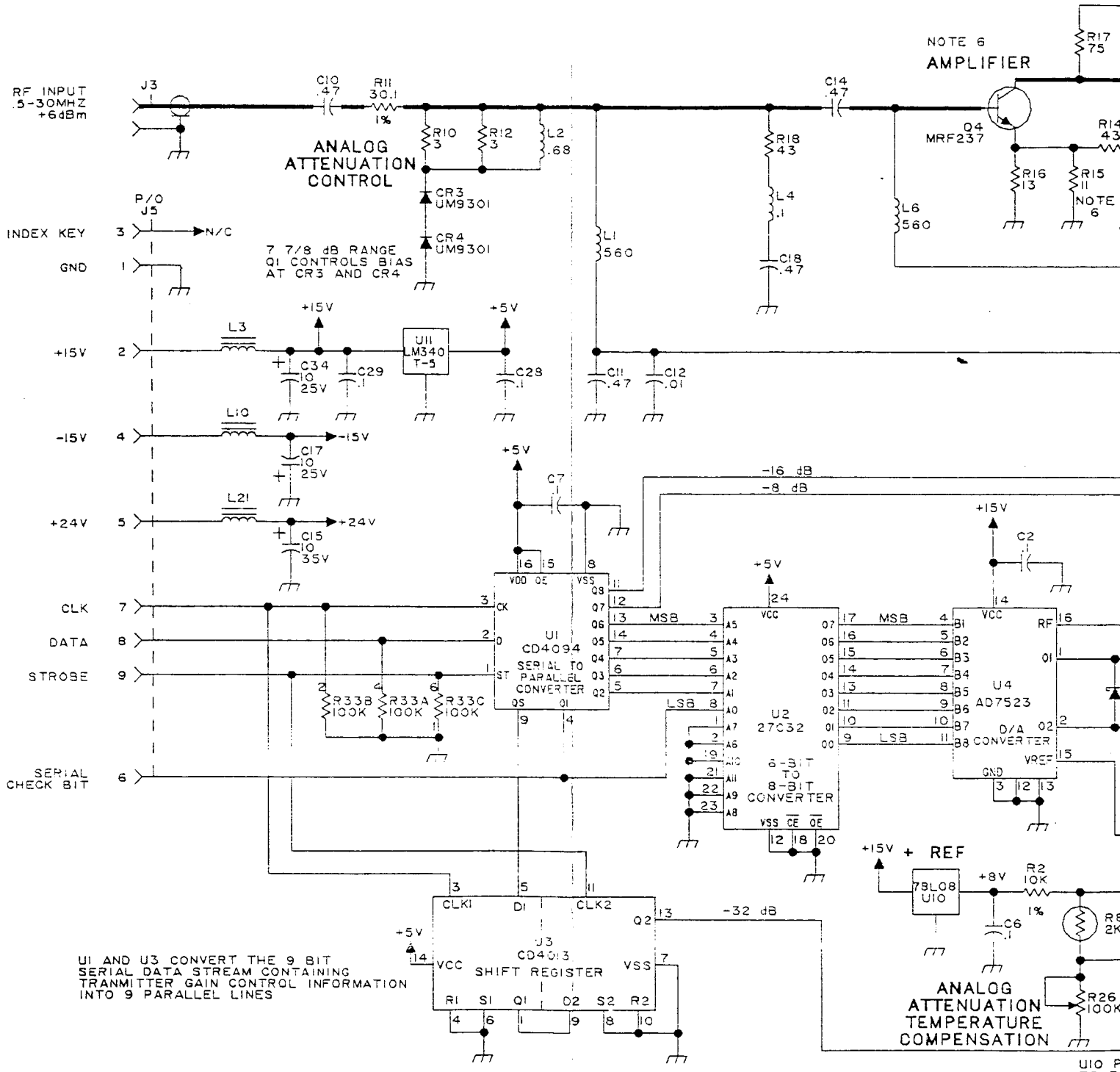
CL

DAT

STROBE

SERIAL
CHECK BIT

U
S
T
IN


RF INPUT
.5-30MHZ
+6dBm
J3
C10
.47
R11
30.1
1%
ANALOG
ATTENUATION
CONTROL
R10
3
R12
3
L2
.68
CR3
UM9301
CR4
UM9301
7 7/8 dB RANGE
Q1 CONTROLS BIAS
AT CR3 AND CR4
C14
.47
NOTE 6
AMPLIFIER
Q4
MRF237
R17
75
R14
43
R16
13
R15
11
NOTE
6
R18
43
L4
.1
C18
.47
L6
560
L1
560
P/O
J5
INDEX KEY
3
N/C
GND
1
+15V
2
L3
C34
10
25V
C29
.1
U11
LM340
T-5
C28
.1
+5V
C11
.47
C12
.01
-15V
4
L10
C17
10
25V
+24V
5
L21
C15
10
35V
-16 dB
-8 dB
C7
.1
CLK
7
DATA
8
STROBE
9
SERIAL
CHECK BIT
6
U1
CD4094
SERIAL TO
PARALLEL
CONVERTER
VDD OE VSS
CK
D
ST
Q8 Q7 Q6 Q5 Q4 Q3 Q2
QS QI
MSB
LSB
R33B
100K
R33A
100K
R33C
100K
U2
27C32
8-BIT
TO
8-BIT
CONVERTER
VCC
A5 A4 A3 A2 A1 A0 A7 A6 A10 A11 A9 A8
VSS CE OE
O7 O6 O5 O4 O3 O2 O1 O0
C2
.1
U4
AD7523
D/A
CONVERTER
B1 B2 B3 B4 B5 B6 B7 B8
RF
OI
O2
VREF
GND
U3
CD4013
SHIFT REGISTER
CLK1 DI CLK2
Q2
VCC VSS
RI SI QI D2 S2 R2
-32 dB
+15V + REF
78L08
U10
+8V
R2
10K
1%
C6
.1
R8
2K
R26
100K
ANALOG
ATTENUATION
TEMPERATURE
COMPENSATION
U1 AND U3 CONVERT THE 9 BIT
SERIAL DATA STREAM CONTAINING
TRANMITTER GAIN CONTROL INFORMATION
INTO 9 PARALLEL LINES

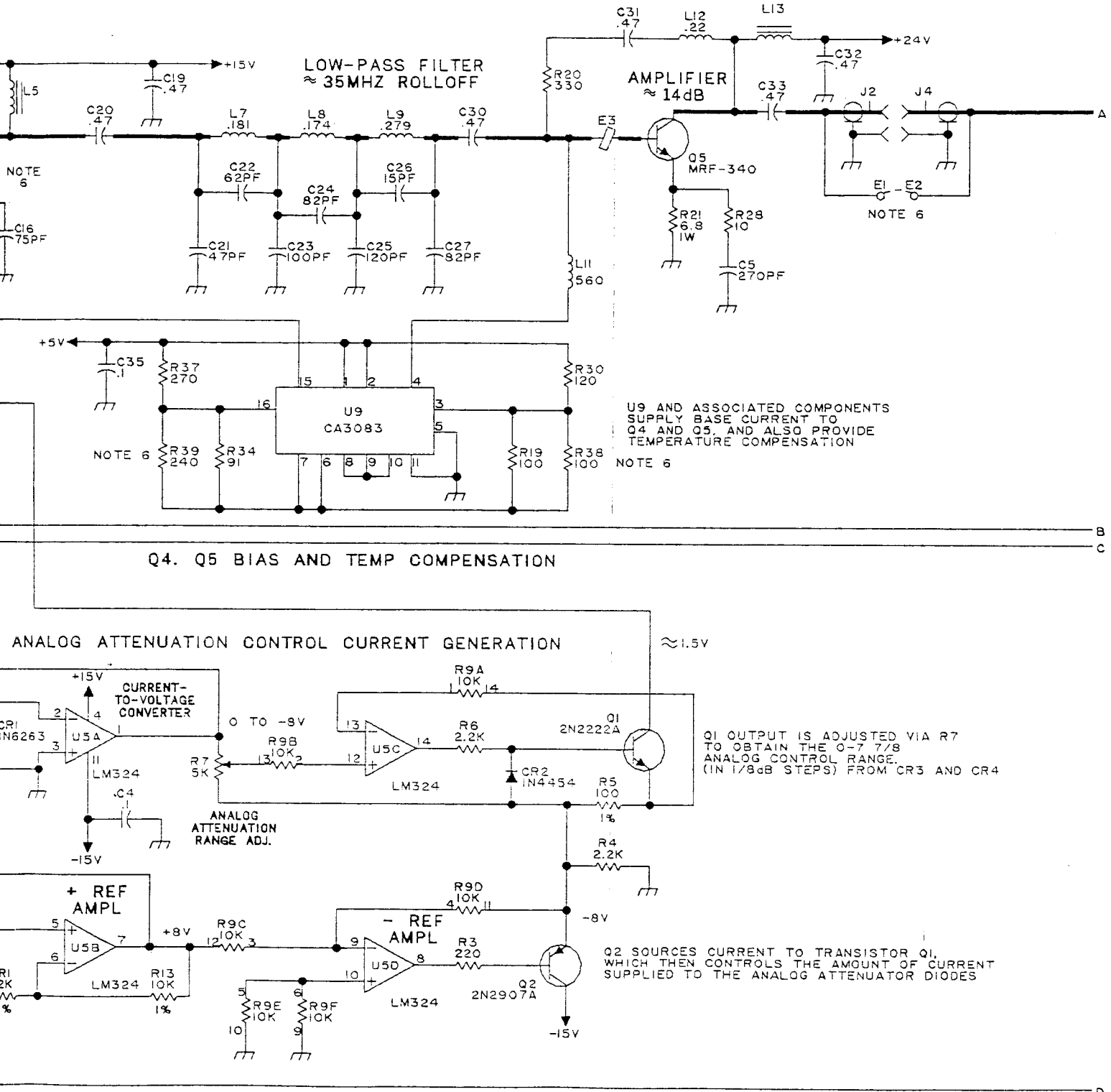
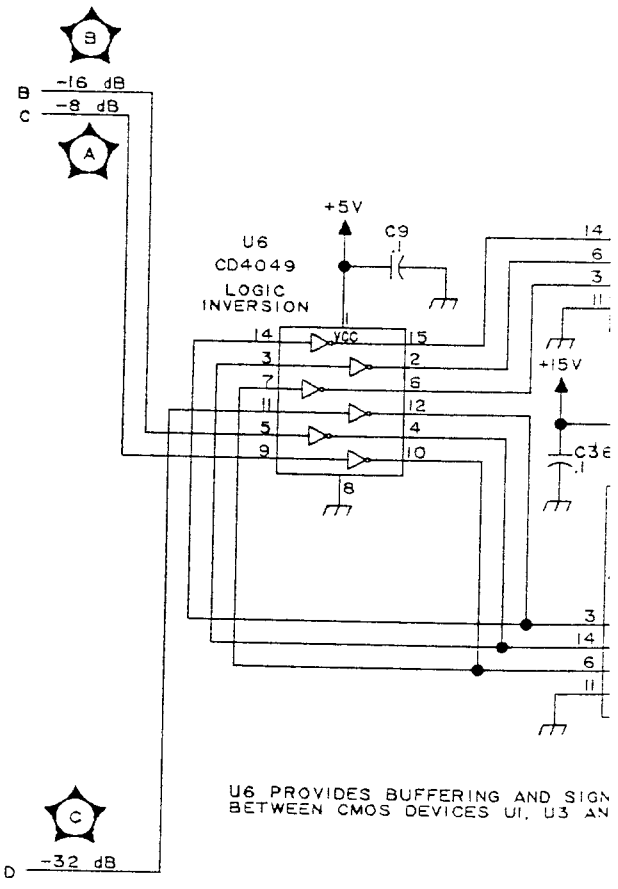


Figure 9. Output Amplifier Assembly A1 Schematic Diagram (10121-5101 Rev. D) (Sheet 1 of 2)

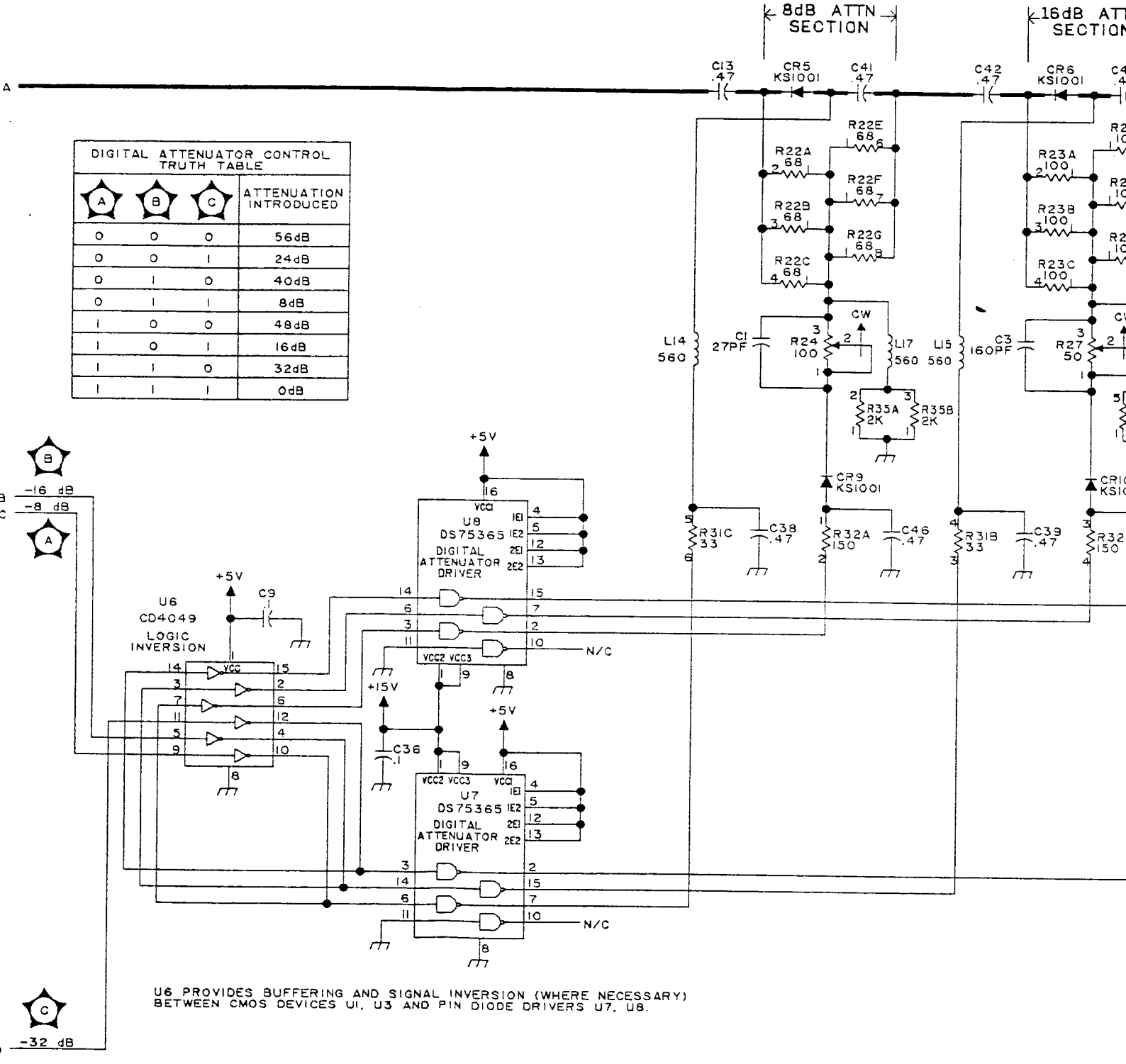
A

DIGITAL ATTENUATOR CONTROL TRUTH TABLE			
A	B	C	ATTENUATION INTRODUCED
0	0	0	56dB
0	0	1	24dB
0	1	0	40dB
0	1	1	8dB
1	0	0	48dB
1	0	1	16dB
1	1	0	32dB
1	1	1	0dB



U6 PROVIDES BUFFERING AND SIGN
BETWEEN CMOS DEVICES U1, U3 AN

DIGITAL



DIGITAL ATTENUATOR CONTROL TRUTH TABLE			
A	B	C	ATTENUATION INTRODUCED
0	0	0	56dB
0	0	1	24dB
0	1	0	40dB
0	1	1	8dB
1	0	0	48dB
1	0	1	16dB
1	1	0	32dB
1	1	1	0dB

U6 PROVIDES BUFFERING AND SIGNAL INVERSION (WHERE NECESSARY) BETWEEN CMOS DEVICES U1, U3 AND PIN DIODE DRIVERS U7, U8.

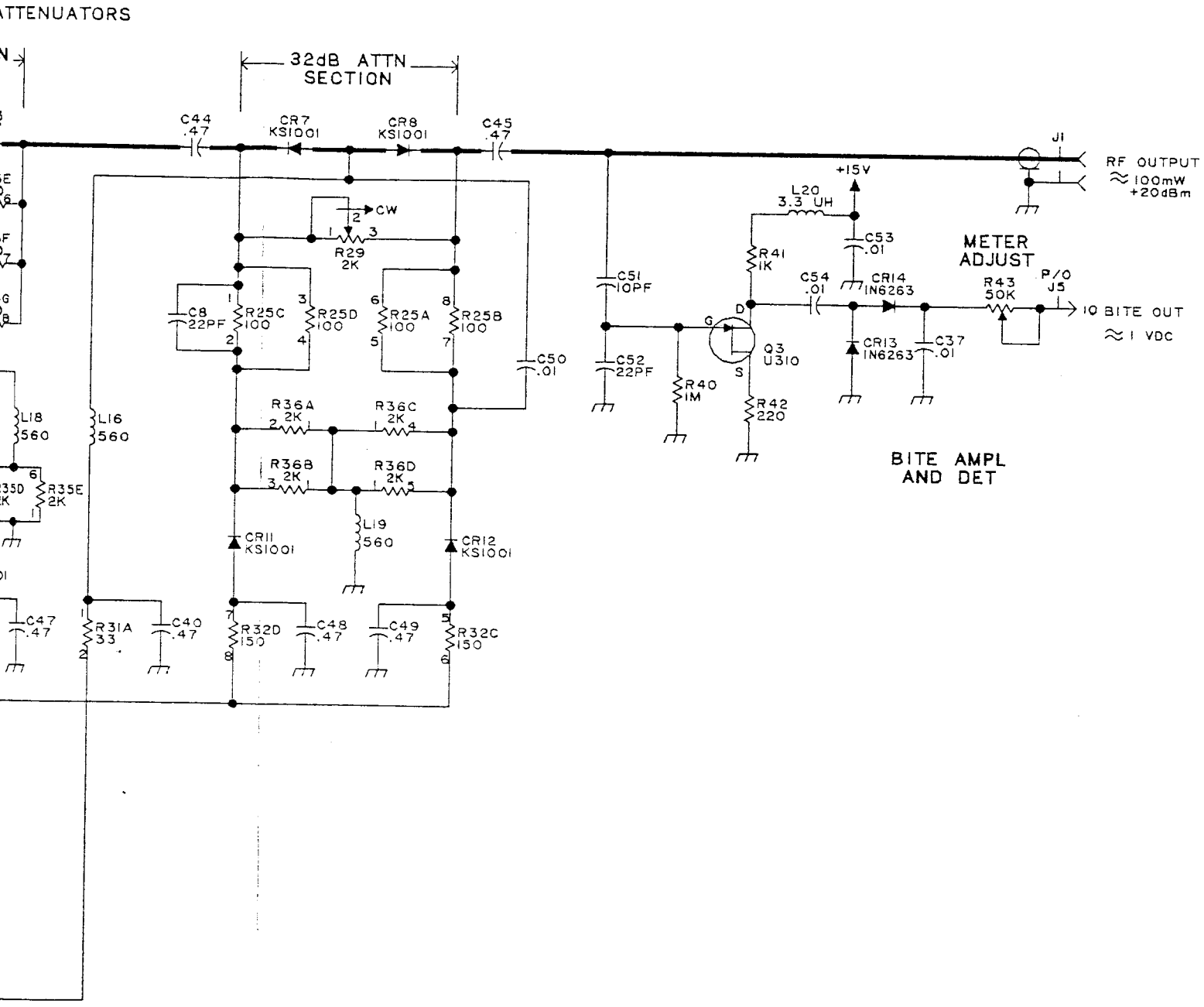


Figure 9. Output Amplifier Assembly A1 Schematic Diagram (10121-5101 Rev. D) (Sheet 2 of 2)