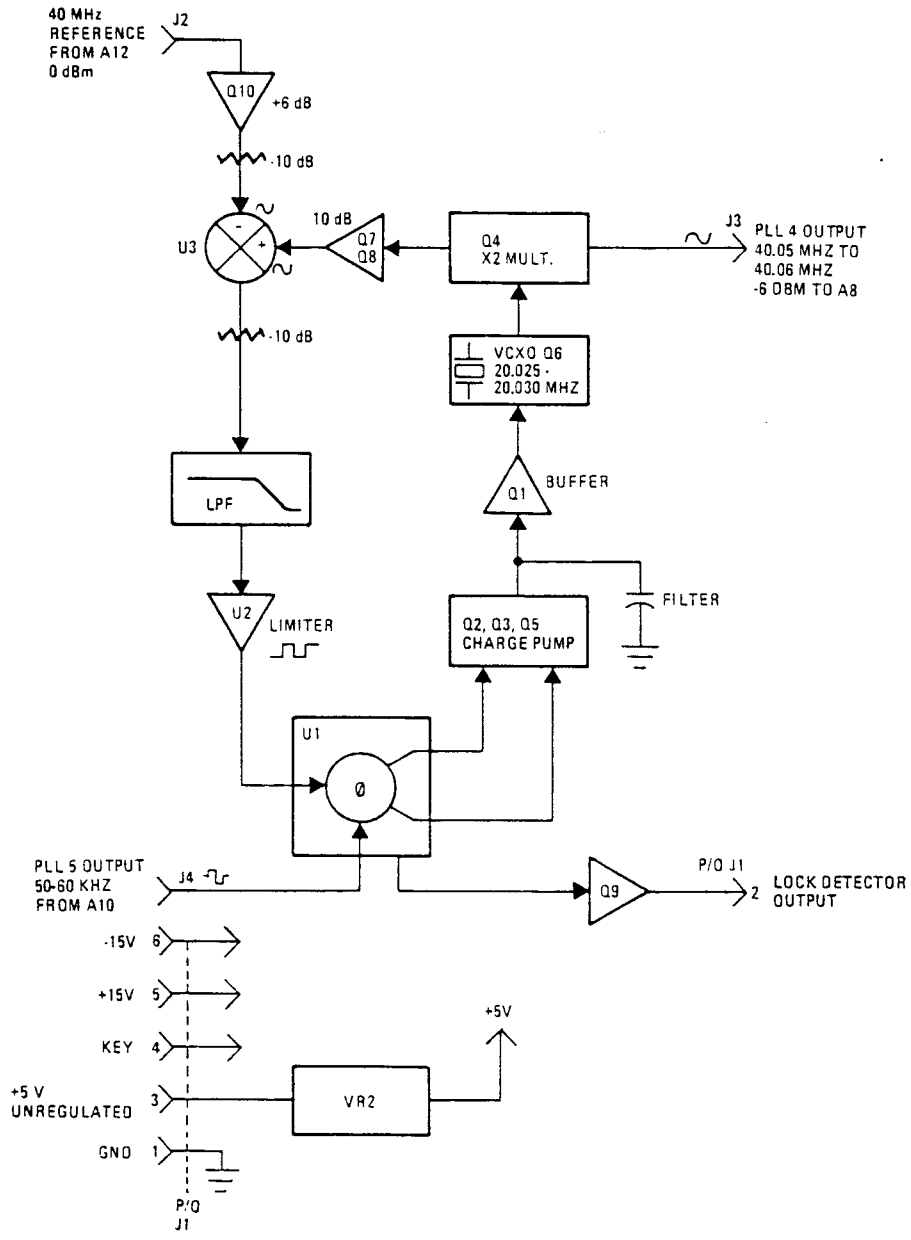
# A9

# PLL 4 ASSEMBLY




1310-087

## TABLE OF CONTENTS



## LIST OF FIGURES



## LIST OF TABLES

# PLL 4 ASSEMBLY A9

## 1. GENERAL DESCRIPTION

PLL 4 Assembly A9 is a translation type phase lock loop which converts the low frequency variable PLL 5 output at 50 to 60 kHz (in 10 Hz steps) into a higher frequency signal at 40.05 to 40.06 MHz. During translation, the 10 Hz step size is preserved. This conversion process is an intermediate step leading toward the 1 Hz, 10 Hz, and 100 Hz tuning increments in the RF-1310 LO 1 frequency range of 40.465 to 70.455 MHz. The 1 Hz, 10 Hz, and 100 Hz tuning increments are defined by the digits in corresponding positions of the transmit frequency.

Figure 1 shows the location of PLL 4 Assembly A9 in the RF-1310 chassis.

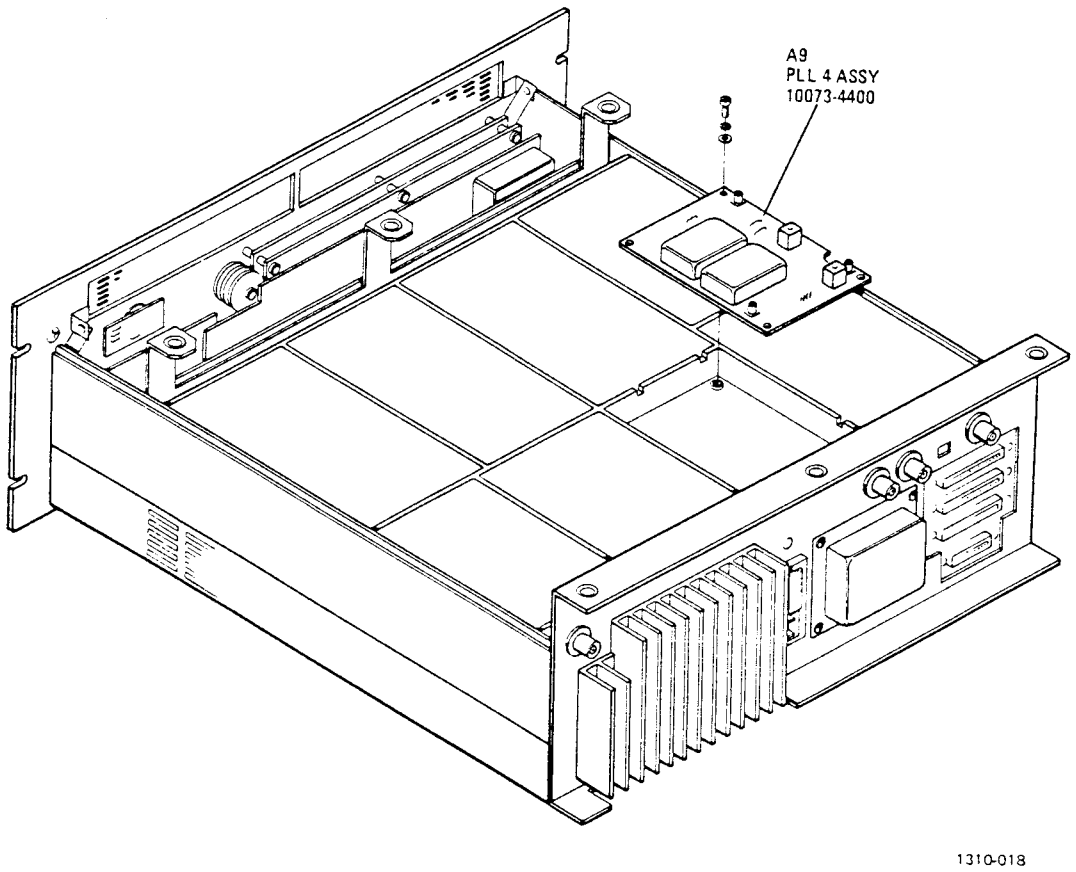



Figure 1. PLL 4 Assembly A9 Location

## 2. INTERFACE CONNECTIONS

Table 1 details the input/output connections and other relevant data.

Table 1. PLL 4 Assembly Interface Connections

| Connector | Function | Characteristics |
|---|---|---|
| J1-1 | Ground | |
| J1-2 | Lock Detector Output | 0 V = Locked, + 5 V = unlocked, P.O BITE Test |
| J1-3 | + 5 Volts Unregulated | Approximately 50 mA |
| J1-4 | Key | |
| J1-5 | + 15 V | Approximately 60 mA |
| J1-6 | -15 V | Approximately 6 mA |
| J2 | 40 MHz Reference | 40.000000 MHz, 0 dBm |
| J3 | PLL 4 Output | 40.050 to 40.060 MHz, -6 dBm |
| J4 | PLL 5 Input | 50.0 to 60.0 kHz, TTL |

## 3. CIRCUIT DESCRIPTION

### 3.1 PLL IF Generation

A PLL intermediate frequency (IF) signal in the range of 50 kHz to 60 kHz is produced at the output of mixer U3. This IF signal is a result of the mixing of the 40.000000 MHz reference from the A12 assembly with a VCXO derived signal in the range of 40.050 to 40.060 MHz.

This IF signal is then compared against the PLL 5 output (a signal also in the range of 50 to 60 kHz) at phase comparator U1. If there is any difference in phase or frequency between the IF and the PLL 5 output signals, U1 produces an error output which forces the VCXO to shift in frequency. The new IF produced will be equal to the A10 output frequency. The net result is that the VCXO derived frequency always equals the reference plus the A10 output frequency (even as the A10 output changes frequencies). As the A10 output changes from 50 to 60 kHz in 10 Hz increments, the A9 output will change from 40.050 MHz to 40.060 MHz (also in 10 Hz increments).

The actual value of the PLL 4 output frequency can be determined by the following formula. f = [40.000,000 + 10 (6000-XXX)] Hz, where XXX is the value of the three least significant digits of the transmit frequency. The 1 Hz digit is not displayed and is always zero.

The 40.000000 MHz reference signal from the A12 assembly enters A9 at J2 (0 dBm) and is applied to 6 dB gain amplifier stage Q10. The signal is attenuated to -4 dBm by 50-ohm matching network R28, R29, and R30. This signal is applied to the RF port of mixer U3 at pin 1.

U3 LO injection at pin 8 is a 40.05 MHz to 40.06 MHz signal derived from the VCXO, and amplified to a + 7 dBm level by LO amplifier stage Q7 and Q8.

U3 mixing action produces a 30 mVrms IF signal at pins 3 and 4 (in 50 to 60 kHz range). The -6 dB matching network R31, R32, and R34 couples this signal to a low pass filter network which removes all undesired mixer products except the IF signal. High gain amplifier U2 boosts this signal to a TTL level prior to application to one side of phase comparator U1.

### 3.2 Phase Comparator and Charge Pump Circuits

Phase comparator U1 compares the IF signal with PLL 5 output signals in the range of 50 to 60 kHz. When these two signals are equal in frequency and phase, U1 outputs at TP2 and TP3 are essentially 5 Vdc. All transistors in the charge pump circuit (Q2, Q3, and Q5) are turned off. The voltage across C19 is constant and Q1 is biased on producing a constant VCXO control voltage across R4. This holds the VCXO frequency constant.

Assume that PLL 5 output increases in frequency. The PLL 5 output frequency at U1, pin 1, will be higher than the IF signal frequency at pin 3. The U1 output at TP3 pulses low, turning Q5 on. Consequently, Q2 turns on as the Q5 collector voltage drops. Q2 pumps charge into C19, causing Q1 to conduct more current with a proportional increase in voltage across R4. This rising control voltage forces the VCXO to increase in frequency, producing a corresponding increase in the IF frequency. As this new IF signal approaches the PLL 5 output frequency, the phase comparator output pulse width becomes narrower, until it is essentially a constant 5 Vdc. Q5 and Q2 turn off, the voltage rise in C19 stops at a new higher level, and the VCXO frequency stabilizes. The two phase comparator inputs are again equal.

Assume that the PLL 5 output decreases in frequency. This time the U1 output at TP2 will pulse low (the pulse width being a function of the difference in frequency at the inputs.) Q3 turns on and C19 now has a low impedance discharge path to ground. As the C19 voltage drops, Q1 conduction decreases, and the voltage across R4 decreases. This forces the VCXO to decrease in frequency which causes a corresponding decrease in the IF frequency. As the two U1 inputs become equal, the negative pulses at TP2 become narrower, until an essentially 5 Vdc level exists. Q3 turns off, holding the C19 voltage and consequently the R4 voltage at a new lower level. The VCXO stops decreasing and also rests at a new lower frequency.

### 3.3 VCO Operation and Control

A charge pump circuit consisting of Q2, Q3, Q5, and associated components in conjunction with filter network C19-R6 convert the two phase comparator pulse outputs into an analog dc control voltage. Buffer amplifier Q1 applies this control voltage to varactor diodes CR1 and CR2 in the VCXO circuit. As the capacitance of these diodes changes due to control voltage fluctuations, JFET Hartley oscillator stage Q6 shifts in frequency. This oscillator stage is crystal controlled by Y1 and operates at 20.025 to 20.030 MHz, which is one-half the desired output frequency range. Therefore, X2 multiplier stage Q4 is used to produce the desired VCXO range of 40.050 to 40.060 MHz. A control voltage of approximately 5 Vdc will tune the VCXO to produce 40.050 MHz at J3, while a control voltage of 10 Vdc will tune it to 40.060 MHz.

VCXO output is applied through an attenuator network to J3 at a level of -6 dBm and on to PLL 3 Assembly A8. It is also applied to 10 dB amplifier stage Q7 and Q8 which functions as a local oscillator (LO) amplifier for U3. This stage provides a +7 dBm LO injection to U3, pin 8, to complete the feedback loop.

## 4. BITE TEST CIRCUITS

Lock detector Q9 monitors the status of phase comparator U1 outputs at TP2 and TP3. If either output pulses low and remains low for a period exceeding the time constants of C57 and R38, the appropriate diode will conduct. Q9 will turn on and the voltage across R41 will increase from 0 to +5 Vdc, indicating an out of lock condition. This immediately flags BITE monitoring circuits on Control Assembly A14. A front panel fault light indicator will turn on.

## 5. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. Perform tests with all connections in normal contact, unless otherwise specified.

### 5.1 X2 Multiplier, LO Amplifier, and RF Amplifier Alignment

Perform the following procedure to align the X2 multiplier, LO, and RF amplifiers:

a. Connect equipment as shown in figure 2.

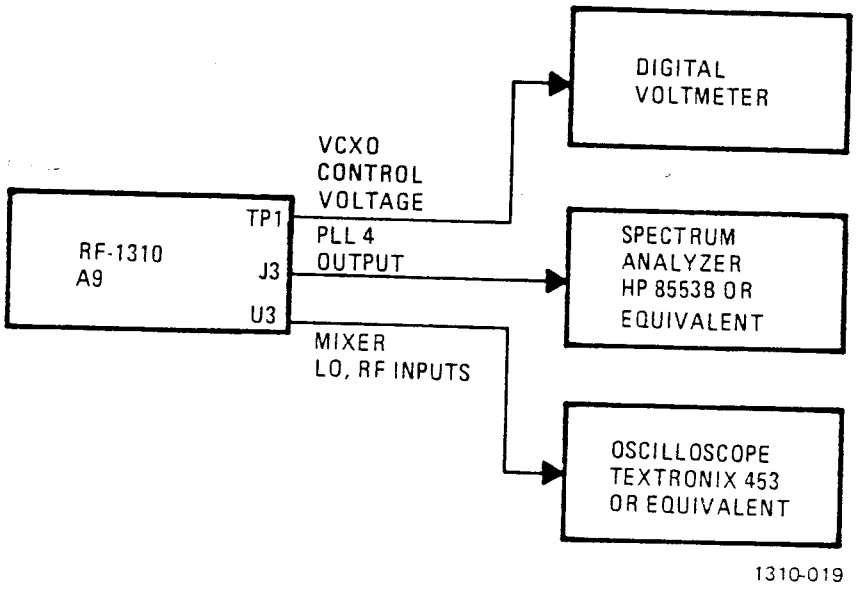



Figure 2. X2 Multiplier, LO, and RF Amplifier Alignment

b. Set exciter to 02.00050 MHz.

c. Monitoring TP1, adjust C23 for 7.5 Vdc.

d. Monitoring J3, adjust T5 and T3 for maximum output level at approximately 40.055 MHz. Level should be -6 dBm ± 3 dB.

e. Monitoring mixer U3 LO input at pin 8, adjust L10 and T4 for maximum level at approximately 40.455 MHz. Level should be approximately 1.25 Vpp ± .5 volts.

f. Monitoring mixer U3 RF input at R28, adjust T2 for a maximum level at 40.000 MHz. Level should be .75 Vpp ± .5 volts. Test is now complete.

### 5.2 VCXO Alignment

Perform the following procedure to align the VCXO:

a. Connect equipment as shown in figure 3.

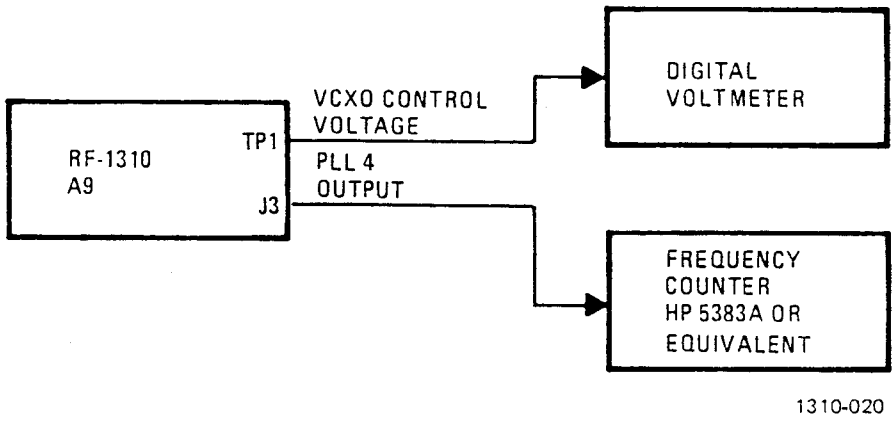



Figure 3. VCXO Alignment

b. Set exciter to 02.00050 MHz. Adjust C23 for 7.5 Vdc.

c. Check that the PLL 4 output frequency, as a function of the exciter tune frequency, agrees with table 2.

Table 2. VCXO Alignment

| Exciter Tune Frequency, MHz | PLL 4 Output Frequency, MHz | Approximate TP1 Voltage, Vdc |
|---|---|---|
| 02.00000 | 40.060 | 10.0 |
| 02.00050 | 40.055 | 7.5 |
| 02.00099 | 40.050 | 5.0 |

d. Fully reconnect the A9 assembly to the RF-1310. Initiate BITE self test. Exciter must pass all tests associated with A9 assembly. Test is now complete.

## 6. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components of the A9 assembly are listed in table 3. The component locations are shown in figure 4. Figure 5 is a schematic diagram of PLL 4 Assembly A9.

Table 3. PLL 4 Assembly A9 Parts List

| Ref. Desig. | Part Number | Description |
|---|---|---|
| A9 | 10073-4400 | PLL 4 ASSEMBLY |
| 1 | 10073-7116 | CAN RECT DEEP DRAWN |
| 2 | MP-0121 | CLIP, MTG, SPRING STEEL |
| 9 | 10073-7113 | SHIELD, COIL |
| 10 | E70-0002-002 | PAD MNT XSTR TO-5 |
| C1 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C2 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C3 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C4 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C5 | C26-0025-100 | CAP 10UF 20% 25V TANT |
| C6 | CK05BX102M | CAP 1000PF 20% 200V CER |
| C7 | CK05BX102M | CAP 1000PF 20% 200V CER |
| C8 | CM06FD102J03 | CAP 1000PF 5% 500V MICA |
| C9 | C26-0025-100 | CAP 10UF 20% 25V TANT |
| C10 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C11 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C12 | CK05BX103M | CAP .01UF 20% 100V CER |
| C13 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C14 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C15 | C26-0025-100 | CAP 10UF 20% 25V TANT |
| C16 | C26-0025-100 | CAP 10UF 20% 25V TANT |
| C17 | CK05BX103M | CAP .01UF 20% 100V CER |
| C18 | C26-0025-339 | CAP 3.3UF 20% 25V TANT |
| C19 | C25-0003-004 | CAP 0.33UF 10% 50V TANT |
| C20 | C26-0025-100 | CAP 10UF 20% 25V TANT |
| C21 | CM04ED680J03 | CAP 68PF 5% 500V MICA |
| C22 | CK05BX103M | CAP .01UF 20% 100V CER |
| C23 | C85-0001-002 | CAPACITOR .8-10 PF |
| C24 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C25 | CK05BX103M | CAP .01UF 20% 100V CER |
| C26 | CK05BX103M | CAP .01UF 20% 100V CER |
| C27 | CM04ED470J03 | CAP 47PF 5% 500V MICA |
| C28 | CK05BX103M | CAP .01UF 20% 100V CER |
| C29 | M39014/02-1320 | CAP .47UF 10% 50V CER-R |
| C30 | CK05BX102M | CAP 1000PF 20% 200V CER |
| C31 | CK05BX103M | CAP .01UF 20% 100V CER |
| C32 | CM04CD010D03 | CAP 1PF +-.5PF 500V MICA |
| C33 | CM04ED470J03 | CAP 47PF 5% 500V MICA |
| C34 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C35 | CM04ED510J03 | CAP 51PF 5% 500V MICA |

Table 3. PLL 4 Assembly A9 Parts List (Cont.)

| Ref. Desig. | Part Number | Description |
|---|---|---|
| C36 | CK05BX103M | CAP .01UF 20% 100V CER |
| C37 | CK05BX103M | CAP .01UF 20% 100V CER |
| C38 | CK05BX103M | CAP .01UF 20% 100V CER |
| C39 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C40 | CK05BX103M | CAP .01UF 20% 100V CER |
| C41 | CK05BX103M | CAP .01UF 20% 100V CER |
| C42 | C26-0025-100 | CAP 10UF 20% 25V TANT |
| C43 | CM04ED300J03 | CAP 30PF 5% 500V MICA |
| C44 | CM04ED330J03 | CAP 33PF 5% 500V MICA |
| C45 | CK05BX103M | CAP .01UF 20% 100V CER |
| C46 | CK05BX103M | CAP .01UF 20% 100V CER |
| C47 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C48 | M39014/02-1310 | CAP .1UF 10% 100V CER-R |
| C49 | CK05BX103M | CAP .01UF 20% 100V CER |
| C50 | C-0912 | CAPACITOR |
| C51 | C-0911 | 200V .01 MFD TUBE |
| C52 | CM06FD272J03 | CAP 2700PF 5% 500V MICA |
| C53 | CM06FD272J03 | CAP 2700PF 5% 500V MICA |
| C54 | CM06FD272J03 | CAP 2700PF 5% 500V MICA |
| C55 | C-0912 | CAPACITOR |
| C56 | C-0912 | CAPACITOR |
| C57 | C25-0001-301 | CAP 1.0UF 20% 20V TANT |
| C59 | CM04ED270J03 | CAP 27PF 5% 500V MICA |
| C60 | CK05BX103M | CAP .01UF 20% 100V CER |
| C61 | CK05BX103M | CAP .01UF 20% 100V CER |
| CR1 | 10073-7118 | VARACTOR 26.0-32.0PF |
| CR2 | 10073-7118 | VARACTOR 26.0-32.0PF |
| CR4 | 1N3064 | DIODE 75mA 75V SW |
| CR5 | 1N3064 | DIODE 75mA 75V SW |
| CR6 | 1N3064 | DIODE 75mA 75V SW |
| J1 | J46-0032-006 | HDR 6 PIN 0.100"SR |
| J2 | J-0031 | CONN SMB VERT PCB F |
| J3 | J-0031 | CONN SMB VERT PCB F |
| J4 | J-0031 | CONN SMB VERT PCB F |
| L1 | L08-0001-001 | CHOKE W B 50 MHZ |
| L2 | L08-0001-001 | CHOKE W B 50 MHZ |
| L3 | MS14046-9 | COIL 27UH 10% FXD RF |
| L4 | MS75084-17 | COIL 27.0UH 10% FXD RF |
| L5 | MS75084-3 | COIL 1.8UH 10% FXD RF |
| L6 | MS75084-17 | COIL 27.0UH 10% FXD RF |
| L7 | MS75084-6 | COIL 3.3UH 10% FXD RF |
| L9 | MS90538-8 | COIL 68UH 5% FXD RF |
| L9 | MS90538-8 | COIL 68UH 5% FXD RF |
| L10 | 10073-7011 | TRANSFORMER, RF, VARIABLE |
| Q1 | Q05-0001-000 | XSTR JFET N-CH |

Table 3. PLL 4 Assembly A9 Parts List (Cont.)

| Ref. Desig. | Part Number | Description |
|---|---|---|
| Q2 | 2N2907 | XSTR SS/GP PNP TO-18 |
| Q3 | 2N2222 | XSTR SS/GP NPN TO-18 |
| Q4 | 2N2369 | XSTR SS/RF NPN |
| Q5 | 2N2222 | XSTR SS/GP NPN TO-18 |
| Q6 | Q35-0003-000 | XSTR U310 JFET HIGH GM |
| Q7 | 2N5109 | XSTR RFPWR NPN TO-39 |
| Q8 | Q35-0003-000 | XSTR U310 JFET HIGH GM |
| Q9 | 2N2907 | XSTR SS/GP PNP TO-18 |
| Q10 | Q35-0003-000 | XSTR U310 JFET HIGH GM |
| R1 | R65-0003-201 | RES 200 5% 1/4W CAR FILM |
| R2 | R65-0003-201 | RES 200 5% 1/4W CAR FILM |
| R3 | R65-0003-472 | RES 4.7K 5% 1/4W CAR FILM |
| R4 | R65-0003-332 | RES 3.3K 5% 1/4W CAR FILM |
| R5 | R65-0003-201 | RES 200 5% 1/4W CAR FILM |
| R6 | RN55D1211F | RES 1210 1% 1/8W MET FLM |
| R7 | RN55D6810F | RES 681.0 1% 1/8W MET FLM |
| R8 | R65-0003-121 | RES 120 5% 1/4W CAR FILM |
| R9 | R65-0003-103 | RES 10K 5% 1/4W CAR FILM |
| R10 | RN55D3321F | RES 3320 1% 1/8W MET FLM |
| R11 | R65-0003-201 | RES 200 5% 1/4W CAR FILM |
| R12 | R65-0003-101 | RES 100 5% 1/4W CAR FILM |
| R13 | RN55D6810F | RES 681.0 1% 1/8W MET FLM |
| R14 | RN55D6810F | RES 681.0 1% 1/8W MET FLM |
| R15 | RN55D6810F | RES 681.0 1% 1/8W MET FLM |
| R16 | R65-0003-911 | RES 910 5% 1/4W CAR FILM |
| R17 | R65-0003-101 | RES 100 5% 1/4W CAR FILM |
| R18 | R65-0003-101 | RES 100 5% 1/4W CAR FILM |
| R19 | R65-0003-470 | RES 47 5% 1/4W CAR FILM |
| R20 | R65-0003-470 | RES 47 5% 1/4W CAR FILM |
| R21 | R65-0003-201 | RES 200 5% 1/4W CAR FILM |
| R22 | R65-0003-242 | RES 2.4K 5% 1/4W CAR FILM |
| R23 | R65-0003-182 | RES 1.8K 5% 1/4W CAR FILM |
| R24 | R65-0003-511 | RES 510 5% 1/4W CAR FILM |
| R25 | R65-0003-471 | RES 470 5% 1/4W CAR FILM |
| R26 | R65-0003-390 | RES 39 5% 1/4W CAR FILM |
| R27 | R65-0003-121 | RES 120 5% 1/4W CAR FILM |
| R28 | R65-0003-101 | RES 100 5% 1/4W CAR FILM |
| R29 | R65-0003-750 | RES 75 5% 1/4W CAR FILM |
| R30 | R65-0003-101 | RES 100 5% 1/4W CAR FILM |
| R31 | R65-0003-101 | RES 100 5% 1/4W CAR FILM |
| R32 | R65-0003-101 | RES 100 5% 1/4W CAR FILM |
| R33 | R65-0003-510 | RES 51 5% 1/4W CAR FILM |
| R34 | R65-0003-750 | RES 75 5% 1/4W CAR FILM |
| R35 | RN55D1001F | RES 1000 1% 1/8W MET FILM |
| R36 | R65-0003-201 | RES 200 5% 1/4W CAR FILM |

Table 3. PLL 4 Assembly A9 Parts List (Cont.)

| Ref. Desig. | Part Number | Description |
|---|---|---|
| R37 | R65-0003-470 | RES 47 5% 1/4W CAR FILM |
| R38 | R65-0003-472 | RES 4.7K 5% 1/4W CAR FILM |
| R39 | R65-0003-472 | RES 4.7K 5% 1/4W CAR FILM |
| R40 | R65-0003-472 | RES 4.7K 5% 1/4W CAR FILM |
| R41 | R65-0003-103 | RES 10K 5% 1/4W CAR FILM |
| R42 | R65-0003-471 | RES 470 5% 1/4W CAR FILM |
| R43 | R65-0003-101 | RES 100 5% 1/4W CAR FILM |
| T1 | 10073-7008 | TRANSFORMER, RF, FIXED |
| T2 | 10073-7012 | TRANSFORMER, RF, FIXED |
| T3 | 10073-7015 | TRANSFORMER, RF, FIXED |
| T4 | 10073-7011 | TRANSFORMER, RF, FIXED |
| T5 | 10073-7011 | TRANSFORMER, RF, FIXED |
| TP1 | J-0071 | TP PWB BRN TOP ACCS .080" |
| TP2 | J-0066 | TP PWB BRN TOP ACCS .080" |
| TP3 | J-0069 | TP PWB BRN TOP ACCS .080" |
| TP4 | J-0070 | TP PWB BRN TOP ACCS .080" |
| TP5 | J-0068 | TP PWB BRN TOP ACCS .080" |
| U1 | IC-0430 | IC MC4044 CERAMIC CMOS |
| U2 | I20-0005-001 | IC LM211H COMPARATOR |
| U3 | I51-0003-003 | MIXER DB 50mW 500 MHZ |
| VR1 | 1N5236 | DIODE 7.5V 20% 5W ZENER |
| VR2 | I11-0001-001 | IC VR 7805 + 5V 1.5A 4% |
| Y1 | 10073-7039 | CRYSTAL 20.0275 MHZ |

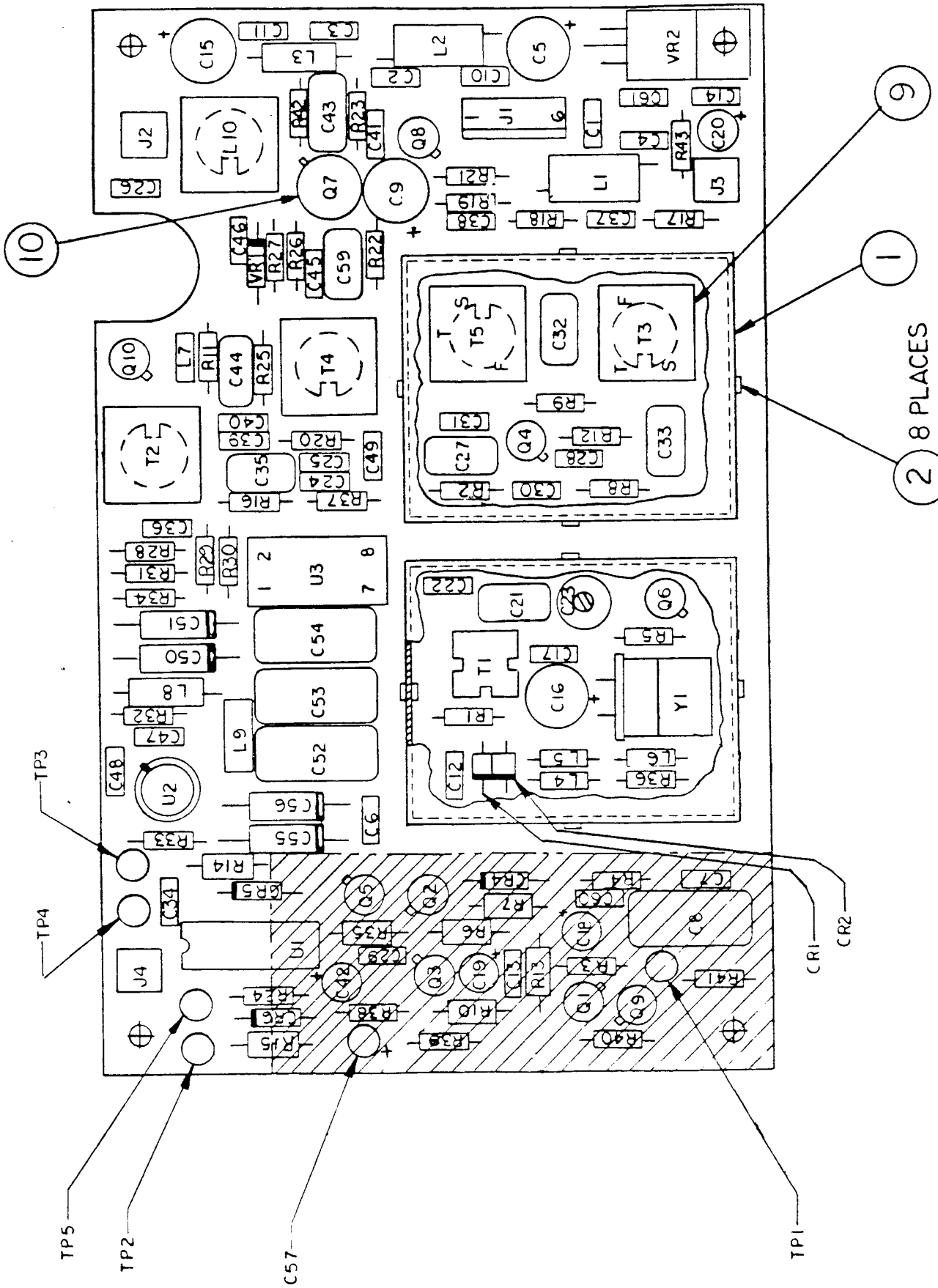
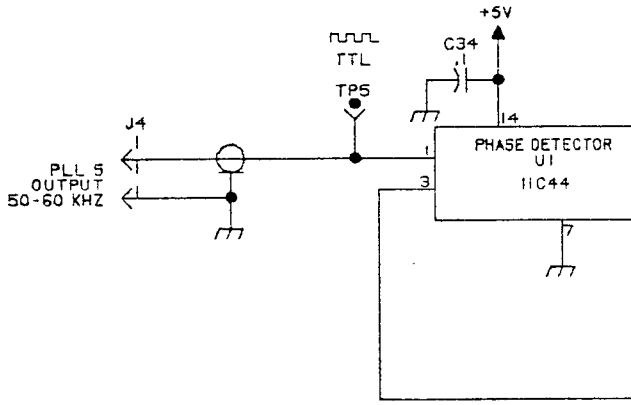
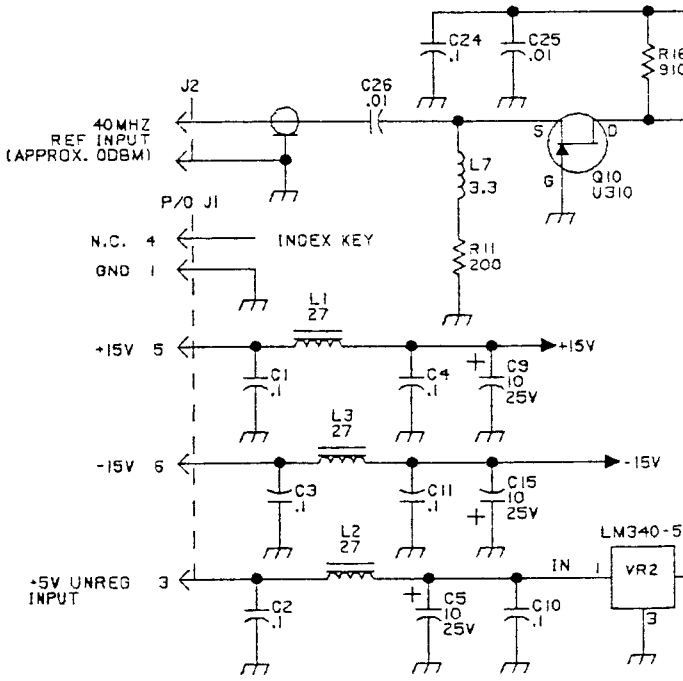



Figure 4. PLL 4 Assembly A9 Component Location Diagram (10073-4400)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. ALL INDUCTOR VALUES ARE IN MICROHENRIES.



SS OTHERWISE SPECIFIED:

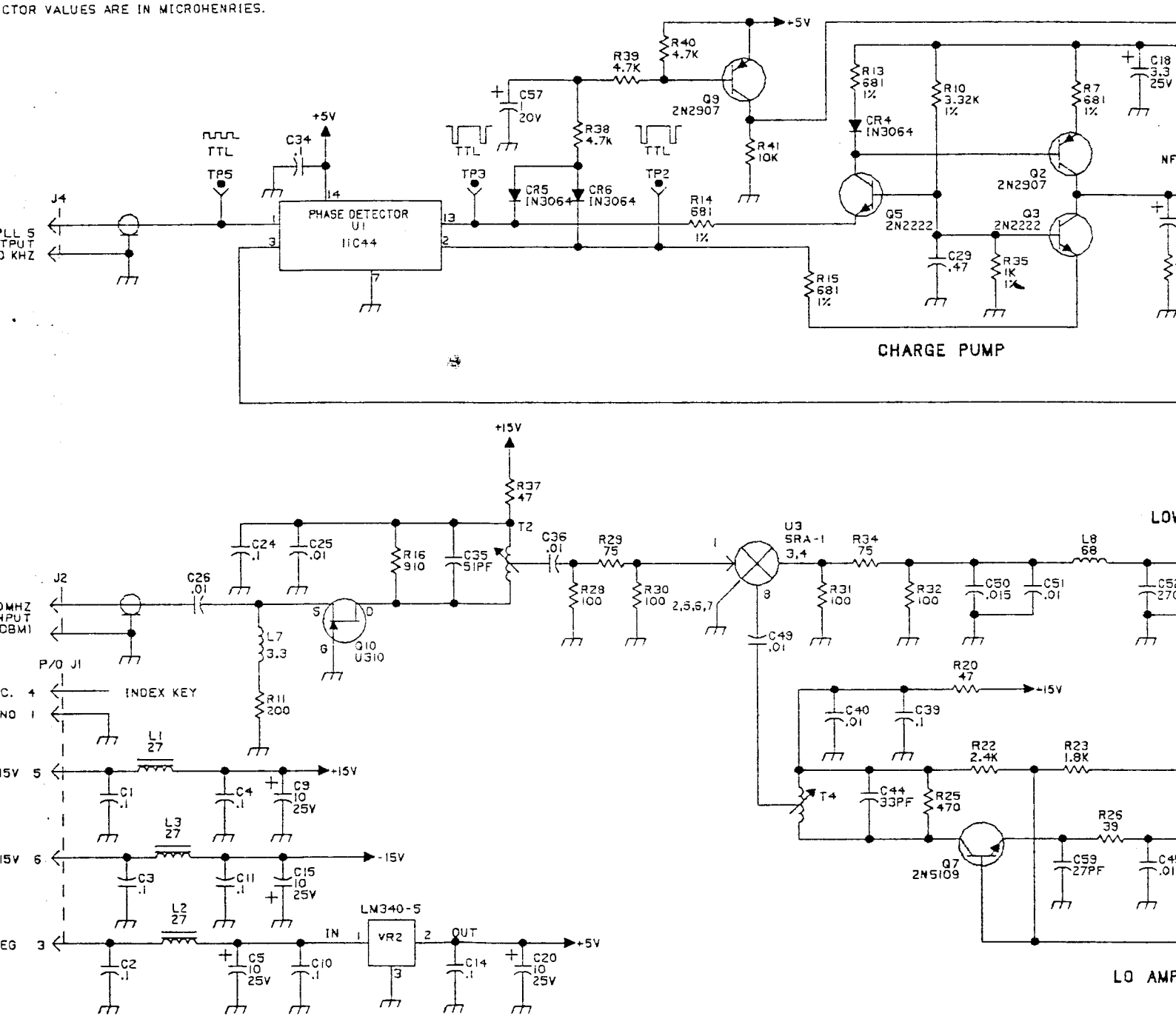
REFERENCE DESIGNATIONS ARE SHOWN.
MPLETE DESIGNATION, PREFIX WITH
AND/OR ASSEMBLY NO. DESIGNATION.

STOR VALUES ARE IN OHMS, 1/4W, ±5%.

ACITOR VALUES ARE IN MICROFARADS.

PART NO. CALLOUTS ARE FOR REFERENCE ONLY.
NTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

CTOR VALUES ARE IN MICROHENRIES.



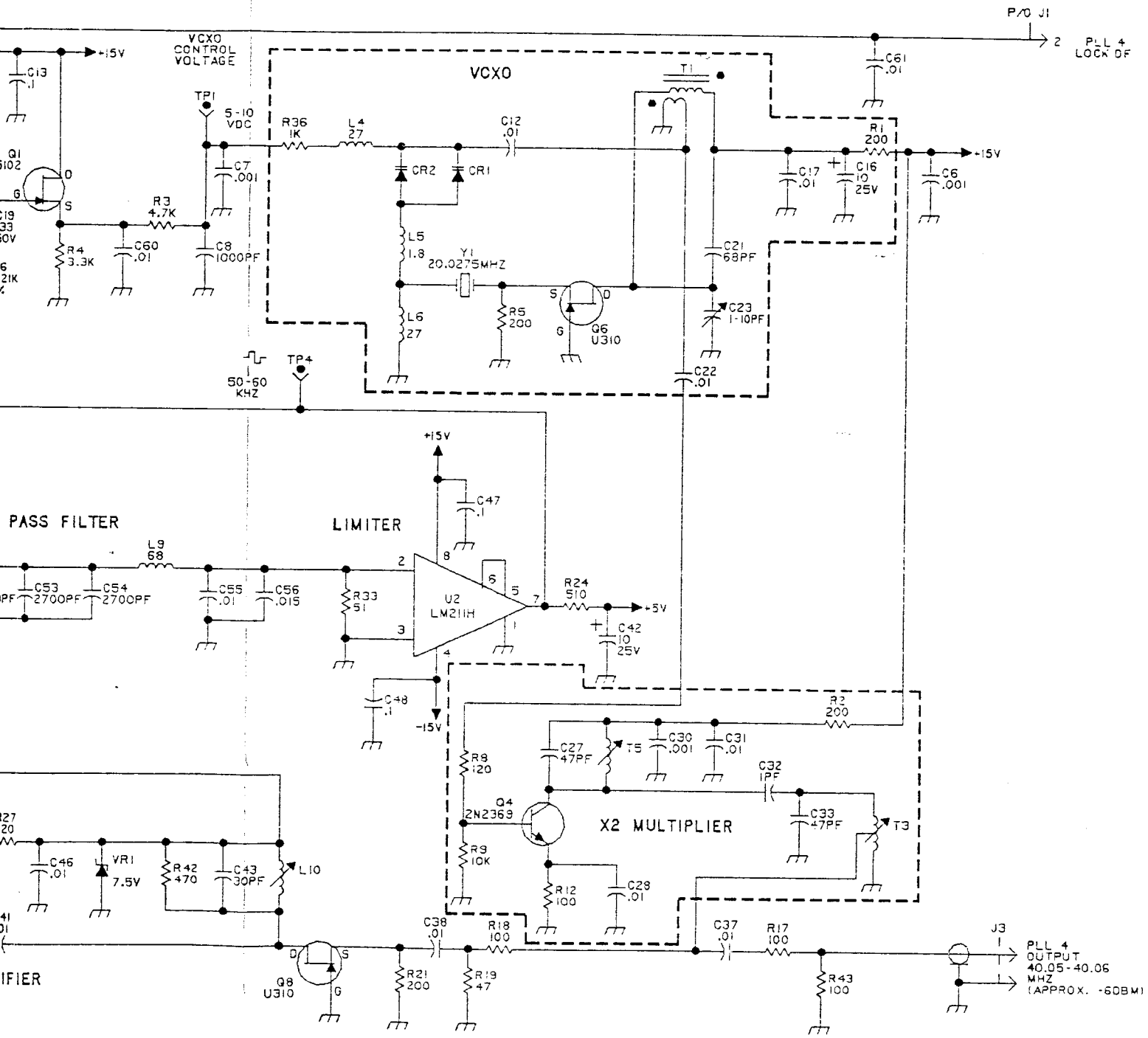



Figure 5. PLL 4 Assembly A9 Schematic Diagram (10073-4401 Rev.D)