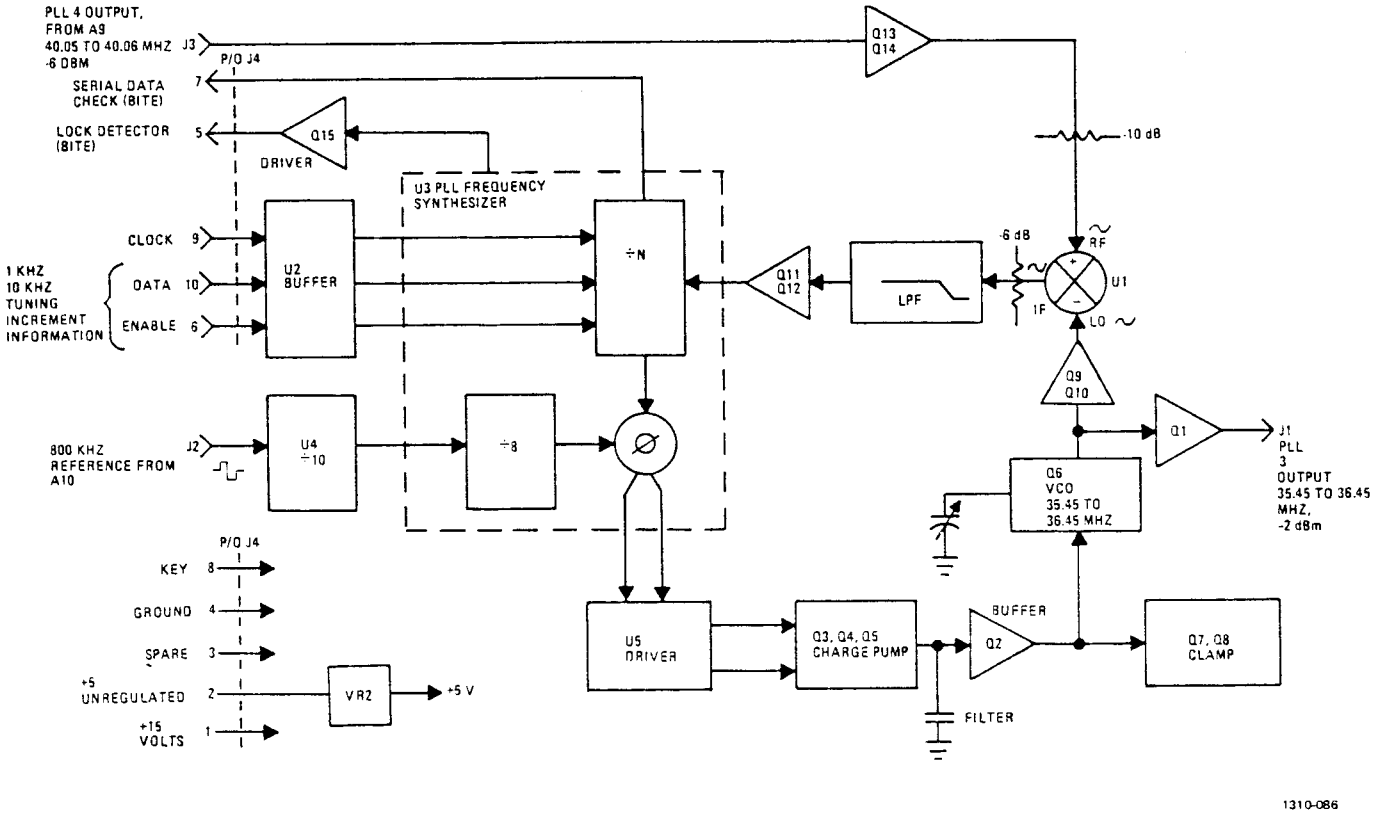
A8
PLL 3 ASSEMBLY



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PLL 3 ASSEMBLY A8

1. GENERAL DESCRIPTION

PLL 3 Assembly A8 is a programmable translation loop which performs the following primary functions:

- Generation of 1 kHz and 10 kHz tuning increments of the LO 1 frequency.
- Combination of these increments with information containing the 1 Hz, 10 Hz, and 100 Hz increments of the LO 1 frequency.

Figure 1 shows the location of PLL 3 Assembly A8 in the RF-1310 chassis.

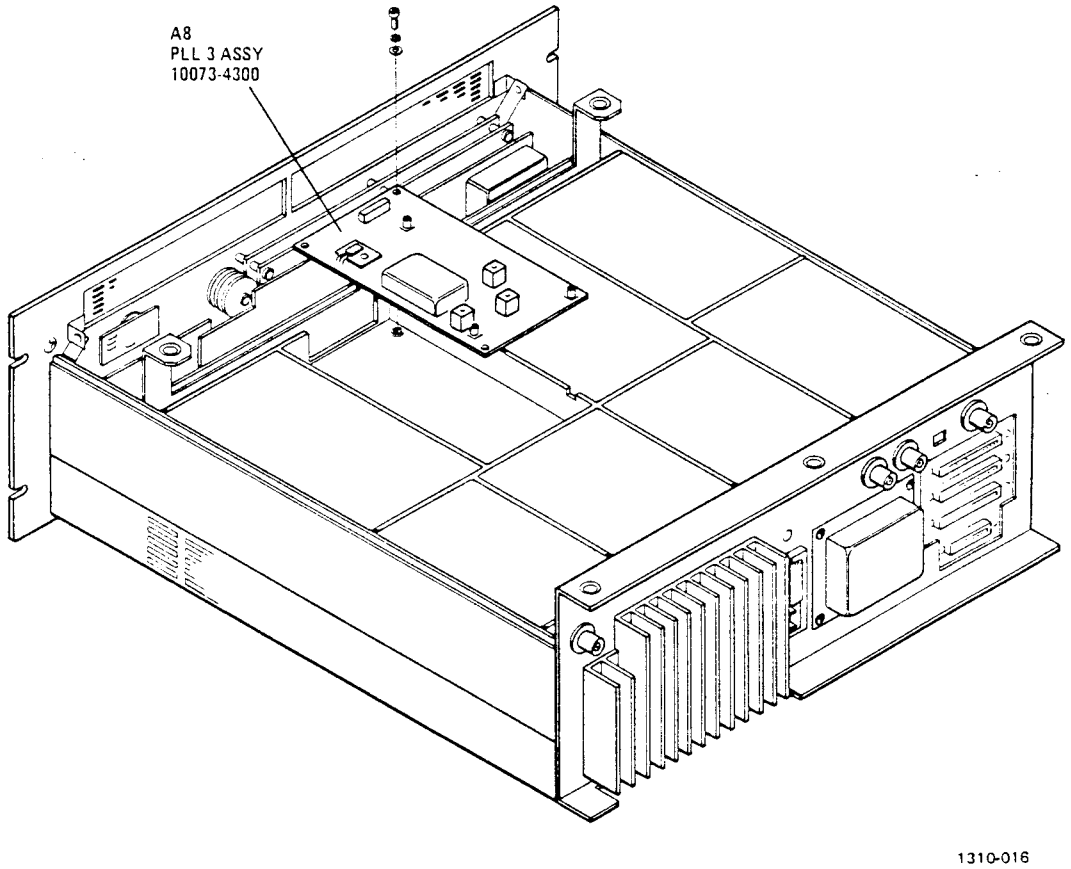

Figure 1. PLL 3 Assembly A8 Location

Frequency select input data for 1 kHz and 10 kHz tuning increments is applied to the A8 assembly in serial data format from the Control Board Assembly microprocessor. The 1 Hz, 10 Hz, and 100 Hz tuning increments information is supplied via PLL 4 Assembly A9 in the frequency range of 40.06 to 40.05 MHz. A8 assembly output to PLL 1 Assembly A6 contains 1 Hz, 10 Hz, 100 Hz, 1 kHz, and 10 kHz tuning information in the frequency range of 35.45 to 36.45 MHz.

2. INTERFACE CONNECTIONS

Table 1 details the input/output connections and other relevant data.

Table 1. PLL 3 Assembly Interface Connections

Connector	Function	Characteristics
J1	PLL 3 Output	35.45 to 36.45 MHz, approximately -2 dBm
J2	800 kHz Reference Input	TTL
J3	PLL 4 Input	40.05 to 40.06 MHz, approximately -6 dBm
J4-1	+ 15 Volts	Approximately 60 mA
J4-2	+ 5 Volts Unregulated	Approximately 30 mA
J4-3	Spare	
J4-4	Ground	
J4-5	Lock Detector Output	0 Vdc = PLL locked; + 5 Vdc = PLL unlocked
J4-6	Enable	+ going pulse = enabled
J4-7	Serial Data Check	P/O BITE test, + 5 Vdc = ok
J4-8	Key	
J4-9	Clock	750 kHz, TTL
J4-10	Data	Serial TTL

3. A8 FREQUENCY GENERATION SCHEME

A PLL intermediate frequency (IF) range of 3.61 MHz to 4.61 MHz is produced at the IF output of mixer U1. The instantaneous IF frequency is a consequence of the subtractive mixing of the following two signals:

- 40.050 to 40.060 MHz PLL 4 (RF port)
- 35.45 to 36.45 MHz VCO (LO port)

This IF signal will change in frequency to satisfy the requirement that the divide-by-N counter output will always try to equal the reference 10.000 kHz signal at the inputs to the phase comparator (P/O U3). When these two signals are not equal, the phase comparator produces an error command to drive the VCO frequency in the direction required to make them equal. If the divide-by-N output exceeds the reference 10.0000 kHz, the VCO will rise in frequency. If the divide-by-N output is less than the reference, the VCO will decrease in frequency.

The VCO output frequency is dependent upon the following two events:

- The division factor of the divide-by-N counter. N = (361 + XX), where XX represents the digits in the 10 kHz and 1 kHz positions of the displayed frequency.
- The PLL 4 output frequency. This is dependent upon the value of the digits in the 100 Hz, 10 Hz, and 1 Hz positions of the displayed frequency (section A9, PLL IV Assembly).

To illustrate this, assume that the exciter is tuned to a frequency of $X_8X_7X_6X_5X_4X_3X_2X_1$ Hz, where X_8 through X_2 represent the frequency display digits and X_1 is always zero. (See the block diagram on the section cover.)

Example 1: Assume that the $X_3X_2X_1$ value decreases.

a. As $X_3X_2X_1$ decreases the frequency of the PLL 4 output increases.

b. As a result, the frequency of the signal from U1 (the PLL 3 IF) to U3 also increases.

c. Since the N of the programmable frequency divider in U3 has not changed, the output frequency of that divider will increase, making it greater than the 10 kHz reference signal.

d. The phase detector in U3 will detect the difference between the programmable divider output and the reference signal, and the VCO frequency will increase.

e. This reduces the difference in frequency between the PLL 3 VCO output and the signal from PLL 4 to what it was before $X_3X_2X_1$ changed.

Example 2: Assume that the X_5X_4 value decreases.

a. As X_5X_4 decreases, the divide-by-N factor in U3 ($N = 361 + X_5X_4$) decreases.

b. The divide-by-N output frequency, equal to IF divide-by-N, increases. Since this now exceeds the 10.000 kHz reference at the phase comparator inputs, the phase comparator output forces the VCO (LO) frequency to increase.

c. In turn, the difference between the frequencies of the VCO output and the input from PLL 4 (the PLL 3 IF) decreases.

d. The output of the divide-by-N divider in U3 will decrease proportionally with the PLL 3 IF and continue to do so until it equals the 10 kHz reference.

The VCO of PLL 3 will decrease in frequency when $X_3X_2X_1$ or X_5X_4 are increased.

The A8 PLL 3 output frequency may be calculated from the following equation given the selected transmit frequency is X_8X_7, $X_6X_5X_4$, $X_3X_2X_1$ Hz:

$$f_{A8} = [40{,}000{,}000 + 10\,(6000\,X_3X_2X_1)]\,[10{,}000\,(361 + X_5X_4)],\ \text{Hz}$$

4. CIRCUIT DESCRIPTIONS

NOTE

A8 operation is similar to the general PLL and charge pump circuits described in section 4. A review of section 4 at this time would help in understanding A8 assembly operation.

4.1 PLL IF Generation

PLL 4 output at a -6 dBm level is applied to 10 dB gain stage Q13 and Q14. This output is attenuated by 50-ohm matching network R39, R40, and R44, and presents a -6 dBm signal ranging from 40.050 MHz to 40.060 MHz to the RF port of mixer U1.

U1 LO injection is supplied by the VCO via amplifier stage Q9 and Q10 at a +7 dBm level. This signal ranges from 35.45 to 36.45 MHz.

U1 IF output is approximately -12 dBm (in the 3.61 to 4.61 MHz range). The 6 dB attenuator network, R41-R43, feeds a low pass filter which removes all mixer products except the desired IF range. Amplifier stage Q11 and Q12 provide a TTL level signal to a divide-by-N counter internal to U3 at pin 10.

4.2 Divide-By-N Counter

Since the A8 assembly requires a variable output frequency dependent upon the 1 kHz and 10 kHz tuning positions, a divide-by-N programmable counter has been incorporated into the VCO feedback loop. The front panel selection of a tune frequency from 00 kHz to 99 kHz causes Control Assembly A14 to generate a serial data code containing information pertaining to the values chosen. This code is applied synchronously with the 750 kHz system clock to U3, whenever the U3 enable line is gated open by A14.

N = (361 + XX) where XX represents the digits in the 10 kHz and 1 kHz positions of the displayed frequency. The divide-by-N counter output will always attempt to equal the 10.000 kHz reference frequency at the phase comparator inputs.

4.3 Phase Comparator and Charge Pump Operation

A 10.000 kHz reference signal is applied to one port of the phase comparator. This signal has been divided down from the 800 kHz TTL reference supplied by the A10 assembly. Divide-by-10 circuit U4 feeds 80 kHz to the divide-by-8 circuit internal to U3.

The second input to the phase comparator is the divide-by-N counter output. When these two signals are equal in frequency and phase, the outputs at buffer stage U5 (TP2 and TP3) are essentially at a +5 Vdc level. This level holds Q4, Q5, and consequently Q3 off. The voltage across C8 is constant. Q2 is biased to produce a constant voltage across R12, and the dc level (VCO control) at TP1 is constant. This holds the VCO at a constant frequency.

Assuming that the divide-by-N output exceeds the reference 10.000 kHz, the phase comparator output at TP3 pulses low (the pulse width being a function of the amount of difference between the two signals). Q5 turns on, and its falling collector voltage turns Q3 on, allowing Q3 to pump charge into C8. C8 voltage increases, causing Q2 to conduct more current and develop a large voltage across R12. The VCO control voltage increases and forces the VCO to tune higher in frequency. This will lower the IF frequency, and divide-by-N counter output will decrease. As the divide-by-N counter output approaches the reference, the pulse widths will get narrower until a 5 Vdc level will again occur at TP3. At this point, Q5 turns off, Q3 stops pumping charge into C8, the VCO control voltage stops at a new higher level, and the VCO has been tuned to a higher frequency.

Assuming that the divide-by-N counter output is less than the reference, the phase comparator output at TP2 will pulse low. Q4 turns on and draws charge out of C8. Q2 conducts less current, and the VCO voltage drops, driving the VCO frequency down. The IF feedback signal frequency will increase, and consequently the divide-by-N counter output will increase. As this output approaches the reference frequency, TP2 pulses will get narrower until Q4 is turned off. The voltage across C8 halts at a lower value (as does the VCO control voltage level). This holds the VCO at a new lower frequency.

4.4 VCO Operation and Control

A charge pump circuit consisting of Q3, Q4, Q5, and associated components in conjunction with filter network C8, C9, and R14 convert the two phase comparator pulse outputs into an analog dc control voltage. Buffer