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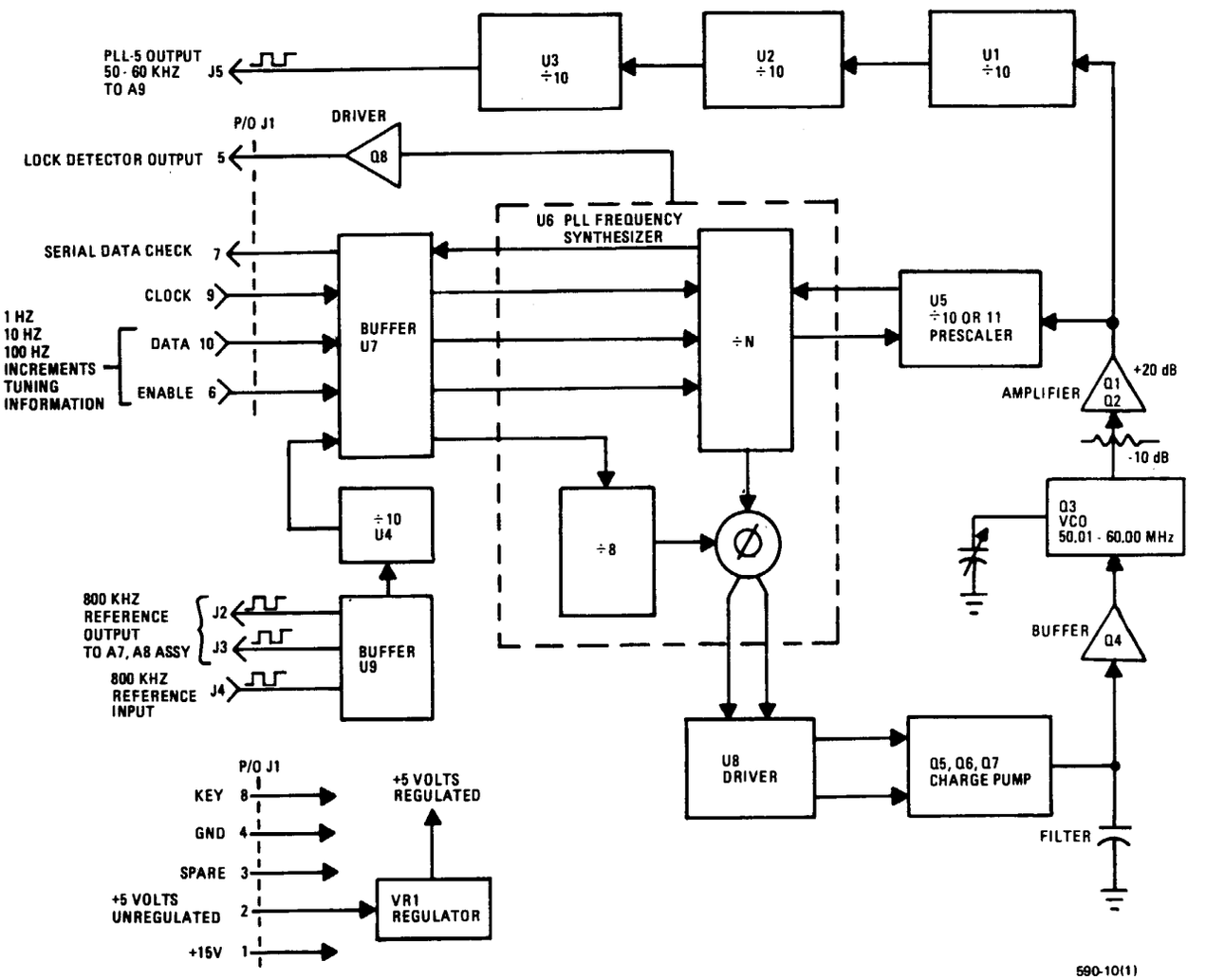

PLL V Assembly A10 Functional Block Diagram

1. GENERAL DESCRIPTION

PLL V Assembly A10 is a single phase locked loop synthesizer that ultimately provides the 1 Hz, 10 Hz, and 100 Hz tuning increments as chosen by the RF-590 front panel frequency selection controls.

Frequency select input data is applied to the assembly in serial data form under Control Board Assembly A14 microprocessor control. A10 output to PLL IV Assembly A9 is a variable 50 to 60 kHz signal in 10 Hz controllable steps. Since 1000 frequency steps are possible, the net results of A10 operation (after further translation to 1 Hz increments in the synthesizer chain) are 1 Hz, 10 Hz, and 100 Hz tuning increments in the LO no. 1 output.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. PLL V Assembly Interface Connections

Connector	Function	Characteristics
J1-1	+15 Volts	Approximately 25 mA
J1-2	+5 Volts unregulated	Approximately 240 mA
J1-3	Spare	
J1-4	Ground	
J1-5	Lock Detector Output	+5 Vdc = unlocked, 0 Vdc = locked, P/O BITE Test
J1-6	Enable	+ going pulse = Enabled
J1-7	Serial Data Check	P/O BITE Test, +5 Vdc = ok
J1-8	Key	
J1-9	Clock	TTL, 750 kHz
J1-10	Data	Serial TTL
J2	800 kHz Reference Output	TTL
J3	800 kHz Reference Output	TTL
J4	800 kHz Reference Input	TTL
J5	PLL-V Output	TTL, 50-60 kHz

3. CIRCUIT DESCRIPTION

NOTE

A10 operation is similar in operation to the general divide by N PLL and charge pump circuits described in section 4. A review of section 4 at this point would aid in the understanding of A10 operation.

3.1 Reference Generation

800 kHz from Reference Generator Assembly A12 enters PLL V Assembly A10 at J4. This signal is buffered via TTL NAND GATES in U9 and directed through J2 and J3 to the A7 and A8 assemblies. It is also routed to divide by 10 counter U4 where it is divided down to 80 kHz. This 80 kHz signal is applied via buffer U7 to a divide by 8 counter internal to U6 to produce a 10 kHz reference signal. Since this has been derived ultimately from the RF-590 crystal frequency standard via the A12 assembly, stable and accurate A10 operation is assured.

3.2 Divide by Counter

Since the A10 assembly requires a variable 50 to 60 kHz output frequency, a programmable counter has been designed into the VCO feedback path to the Phase Comparator. This counter consists of dual modulus ÷ 10/÷ 11 prescaler U5 and a programmable divide by N counter internal to U6. Together U5 and the programmable portion of U6 create a total division range of N = 5001 to N = 6000, where N is a function of the setting of the receiver 1, 10, and 100 Hz tuning positions.

The output of the divide by N counter will always attempt to equal the 10.000 kHz reference frequency at the Phase Comparator inputs, despite changes in the divide by N factor due to changing the 1, 10, and/or 100 Hz receiver tuning increments. The VCO frequency will change to accomplish this (in response to command signals generated by the Phase Comparator). The VCO frequency will always equal (N) (reference frequency), or (N) (10.000 kHz) = 50.01 MHz to 60.00 MHz. Division of this range by 1000 will result in the required A10 output range of 50.01 kHz to 60.00 kHz.

The exact value of N is determined by the value of the 1, 10, and/or 100 Hz receiver tuning positions. This front panel selection causes control assembly A14 to generate a serial data code containing information pertaining to the values of the increments chosen. (This code is applied synchronously with the 750 kHz system clock to U6 whenever the U6 enable line is gated open by A14.) In general, N = (6000 – XXX), where XXX is the value of the 100, 10, and 1 Hz positions chosen at the receiver front panel frequency controls.

For example, tuning the RF-590 to 10.401475 MHz would make N = (6000 – 475) = 5525. The VCO frequency will be (N) (reference) = (5525) (10.000 kHz) = 55.25 MHz. The VCO output is then divided by 1000 to produce the A10 output at 55.25 kHz.

The actual frequency of the A10 output may therefore be calculated from the following formula. F = 10 (6000 – XXX) Hz, where XXX is the value of the receiver 100 Hz, 10 Hz, and 1 Hz tuning increments, respectively.

3.3 Phase Comparator and Charge Pump Operation

Phase comparison of the 10 kHz reference and the 10 kHz VCO derived signal at the divide by N counter output is accomplished by a Phase Comparator internal to U6. When these two signals are equal in frequency and phase, the Phase Comparator outputs at TP2 and TP3 are essentially 5 Vdc. U8 functions as a buffer for the Phase Comparator to the input of the charge pump circuit, consisting of Q5, Q6, and Q7. This 5 volt level holds Q6 and Q7 off. Consequently, Q5 is also off and the voltage across C24 is at some constant level. This biases Q4 to some specific source current, and the voltage across R16 at TP1 is constant. This VCO control voltage holds the VCO frequency constant, somewhere between 50 and 60 MHz.

Assume that the VCO derived feedback signal at the divide by N counter output is suddenly less than the reference frequency. This is what will happen at the instant the divide by N factor is increased. Since the two Phase Comparator inputs are no longer equal, the Phase Comparator will output a series of negative pulses at TP3. Q7 will turn on, forcing Q5 on. Q5 will start to pump charge into C24, causing Q4 to conduct more current as the voltage across C24 increases. This produces a higher dc level at TP1. The VCO frequency will increase in response to it until the signals at the Phase Comparator inputs are again equal. As the VCO derived signal is approaching the reference frequency, the output pulse width at TP3 will get smaller until the signal is essentially +5 Vdc again. Q7 and Q5 will turn off. The voltage at C24 will rest at this new higher dc value causing the VCO frequency to also rest at its new higher value.

Assume that the VCO feedback signal at the divide by N counter output is suddenly greater than the reference signal (meaning that the divide by N factor has just decreased). The two Phase Comparator inputs are again unequal, but now the Phase Comparator will output the negative pulses at TP2. Q6 will turn on, drawing charge out of C24, and causing the VCO control voltage to drop. Consequently, the VCO will shift lower in frequency, and the VCO derived signal at the Phase Comparator input will again approach the reference frequency. The output pulses will become very narrow, approaching 5 Vdc. Q6 will turn off, and equilibrium at the new lower VCO frequency will be obtained.

3.4 VCO Operation and Control

A charge pump circuit consisting of Q5, Q6, Q7, and associated components in conjunction with filters C24 and C25 convert the two Phase Comparator pulse outputs into an analog dc control voltage. Buffer amplifier Q4 applies this control voltage to the varactor diode string in the VCO. The VCO itself is a JFET (Q3) Hartley oscillator stage whose frequency shifts as the capacitance of the varactor diodes changes with changes in control voltage. A net control voltage change of 5 Vdc to 10 Vdc produces a net VCO frequency shift of 50 MHz to 60 MHz. Note also that the 10 volt limit corresponds to N = 6000 while the 5 volt limit corresponds to N = 5001.

The VCO output is fed through 10 dB attenuator network R10-R11 to a +20 dB gain amplifier stage consisting of Q1, Q2, and associated components. This output is split and sent to divide by N circuit U5 and

U6 and to a divide by 1000 divider chain consisting of U1, U2, and U3. This divider output is therefore at a frequency range of 50.01 to 60 kHz (in 10 Hz increments) and is the PLL V output. This output is fed through J5 to PLL IV Assembly A9 where further signal processing occurs.

3.5 BITE Circuits

The A10 assembly contains two circuits for self-test evaluation.

- Lock detector Q8 whose output is 0 Vdc whenever the PLL is tracking properly. This line is constantly monitored by the A14 assembly. It will cause a front panel fault light to appear if the loop ever unlocks.

- Serial Data check that verifies the tuning data from the A14 assembly has been received and properly translated into the correct divide by N factor. A serial data word is sent on the data line (J1 pin 10) and the U6 serial data check line is read back to the A14 assembly (J1 pin 7).. If the word has been received and properly decoded, this line will pulse to +5 Vdc. The serial data check occurs automatically, but only when the receiver BITE self-test is actuated.

4. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. All tests should be performed with all connections in normal contact, unless otherwise specified.

4.1 VCO Frequency Adjustment

a. Connect equipment as shown in figure 1.

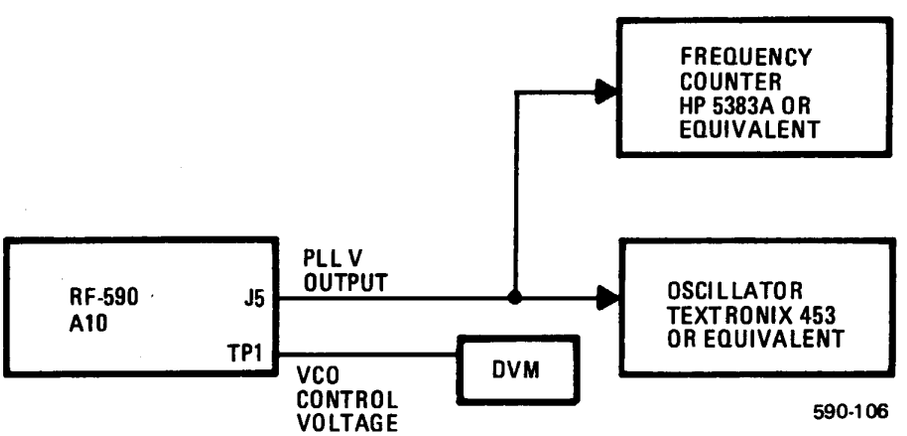

Figure 1. PLL V VCO Adjustment

b. Set RF-590 frequency to 00.000500 MHz.

c. Adjust C20 for 7.5 Vdc at TP1. PLL V output vs. receiver tune frequency should agree with table 2. The output waveform should always be a TTL signal.

Table 2. VCO Frequency Range

Receiver Tune Frequency, MHz	PLL V Output Frequency, kHz	Approximate TP1 Voltage, Vdc
00.000500	55.00	7.5
00.000000	60.00	10.0
00.000999	50.01	5.0

d. Fully reconnect the A10 assembly to RF-590. Initiate BITE self-test. Receiver must pass all tests associated with assembly A10. Test is complete.

5. PARTS LIST

Table 3 is a comprehensive parts list of all replaceable components in PLL V Assembly A10. When ordering parts from the factory, include a full description of the part. Use figure 2, PLL V Assembly A10 Component Parts Location Diagram to identify parts.

6. SCHEMATIC DIAGRAM

Figure 3 is the PLL V Assembly A10 schematic diagram.

Table 3. PLL V Assembly A10 Parts List (PL 10073-4500)

Ref. Desig.	Part Number	Description
	10073-4500	PWB, PLL 5
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	C26-0025-470	CAP 47UF 20% 25V TANT
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/01-1535	CAP .01UF 20% 100V CER
C5	CK05BX102M	CAP 1000PF 20% 200V CER
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310	CAP .1UF 10% 100V CER-R
C9	M39014/01-1535	CAP .01UF 20% 100V CER
C10	M39014/01-1535	CAP .01UF 20% 100V CER
C11	M39014/01-1535	CAP .01UF 20% 100V CER
C12	M39014/01-1535	CAP .01UF 20% 100V CER
C13	CK05BX102M	CAP 1000PF 20% 200V CER
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R

Table 3. PLL V Assembly A10 Parts List (PL 10073-4500) (Cont.)

Ref. Desig.	Part Number	Description
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310	CAP .1UF 10% 100V CER-R
C17	C26-0025-680	CAP 68UF 20% 25V TANT
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	M39014/01-1535	CAP .01UF 20% 100V CER
C20	C84-0003-008	CAP 3-15PF 200V CER
C21	CK05BX102M	CAP 1000PF 20% 200V CER
C22	CK05BX102M	CAP 1000PF 20% 200V CER
C23	C26-0025-100	CAP 10UF 20% 25V TANT
C24	C25-0003-004	CAP 0.33UF 10% 50V TANT
C25	M39014/01-1546	CAP FXD CER 039UF
C26	C26-0025-470	CAP 47UF 20% 25V TANT
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C28	C26-0035-109	CAP 1.0UF 20% 35V TANT
C29	C26-0016-151	CAP 150UF 20% 16V TANT
C30	M39014/02-1310	CAP .1UF 10% 100V CER-R
C31	C26-0025-100	CAP 10UF 20% 25V TANT
C32	M39014/02-1310	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310	CAP .1UF 10% 100V CER-R
C34	M39014/02-1310	CAP .1UF 10% 100V CER-R
C35	C26-0035-109	CAP 1.0UF 20% 35V TANT
C36	M39014/02-1310	CAP .1UF 10% 100V CER-R
C37	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	M39014/02-1310	CAP .1UF 10% 100V CER-R
C39	M39014/02-1310	CAP .1UF 10% 100V CER-R
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C41	M39014/02-1310	CAP .1UF 10% 100V CER-R
C43	C26-0025-470	CAP 47UF 20% 25V TANT
CR1	10073-7118	DIODE, SILICON, HYPERABRUPT
CR2	10073-7118	DIODE, SILICON, HYPERABRUPT
CR3	10073-7118	DIODE, SILICON, HYPERABRUPT
CR4	10073-7118	DIODE, SILICON, HYPERABRUPT
CR5	10073-7118	DIODE, SILICON, HYPERABRUPT
CR6	10073-7118	DIODE, SILICON, HYPERABRUPT
CR7	10073-7118	DIODE, SILICON, HYPERABRUPT
CR8	10073-7118	DIODE, SILICON, HYPERABRUPT
CR9	1N6263	DIODE, HOT CARRIER
CR10	1N3064	DIODE 75mA 75V SW
CR11	10073-7118	DIODE, SILICON, HYPERABRUPT
CR12	10073-7118	DIODE, SILICON, HYPERABRUPT
J1	J46-0032-010	HDR 10 PIN 0.100" SR
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
J5	J-0031	CONN SMB VERT PCB F

Table 3. PLL V Assembly A10 Parts List (PL 10073-4500) (Cont.)

Ref. Desig.	Part Number	Description
L1	MS14046-9	COIL 27UH 10% FXD RF
L2	MS75084-3	COIL 1.8UH 10% FXD RF
L3	MS75084-10	COIL 6.8UH 10% FXD RF
L4	L08-0001-001	CHOKE W B 50 MHZ
Q1	Q35-0003-000	XSTR U310 JFET HIGH GM
Q2	2N2369	XSTR SS/RF NPN
Q3	Q35-0003-000	XSTR U310 JFET HIGH GM
Q4	Q05-0001-000	XSTR JFET N-CH
Q5	2N2907	XSTR SS/GP PNP TO-18
Q6	2N2222	XSTR SS/GP NPN TO-18
Q7	2N2222	XSTR SS/GP NPN TO-18
Q8	2N2907	XSTR SS/GP PNP TO-18
R1	R65-0003-201	RES 200 5% 1/4W CAR FILM
R2	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R3	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R4	R65-0003-270	RES 27 5% 1/4W CAR FILM
R5	R65-0003-201	RES 200 5% 1/4W CAR FILM
R6	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R7	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R8	R65-0003-100	RES 10 5% 1/4W CAR FILM
R9	R65-0003-151	RES 150 5% 1/4W CAR FILM
R10	R65-0003-101	RES 100 5% 1/4W CAR FILM
R11	R65-0003-201	RES 200 5% 1/4W CAR FILM
R12	R65-0003-101	RES 100 5% 1/4W CAR FILM
R13	R65-0003-470	RES 47 5% 1/4W CAR FILM
R14	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R15	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R16	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R17	RN55D3651F	RES,3650 1% 1/8W MET FLM
R18	R65-0003-470	RES 47 5% 1/4W CAR FILM
R19	R65-0003-470	RES 47 5% 1/4W CAR FILM
R20	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R21	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R22	RN55D9091F	RES,9090 1% 1/8W MET FLM
R23	RN55D3321F	RES,3320 1% 1/8W MET FLM
R24	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R25	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R26	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R27	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R28	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R29	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R30	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R31	R65-0003-103	RES 10K 5% 1/4W CAR FILM
T1	10073-7002	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"

Table 3. PLL V Assembly A10 Parts List (PL 10073-4500) (Cont.)

Ref. Desig.	Part Number	Description
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	165-0004-001	IC 12013 PLASTIC ECL
U2	105-0000-090	IC 74LS90 PLASTIC TTL
U3	105-0000-090	IC 74LS90 PLASTIC TTL
U4	105-0000-090	IC 74LS90 PLASTIC TTL
U5	165-0004-001	IC 12013 PLASTIC ECL
U6	170-0002-001	IC MC145156 PLASTIC CMOS
U7	101-0000-019	IC 4050B PLASTIC CMOS
U8	105-0000-000	IC 74LS00 PLASTIC TTL
U9	105-0000-000	IC 74LS00 PLASTIC TTL
VR1	111-0001-001	IC VR 7805 + 5V 1.5A 4%

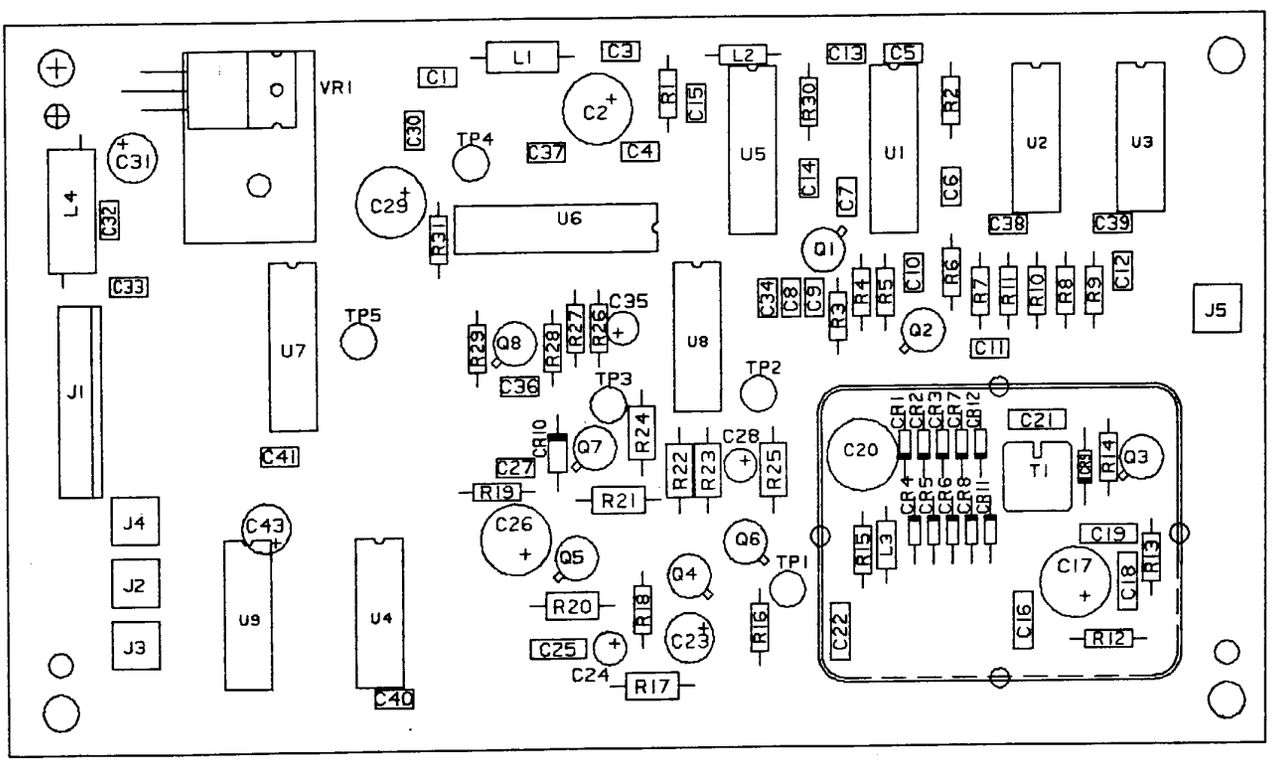

Figure 2. PLL V Assembly A10 Component Location Diagram (10073-4500, Rev. C)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS
4. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

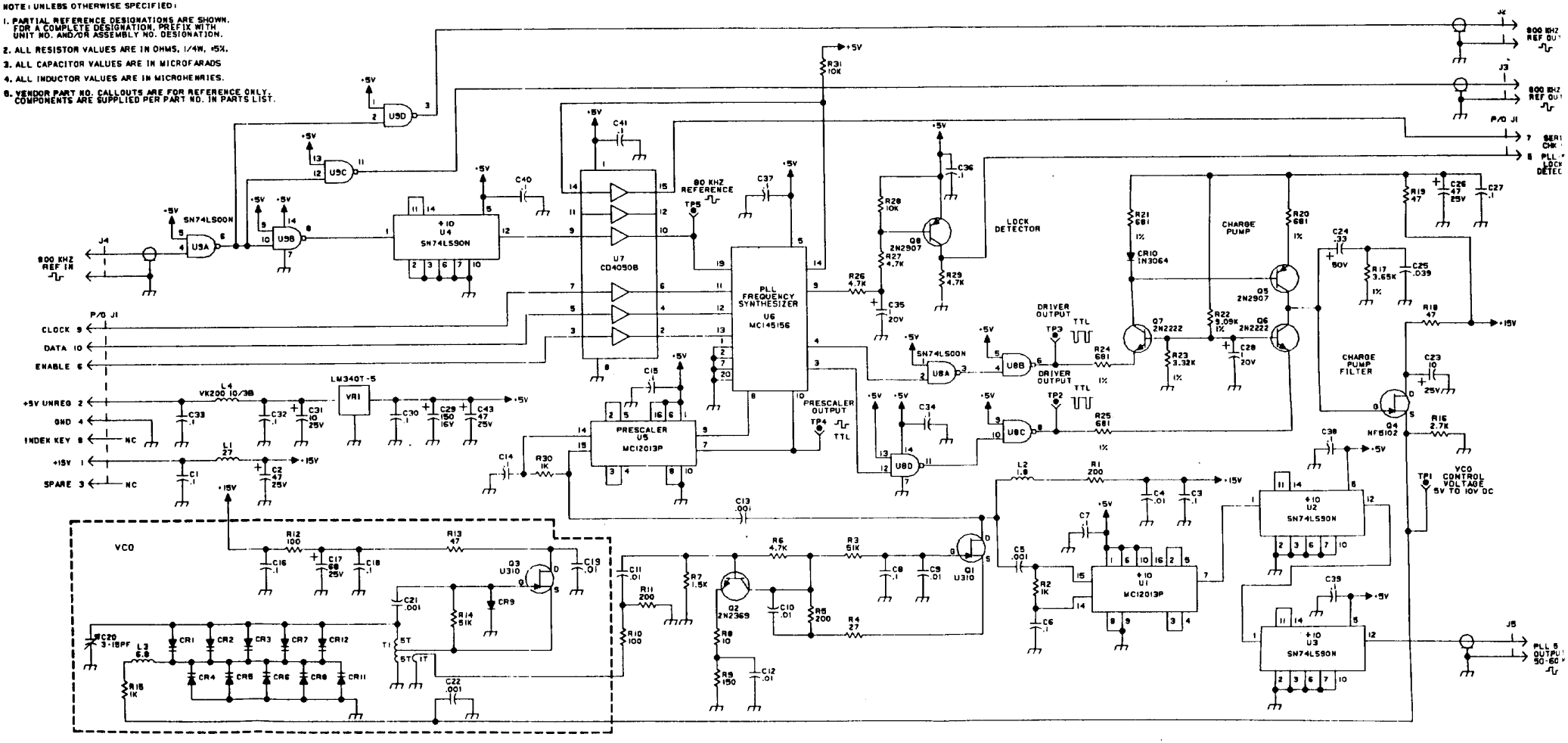

Figure 3. PLL V Assembly A10 Schematic Diagram (10073-4501, Rev. E)

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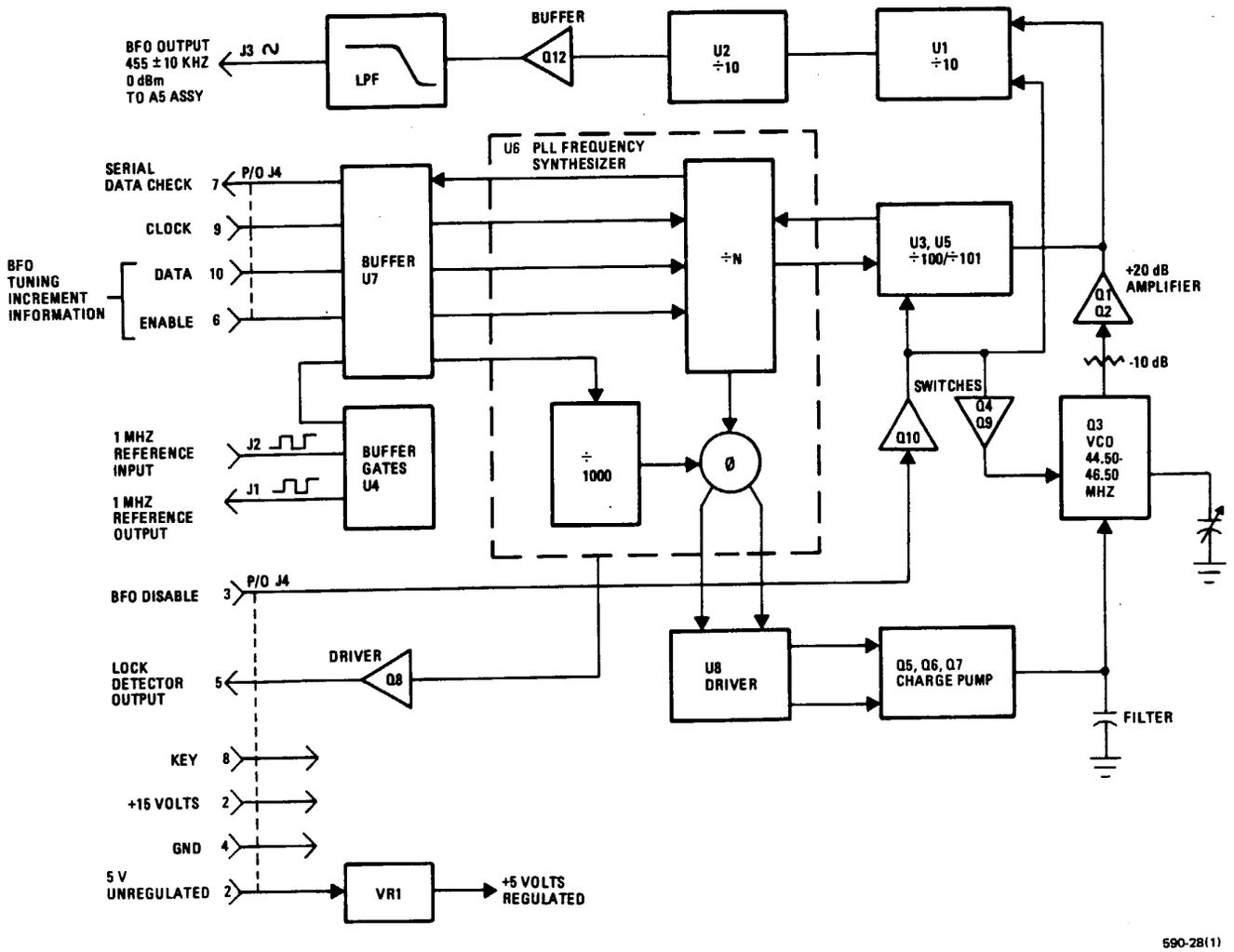

BFO Assembly A11 Functional Block Diagram

1. GENERAL DESCRIPTION

The A11 BFO Synthesizer Assembly is a single phase locked loop synthesizer that provides the BFO offset injection required for proper CW or SB reception. The BFO range is ± 10 kHz around 455 kHz. It is selected via RF-590 BFO selection controls in 10 Hz increments.

Frequency select input data is applied to the A11 assembly in serial data form under Control Board Assembly A14 microprocessor control. A11 output is applied to IF/Audio Assembly A5 where it mixes with the second IF of 455 kHz to permit proper CW and SB demodulation.

2. INTERFACE CONNECTIONS

Table 1 lists the various input/output connections and other relevant data.

Table 1. A11 BFO Synthesizer Interface Connections

Connector	Function	Characteristics
J1	1 MHz Reference Output	TTL
J2	1 MHz Reference Input	TTL
J3	BFO Output	455 kHz ± 10 kHz, 0 dBm
J4-1	+15 V	Approximately 20 mA
J4-2	+5.0 V Unregulated	Approximately 200 mA
J4-3	BFO Disable	+5 V = BFO Disabled
J4-4	GND	
J4-5	Lock Detector Output	P/O BITE, +5 V = Unlocked, 0V = Locked
J4-6	Enable	+ going pulse = Enabled
J4-7	Serial Data Check	P/O BITE Testing, +5 Vdc = ok
J4-8	Key	
J4-9	Clock	TTL, 750 kHz
J4-10	Data	TTL

3. CIRCUIT DESCRIPTION

NOTE

A11 operation is similar to the general divide by N PLL and charge pump circuits described in section 4. Reviewing section 4 at this point would aid in understanding A11 operation.

3.1 Reference Generation

A 1 MHz signal from Reference Generator Assembly A12 enters the A11 BFO synthesizer at J2. This signal is buffered by TTL NAND gates in U4 and directed to J1, a spare 1 MHz output. It is also routed to a divide by 1000 counter (internal to U6) via buffer stage U7 to produce a 1 kHz reference signal. Since this has been ultimately derived from the RF-590 crystal frequency standard via the A12 assembly, stable and accurate A11 operation is assured.

3.2 Divide by N Counter

Since the A11 assembly requires a variable output frequency (455 kHz ± 10 kHz), a programmable counter has been incorporated into the VCO feedback path to the phase comparator. This counter consists of dual modulus ÷ 100/÷ 101 prescaler network U5 and U3 and a programmable counter internal to U6. Together this circuit creates a total division range of N = 44,500 to N = 46,500, where N is a function of the receiver BFO offset tune positions.

The output of the divide by N counter will always attempt to equal the 1 kHz reference frequency at the phase comparator inputs (despite changes in the divide by N factor due to changing the 1 kHz, 100 Hz, and/or 10 Hz BFO offset tuning positions). To accomplish this, VCO frequency will change in response to command signals generated by the phase comparator output. The VCO frequency will always equal (N) (reference frequency) or (N) (1000 Hz) = 44.50 MHz to 46.50 MHz.

Selection of a BFO offset frequency from the front panel causes Control Assembly A14 to generate a serial data code containing information about the frequency chosen. This code is applied synchronously with the 750 kHz system clock to U6 whenever the U6 enable line is gated open by A14.

The value of N may be found from the formula, N = (45,500 – XXX), where XXX is the ± value of the 1 kHz, 100 Hz, and 10 Hz BFO offset tuning positions. For example, tuning the BFO offset to +5.00 kHz would make N = 45,500 – (+500) = 45,000. The VCO frequency would be (N) (reference) = (45,000) (1000) = 45.00 MHz. There is a divide by 100 counter at the VCO output, so the BFO output at J3 would be 450 kHz. Note that as the selected BFO offset frequency increases the BFO output frequency must decrease.

In summary, the BFO output frequency may be calculated from the following formula, F = 10 (45,500 – XXX) Hz, where ± XXX represents the value of the 1 kHz, 100 Hz, and 10 Hz BFO offset tune frequency.

3.3 Phase Comparator and Charge Pump Operation

Phase comparison of the 1 kHz reference and the 1 kHz VCO derived signal at the divide by N counter output is accomplished by a phase comparator internal to U6.

When these two signals are equal in frequency and phase, the phase comparator outputs at TP4 and TP5 are essentially 5 Vdc. U8 buffers this level to the charge pump circuit where +5 Vdc on the Q6 and Q7 emitters holds both transistors off. Q5 is also off, and the voltage at TP1 (across C24) is constant. This level holds the VCO frequency constant between 44.5 MHz and 46.5 MHz.

Assume that the division ratio of U3, U5, and U6 is changed so that the VCO derived feedback signal is less than the 1 kHz reference. (This will happen if the divide by N factor increases.) The phase comparator will output a series of negative going pulses at TP4 whose pulse widths are a function of the difference in frequency. Q7 will turn on during these negative periods, and its collector voltage drops. This permits Q5 to turn on and pump charge into C24. This causes the C24 voltage to increase, which in turn causes an increase in the VCO frequency. The VCO frequency increases until the signals at the U6 phase comparator inputs are equal. At this time, the phase comparator output error pulse width will have decreased to an extremely small value. TP4 is essentially at 5 Vdc, Q5 and Q7 turn off, and no further increase in the voltage across C24 will occur. The VCO will therefore rest at a new higher frequency.

Assume that the division ratio changes so the VCO derived feedback signal is greater than the 1 kHz reference. U6 will pulse low at TP5, causing Q6 to turn on. C24 will start to discharge through Q6 to ground, and its voltage drops. This causes the VCO to decrease in frequency until the inputs at the phase comparator are equal. Again, the output error pulse width will have decreased to an extremely small value. TP5 will be at essentially 5 Vdc, Q6 will turn off, the C24 voltage will no longer decrease, and the VCO frequency will rest at this new lower value.

3.4 VCO Operation and Control

Buffer stage U8 applies the phase comparator outputs to a charge pump circuit consisting of Q5, Q6, Q7, and associated components followed by filters C24 and C25. This stage converts the two phase comparator pulse outputs into an analog dc control voltage. This control voltage is then applied to the varactor diode string in the VCO. It controls the operating frequency of JFET Hartley oscillator stage Q3. A net control voltage change of 6.5 Vdc to 8.5 Vdc produces a VCO frequency range of 44.500 MHz to 46.500 MHz.

The VCO output is fed through -10 dB attenuator network R10-R11 and to 20 dB gain amplifier stage, Q1 and Q2. The signal is then split and sent to the divide by N circuit U3, U5, and U6 (to complete the feedback loop) and to divide by 100 chain U1 and U2. U2 TLL output at 455 to 465 kHz is applied through buffer stage Q12 to a low pass filter (LPF) network. LPF output is a 455 kHz ± 10 kHz, 0 dBm sine wave and is fed through J3 to IF/Audio Assembly A5 to become the BFO injection frequency.

BFO disabling occurs whenever the receiver is in any mode other than LSB, USB, ISB, or CW modes. This occurs in response to a +5 Vdc command by the A14 assembly at J4, pin 3. This signal disables the VCO

by turning Q10 on. This turns Q4 on. Q4 then removes base drive to Q9. Q9 turns off and removes the supply voltage from oscillator stage Q3. Also, Q10's on state forward biases diodes CR14 and CR15, which shorts out the signals at the U1 and U5 inputs.

3.5 BITE Circuits

The A11 assembly contains two circuits for self-test evaluation.

- Lock detector Q8 whose output is 0 Vdc whenever the PLL is tracking properly. This line is constantly monitored by Control Assembly A14. A front panel fault light will appear if the loop ever unlocks.

- Serial data check that verifies that the tuning data from the A14 assembly has been received and properly translated into the correct divide by N factor. A serial data word is sent by the A14 assembly on the BFO tuning data line (J4 pin 10) and the U6 SW1 output is read at J4, pin 7. If the word has been received and properly decoded, this line will pulse to +5 Vdc. The serial data check test occurs automatically, but only when the receiver BITE self-test is actuated.

4. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. A11 tests should be performed with all connections in normal contact, unless otherwise specified.

4.1 VCO Adjustment

Perform this procedure to align the VCO.

a. Connect equipment as shown in figure 1.

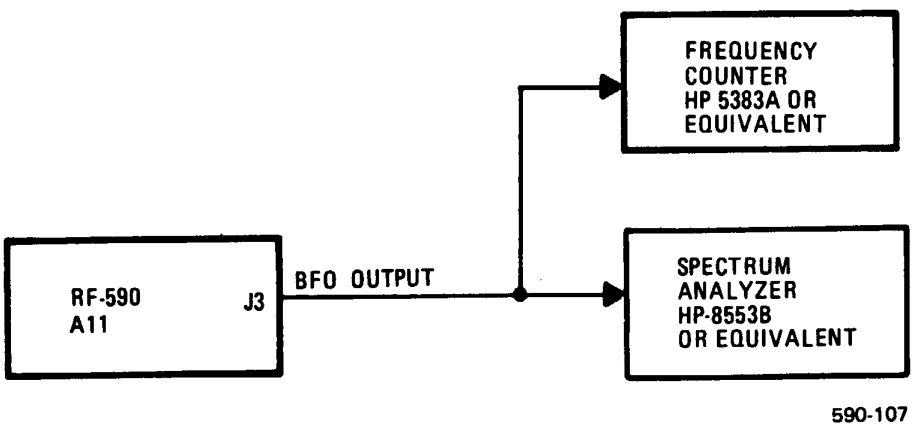

Figure 1. BFO VCO Alignment

NOTE

A11J3 mates with A5A1J2 through a hole in the chassis. It will be necessary to remove the A5 assembly to gain access to A11J3.

b. Set RF-590 controls as follows:

- Frequency to 10.000000 MHz
- MODE to USB
- BFO to 0.00 kHz

c. Monitor TP1 with a digital voltmeter. Adjust C20 for 7.0 Vdc.

d. Check that the BFO output frequency (as a function of the front panel BFO settings) agree with table 2. (BFO output amplitude should always be 0 dBm ± 2 dB.)

Table 2. BFO Frequency Offset

BFO Offset Frequency Selected	BFO Output Frequency	Approximate Voltage at TP1
0.00 kHz	455.00 kHz	7.0
+9.99 kHz	445.01 kHz	6.0
-9.99 kHz	464.99 kHz	8.0

e. Fully reconnect the A11 assembly to the RF-590. Initiate BITE self-test. Receiver must pass all tests associated with the A11 assembly. Test is complete.

5. PARTS LIST

Table 3 is a comprehensive parts list of all replaceable components in BFO Assembly A11. When ordering parts from the factory, include a full description of the part. Use figure 2, BFO Assembly A11 Component Location Diagram to identify parts.

6. SCHEMATIC DIAGRAM

Figure 3 is the BFO Assembly A11 schematic diagram.

Table 3. BFO Assembly A11 Parts List (PL 10073-4600)

Ref. Desig.	Part Number	Description
	10073-4600	PWB
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	C26-0025-470	CAP 47UF 20% 25V TANT
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/01-1535	CAP .01UF 20% 100V CER
C5	CK05BX102M	CAP 1000PF 20% 200V CER
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310	CAP .1UF 10% 100V CER-R
C9	M39014/01-1535	CAP .01UF 20% 100V CER
C10	M39014/01-1535	CAP .01UF 20% 100V CER
C11	M39014/01-1535	CAP .01UF 20% 100V CER
C12	M39014/01-1535	CAP .01UF 20% 100V CER
C13	CK05BX102M	CAP 1000PF 20% 200V CER
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310	CAP .1UF 10% 100V CER-R
C17	C26-0025-680	CAP 68UF 20% 25V TANT
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	M39014/01-1535	CAP .01UF 20% 100V CER
C20	C84-0003-004	CAP 9-35PF 200V CER
C21	CK05BX102M	CAP 1000PF 20% 200V CER
C22	CK05BX102M	CAP 1000PF 20% 200V CER
C23	C26-0025-680	CAP 68UF 20% 25V TANT
C24	C25-0003-107	CAP 1.0UF 10% 35V TANT
C25	C25-0003-004	CAP 0.33UF 10% 50V TANT
C26	C26-0025-100	CAP 10UF 20% 25V TANT
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C28	C25-0001-301	CAP 1.0UF 20% 20V TANT
C29	C26-0016-151	CAP 150UF 20% 16V TANT
C30	M39014/02-1310	CAP .1UF 10% 100V CER-R
C31	C26-0025-100	CAP 10UF 20% 25V TANT
C32	M39014/02-1310	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310	CAP .1UF 10% 100V CER-R
C34	M39014/02-1310	CAP .1UF 10% 100V CER-R
C35	C25-0001-301	CAP 1.0UF 20% 20V TANT
C36	M39014/02-1310	CAP .1UF 10% 100V CER-R
C37	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	M39014/02-1310	CAP .1UF 10% 100V CER-R
C39	M39014/02-1310	CAP .1UF 10% 100V CER-R
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C41	M39014/02-1310	CAP .1UF 10% 100V CER-R
C42	M39014/02-1310	CAP .1UF 10% 100V CER-R
C43	M39014/02-1310	CAP .1UF 10% 100V CER-R
C44	6628-0660	CAP 5600PF 5% 300V MICA

Table 3. BFO Assembly A11 Parts List (PL 10073-4600) (Cont.)

Ref. Desig.	Part Number	Description
C45	CM06FD272J03	CAP 2700PF 5% 500V MICA
C46	CM06FD751J03	CAP 750PF 5% 500V MICA
C47	C-2503	CAP 820PF 2% 300V MICA
C48	6628-0660	CAP 5600PF 5% 300V MICA
C49	CM06FD272J03	CAP 2700PF 5% 500V MICA
C50	M39014/02-1310	CAP .1UF 10% 100V CER-R
C51	M39014/01-1535	CAP .01UF 20% 100V CER
C52	M39014/01-1535	CAP .01UF 20% 100V CER
CR1	10073-7118	DIODE, SILICON, HYPERABRUPT
CR2	10073-7118	DIODE, SILICON, HYPERABRUPT
CR3	10073-7118	DIODE, SILICON, HYPERABRUPT
CR4	10073-7118	DIODE, SILICON, HYPERABRUPT
CR5	10073-7118	DIODE, SILICON, HYPERABRUPT
CR6	10073-7118	DIODE, SILICON, HYPERABRUPT
CR7	10073-7118	DIODE, SILICON, HYPERABRUPT
CR8	10073-7118	DIODE, SILICON, HYPERABRUPT
CR9	10073-7118	DIODE, SILICON, HYPERABRUPT
CR10	10073-7118	DIODE, SILICON, HYPERABRUPT
CR11	1N6263	DIODE, HOT CARRIER
CR12	1N3064	DIODE 75mA 75V SW
CR13	1N3064	DIODE 75mA 75V SW
CR14	1N3064	DIODE 75mA 75V SW
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J46-0032-010	HDR 10 PIN 0.100" SR
L1	MS14046-9	COIL 27UH 10% FXD RF
L2	MS75084-3	COIL 1.8UH 10% FXD RF
L3	MS75084-10	COIL 6.8UH 10% FXD RF
L4	L08-0001-001	CHOKE W B 50 MHZ
L5	MS14046-7	COIL 18UH 10% FXD RF
Q1	Q35-0003-000	XSTR U310 JFET HIGH GM
Q2	2N2369	XSTR SS/RF NPN
Q3	Q35-0003-000	XSTR U310 JFET HIGH GM
Q4	2N2907	XSTR SS/GP PNP TO-18
Q5	2N2907	XSTR SS/GP PNP TO-18
Q6	2N2222	XSTR SS/GP NPN TO-18
Q7	2N2222	XSTR SS/GP NPN TO-18
Q8	2N2907	XSTR SS/GP PNP TO-18
Q9	2N2907	XSTR SS/GP PNP TO-18
Q10	2N2222	XSTR SS/GP NPN TO-18
Q11	2N5088	XSTR SS/GP
Q12	2N2222	XSTR SS/GP NPN TO-18
R1	R65-0003-201	RES 200 5% 1/4W CAR FILM
R2	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM

Table 3. BFO Assembly A11 Parts List (PL 10073-4600) (Cont.)

Ref. Desig.	Part Number	Description
R3	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R4	R65-0003-270	RES 27 5% 1/4W CAR FILM
R5	R65-0003-201	RES 200 5% 1/4W CAR FILM
R6	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R7	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R8	R65-0003-100	RES 10 5% 1/4W CAR FILM
R9	R65-0003-151	RES 150 5% 1/4W CAR FILM
R10	R65-0003-101	RES 100 5% 1/4W CAR FILM
R11	R65-0003-201	RES 200 5% 1/4W CAR FILM
R12	R65-0003-101	RES 100 5% 1/4W CAR FILM
R13	R65-0003-270	RES 27 5% 1/4W CAR FILM
R14	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R15	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R16	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R17	RN55D5621F	RES,5620 1% 1/8W MET FLM
R18	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R19	R65-0003-561	RES 560 5% 1/4W CAR FILM
R20	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R21	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R22	RN55D9091F	RES,9090 1% 1/8W MET FLM
R23	RN55D3321F	RES,3320 1% 1/8W MET FLM
R24	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R25	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R26	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R27	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R28	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R29	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R30	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R31	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R32	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R33	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R34	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R35	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R36	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R37	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R38	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R39	R65-0003-151	RES 150 5% 1/4W CAR FILM
R40	R65-0003-750	RES 75 5% 1/4W CAR FILM
R41	R65-0003-103	RES 10K 5% 1/4W CAR FILM
T1	10073-7003	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"

Table 3. BFO Assembly A11 Parts List (PL 10073-4600) (Cont.)

Ref. Desig.	Part Number	Description
TP6	J-0072	TP PWB BLU TOP ACCS .080"
U1	165-0004-001	IC 12013 PLASTIC ECL
U2	105-0000-090	IC 74LS90 PLASTIC TTL
U3	105-0000-168	IC 74LS168 PLASTIC TTL
U4	105-0000-000	IC 74LS00 PLASTIC TTL
U5	165-0004-001	IC 12013 PLASTIC ECL
U6	170-0002-001	IC MC145156 PLASTIC CMOS
U7	101-0000-019	IC 4050B PLASTIC CMOS
U8	105-0000-000	IC 74LS00 PLASTIC TTL
VR1	111-0001-001	IC VR 7805 + 5V 1.5A 4%

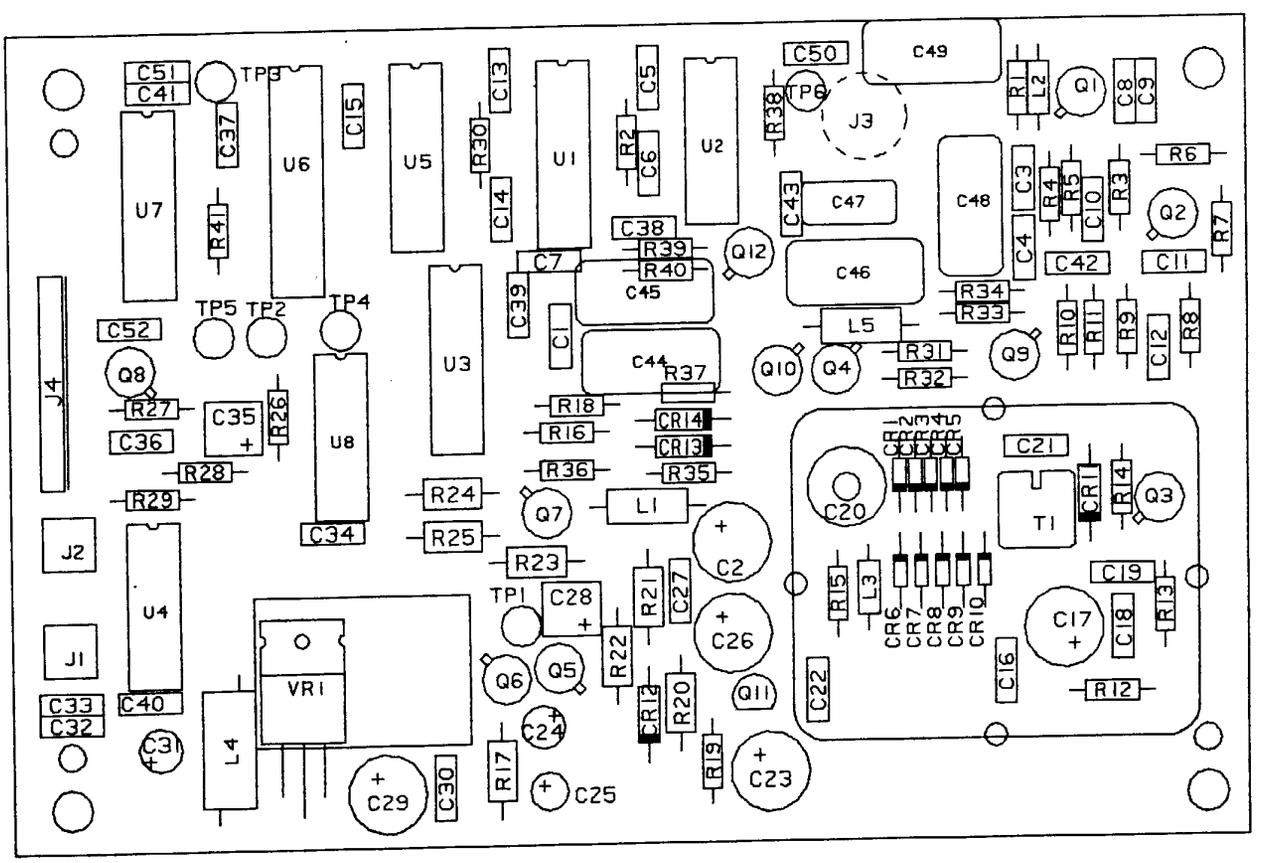

Figure 2. BFO Assembly A11 Component Location Diagram (10073-4600, Rev. C)

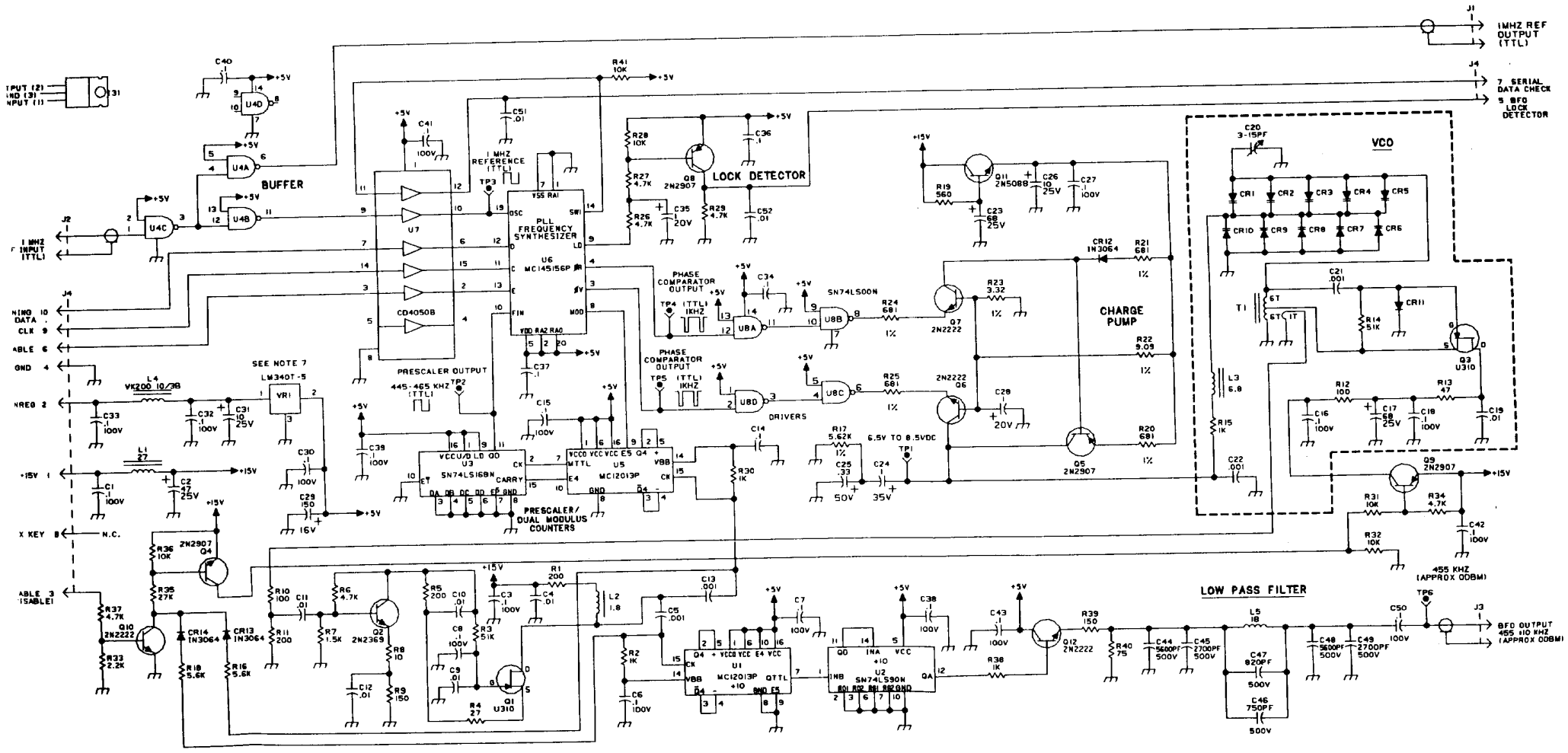

Figure 3. BFO Assembly A11 Schematic Diagram (10073-4601, Rev. F)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS, 200V.
4. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
6. TTL LEVEL IS NORMALLY .6V LOW AND APPROX. 4V HIGH.
7. TOP VIEW OF VR1.